# SY21034

## High-Efficiency, 200kHz, 100V Input, 0.6A Asynchronous Step-Down Regulator

## General Description

The SY21034 high-efficiency asynchronous step-down DC/DC regulator can deliver 0.6A current over a wide input voltage range from 4.5V to 100V. It uses constant-off-time and peak-current-mode control to achieve fast transient response, and integrates a main switch with low $R_{DS(ON)}$ to minimize conduction loss.

The 200kHz switching frequency permits low output-voltage ripple and reduces external inductor and capacitor sizes. The SY21034 also provides cycle-by-cycle current limiting and hiccup short-circuit protection.

The SY21034 is available in a compact TSOT23-6 package.

## Features

- 4.5V to 100V Input Voltage Range
- Up to 0.6A Output Current
- Low $R_{DS(ON)}$ for Internal N-Channel power FET: 1Ω
- 200kHz Pseudo-constant Switching Frequency
- Constant Off-Time and Peak-Current-Mode control
- Internal Soft-Start
- 0.6V ±1% Reference
- Hiccup Mode Short-Circuit Protection
- EN On/Off Control with Accurate Threshold
- Cycle-by-Cycle Peak Current limit
- Compact TSOT23-6 Package

## Applications

- Non-Isolated Telecommunication Buck Regulator
- Secondary High-Voltage Post Regulator
- Automotive Systems
- Electric Bicycles

## Typical Application

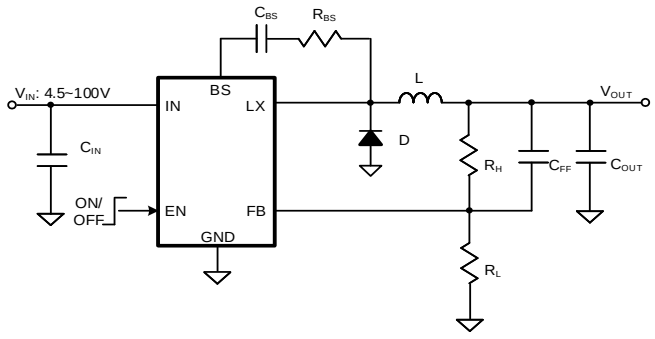



*Figure 1. Typical Application Circuit*

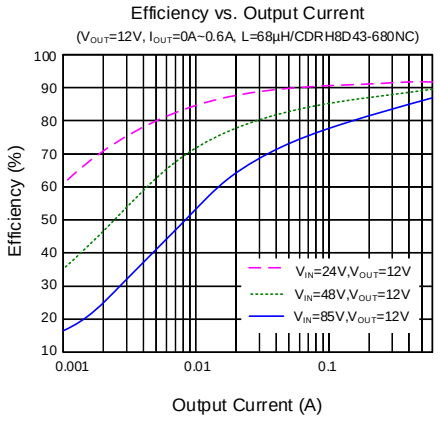


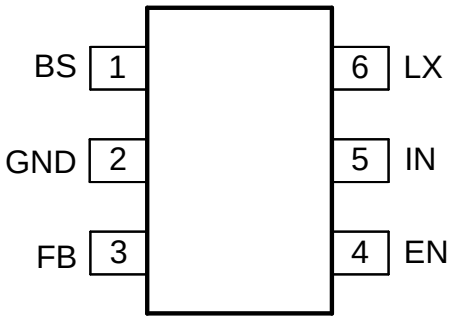

*Figure 2. Efficiency vs. Output Current*

## Ordering Information

| Ordering Part Number | Package type | Top Mark |
|---|---|---|
| SY21034ADC | TSOT23-6<br>RoHS-Compliant and Halogen-Free | **HD*xyz*** |

***x = year code, y = week code, z = lot number code***

## Pinout (top view)




(SOT23-6)

## Pin Description

| Pin No | Pin Name | Pin Description |
|---|---|---|
| 1 | BS | Bootstrap pin. Supply for the high-side gate driver. Connect a 0.1µF ceramic capacitor between the BS and the LX pin. |
| 2 | GND | Ground pin. |
| 3 | FB | Output feedback pin. Connect this pin to the center point of the output resistor-divider (as shown in Figure 1) to program the output voltage using the following equation: $V_{OUT} = 0.6 \times (1 + R_H / R_L)$ |
| 4 | EN | Enable control pin. Pull high to turn on. Do not leave floating. |
| 5 | IN | Input pin. Decouple this pin to the GND pin with at least a 4.7µF ceramic capacitor. |
| 6 | LX | Inductor pin. Connect this pin to the switching node of the inductor. |

## Block Diagram

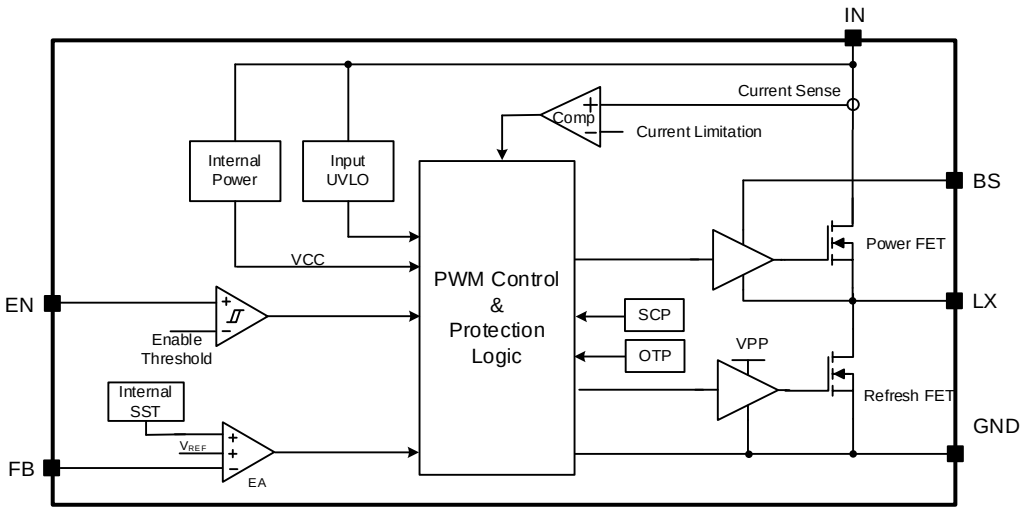



*Figure 3. Block Diagram*

## Absolute Maximum Ratings

| Parameter (Note 1) | Min | Max | Unit |
|---|---|---|---|
| IN | -0.3 | 100 | V |
| FB | -0.3 | 24 | |
| EN, LX | -0.3 | IN + 0.3 | |
| LX, 20ns duration | GND - 5 | IN + 3 | |
| Junction Temperature, Operating | -40 | 150 | °C |
| Lead Temperature (Soldering, 10s) | | 260 | |
| Storage Temperature | -65 | 150 | |

## Thermal Information

| Parameter (Note 2) | Typ | Unit |
|---|---|---|
| $\theta_{JA}$ Junction-to-Ambient Thermal Resistance | 100 | °C/W |
| $\theta_{JC}$ Junction-to-Case Thermal Resistance | 25 | |
| $P_D$ Power Dissipation $T_A$ = 25°C | 1 | W |

## Recommended Operating Conditions

| Parameter (Note 3) | Min | Max | Unit |
|---|---|---|---|
| IN | 4.5 | 100 | V |
| Junction Temperature | -40 | 125 | °C |
| Ambient Temperature | -40 | 85 | |

## Electrical Characteristics

($V_{IN}$ = 48V, $V_{OUT}$ = 12V, L = 68µH, $C_{OUT}$ = 10µF, $T_A$ = 25°C, $I_{OUT}$ = 0.1A, unless otherwise specified.)

| Parameter | | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Input | Voltage Range | $V_{IN}$ | | 4.5 | | 100 | V |
| | UVLO Rising Threshold | $V_{IN,UVLO}$ | | | | 4.5 | V |
| | UVLO Hysteresis | $V_{HYS}$ | | | 110 | | mV |
| | Quiescent Current | $I_Q$ | $I_{OUT}$ = 0A, $V_{FB}$ = 105% × $V_{REF}$ | | 100 | | µA |
| | Shutdown Current | $I_{SHDN}$ | $V_{EN}$ = 0V | | 9 | 20 | µA |
| Output | Reference Voltage | $V_{REF}$ | | 0.588 | 0.6 | 0.612 | V |
| | FB Input Current | $I_{FB}$ | $V_{FB}$ = $V_{IN}$ | -50 | | 50 | nA |
| | Soft-Start Time | $t_{SS}$ | | | 800 | | µs |
| MOSFET | Power FET $R_{DS(ON)}$ | $R_{DS(ON)}$ | | | 1 | | Ω |
| | Power FET Current Limit | $I_{LMT}$ | | 0.9 | | 1.3 | mA |
| Enable (EN) | Input Voltage High | $V_{EN,H}$ | | 1.14 | 1.2 | 1.26 | V |
| | Input Voltage Low | $V_{EN,L}$ | | 0.94 | 1 | 1.06 | V |
| COT | Switching Frequency | $f_{SW}$ | | 160 | 200 | 240 | kHz |
| | Minimum On-Time | $t_{ON,MIN}$ | | | 80 | | ns |
| | Minimum Off-Time | $t_{OFF,MIN}$ | | | 80 | | ns |
| OTP | Temperature | $T_{OTP}$ | | | 150 | | °C |
| | Temperature Hysteresis | $T_{HYS}$ | | | 15 | | °C |

**Note 1**: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2**: $\theta_{JA}$ is measured in the natural convection at $T_A$ = 25°C on a two-layer Silergy Evaluation Board.

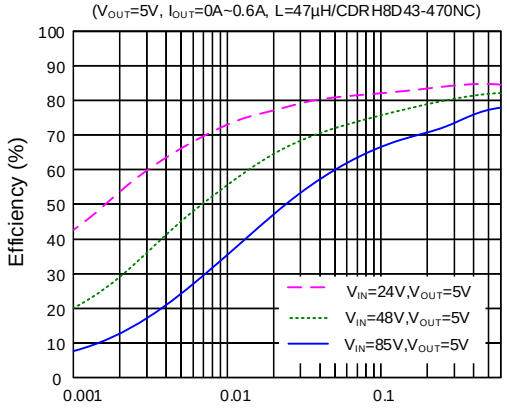
**Note 3:** The device is not guaranteed to function outside its operating conditions

# Typical Performance Characteristics

($V_{IN}$ = 12V, $V_{OUT}$ = 5V, L = 6.8μH, $C_{OUT}$ = 22μF, $T_J$ = 25°C, $I_{OUT}$ = 2A, unless otherwise noted)

Efficiency vs. Output Current

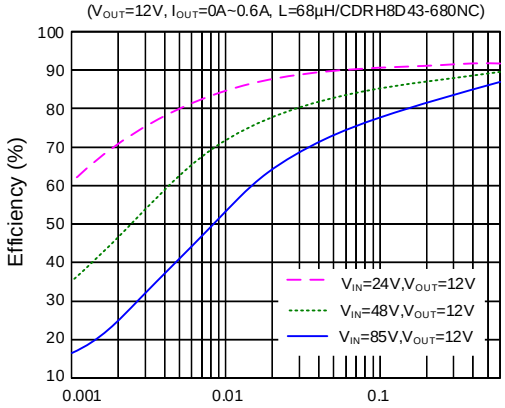
($V_{OUT}$=5V, $I_{OUT}$=0A~0.6A, L=47μH/CDRH8D43-470NC)




Output Current (A)

Efficiency vs. Output Current

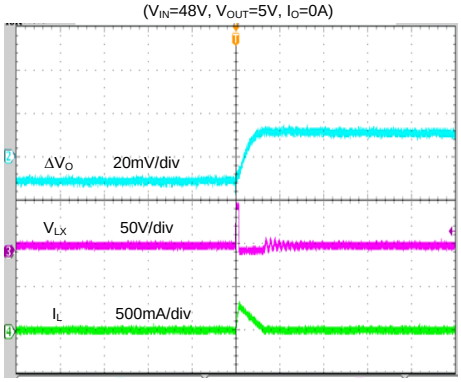
($V_{OUT}$=12V, $I_{OUT}$=0A~0.6A, L=68μH/CDRH8D43-680NC)




Output Current (A)

Output Ripple

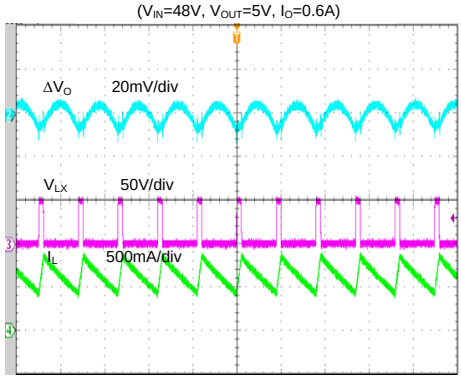
($V_{IN}$=48V, $V_{OUT}$=5V, $I_O$=0A)




Time (4μs/div)

Output Ripple

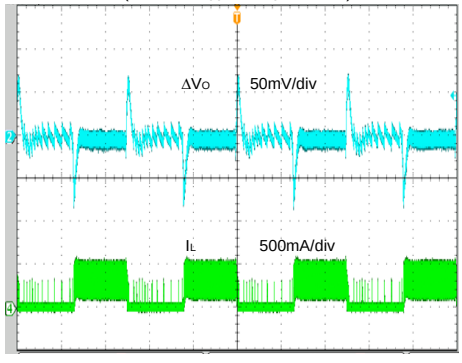
($V_{IN}$=48V, $V_{OUT}$=5V, $I_O$=0.6A)




Time (4μs/div)

Load Transient

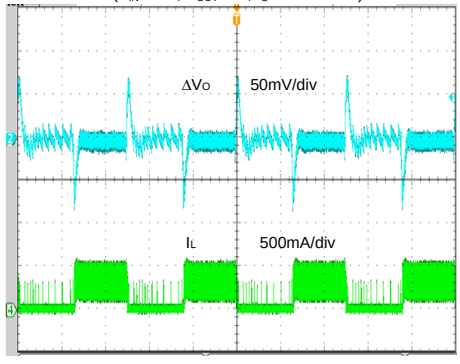
($V_{IN}$=48V, $V_{OUT}$=5V, $I_O$=0A-0.3A)




Time (400μs/div)

Load Transient

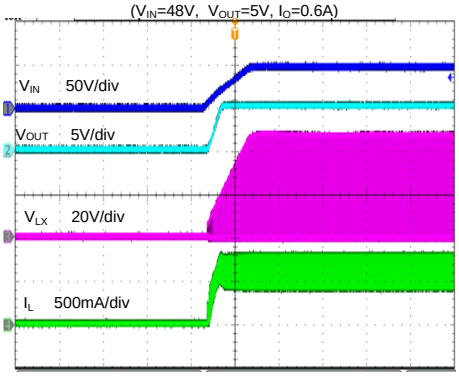
($V_{IN}$=48V, $V_{OUT}$=5V, $I_O$=0.06A-0.6A)




Time (400μs/div)

Startup from $V_{IN}$

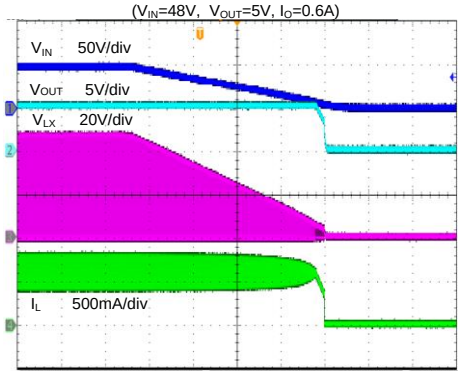
($V_{IN}$=48V, $V_{OUT}$=5V, $I_O$=0.6A)




Time (4ms/div)

Shutdown from $V_{IN}$

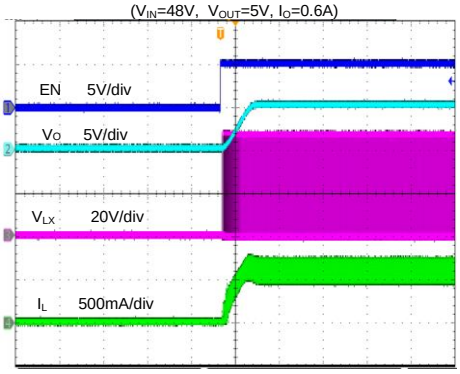
($V_{IN}$=48V, $V_{OUT}$=5V, $I_O$=0.6A)




Time (10ms/div)

Startup from Enable

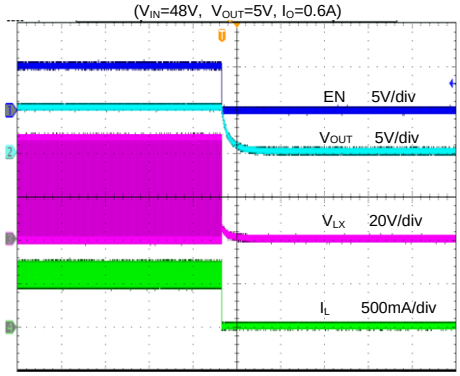
($V_{IN}$=48V, $V_{OUT}$=5V, $I_O$=0.6A)




Time (2ms/div)

Shutdown from Enable

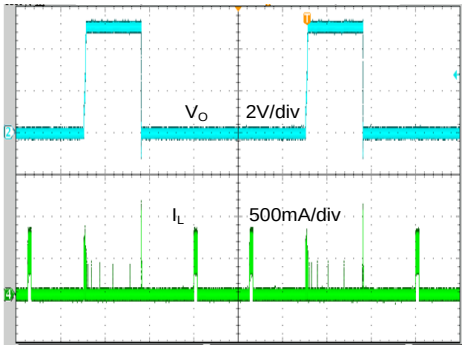
($V_{IN}$=48V, $V_{OUT}$=5V, $I_O$=0.6A)




Time (2ms/div)

Short Circuit Protection

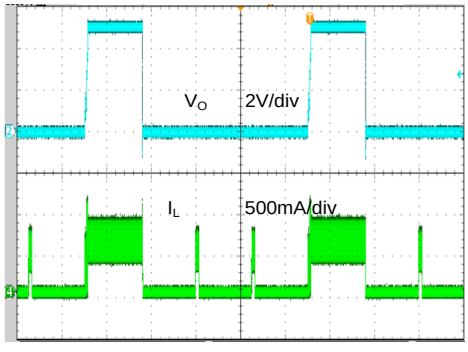
($V_{IN}$=48V, $V_{OUT}$=5V,$I_O$=0A~Short)



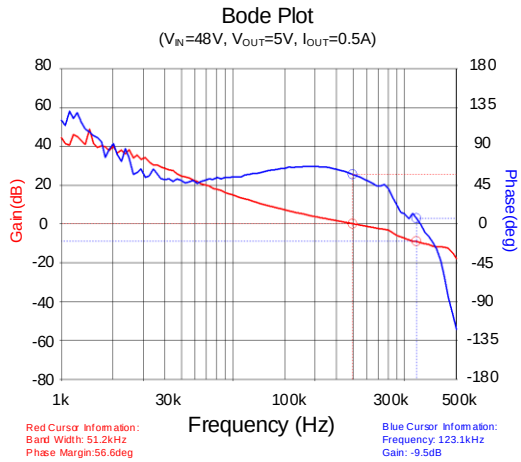

Time (20ms/div)

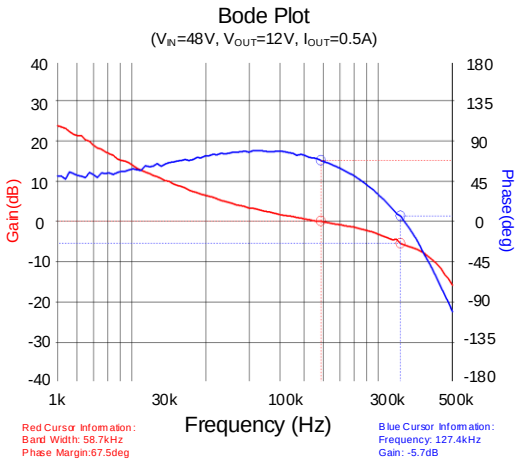
Short Circuit Protection

($V_{IN}$=48V, $V_{OUT}$=5V,$I_O$=0.6A~Short)




Time (20ms/div)



## Detailed Description

The SY21034 high-efficiency asynchronous step-down DC/DC regulator can deliver 2A current over a wide input voltage range from 4.5V to 100V. It integrates a main switch with low $R_{DS(ON)}$ to minimize conduction loss.

The 800kHz switching frequency permits low output-voltage ripple and reduces external inductor and capacitor sizes. The SY21034 also provides cycle-by-cycle current limiting, thermal shutdown, and hiccup short-circuit protection.

The SY21034 uses constant-off-time and peak-current-mode control. When the power FET's current-sense signal reaches internal $V_{COMP}$, the power FET turns off for a fixed period of time (constant $t_{OFF}$). $t_{OFF}$ is internally calculated according to the input voltage, output voltage, and desired switching frequency ($f_{SW}$):

$$t_{OFF} = \frac{1 - V_{OUT}/V_{IN}}{f_{SW}}$$

The power FET turns on after a period of $t_{OFF}$.

**Enable Control**

Pulling the EN pin low (<0.94V) will shut down the device. During shutdown mode, the SY21034 shutdown current will drop below 10μA. Driving the EN pin high (>1.26V) will turn the IC on again.

It is not recommended to connect EN and IN directly. A resistor in the range of 1kΩ to 1MΩ should be used if EN is pulled high by IN.

## Fault-Protection Modes

**Output Current Limit**

With load current increasing, as soon as the FET current exceeds the peak-current-limit threshold, the FET will turn off. If the load current continues to increase, the output voltage will drop.

**Overtemperature Protection (OTP)**

Instant-PWM architecture includes overtemperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds 150°C. Once the junction temperature cools by approximately 15°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the OTP threshold.

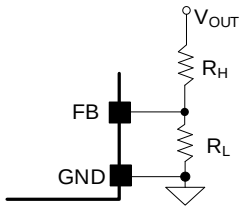
## Application Information

The following paragraphs describe the selection process for the feedback resistors ($R_H$ and $R_L$), input capacitor $C_{IN}$, output capacitor $C_{OUT}$, output inductor L, and rectifier diode D.

**Feedback Resistor-Divider $R_H$ and $R_L$**

Choose $R_H$ and $R_L$ to program the proper output voltage. Choose large resistance values between 10kΩ and 1MΩ for both $R_H$ and $R_L$ to minimize power consumption under light loads. If $V_{OUT}$ is 1.2V, a value of 100kΩ is chosen for $R_H$, then using the following equation, $R_L$ can be calculated as 100kΩ:

$$R_L = \frac{0.6V}{V_{OUT}\text{-}0.6V} R_H$$




**Input Capacitor $C_{IN}$**

For the best performance, select a typical X5R or better grade ceramic capacitor with greater than a 100V rsting and 1μF capacitance. The capacitor should be placed as close as possible to IN pin and the negative end of the rectifier. When selecting an input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating higher than the system requirements. X5R series ceramic capacitors are most often selected due to their small size, low cost, surge-current capability, and high RMS current ratings over a wide temperature and voltage range. However, systems that are powered by a wall adapter or other long and therefore inductive cabling may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum, or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic

capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplicity, use an input capacitor with an RMS current rating greater than 50% of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1-D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. A single 4.7μF X5R capacitor is sufficient in most applications.

**Output Capacitor $C_{OUT}$**

Select the output capacitor $C_{OUT}$ to handle the output ripple requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting the component. For the best performance, use an X5R or better grade ceramic capacitor with capacitance greater than 22μF. The capacitance derating with DC voltage must be considered.

For applications where the design must meet stringent ripple requirements, the following considerations must be followed:

The output voltage ripple at the switching frequency is caused by the inductor current ripple ($\Delta I_L$) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple).

When calculating total ripple, consider both.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

The capacitive ripple might be higher because the effective capacitance for ceramic capacitors decreases with the voltage across the terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

**Output Inductor L**

Consider the following when choosing this inductor:

1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{f_{sw} \times I_{OUT,MAX} \times 0.4}$$

where $f_{SW}$ is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY21034 has high tolerance for ripple current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

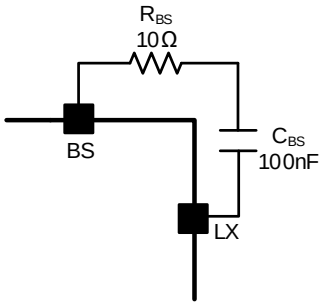
2) The inductor's saturation current rating must be greater than the peak inductor current under full load:

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Choose an inductor with DCR less than 50mΩ to achieve good overall efficiency.

**External Bootstrap Capacitor**

The external bootstrap capacitor provides the gate driver voltage for the internal high-side MOSFET. A 100nF low-ESR ceramic capacitor connected between the BS pin and the LX pin is recommended.

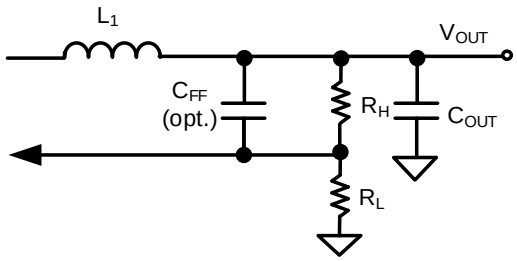



**Rectifier Diode**

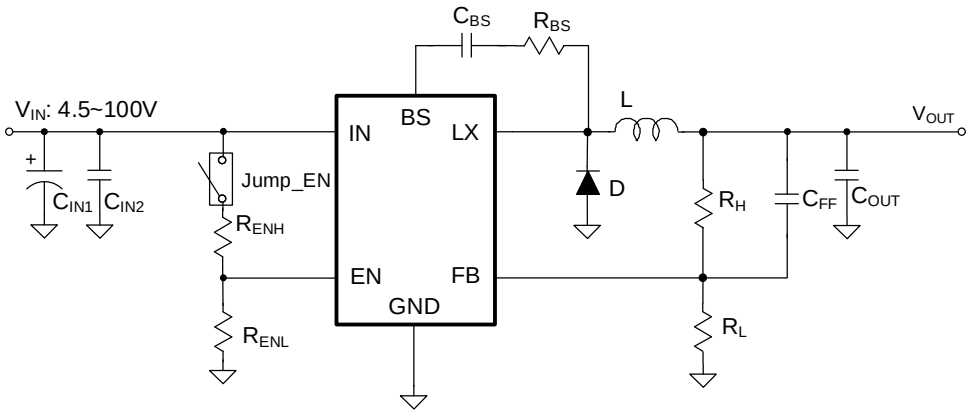
To accommodate the SY21034's high switching speed, choose a Schottky diode with low forward voltage and fast switching speed. The diode's voltage rating must be higher than the SY21034's maximum output voltage, and the diode's average and peak current rating should exceed the SY21034's average output current and peak current.

**Load-Transient Considerations**

The SY21034 integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a 47pF ceramic capacitor in parallel with $R_H$ may further speed up the load-transient responses and is therefore recommended for applications with large load-transient step requirements




## Application Schematic ($V_{OUT}$ = 5V)



## BOM List

| Reference Designator | Description | Part Number | Manufacturer |
|---|---|---|---|
| L | 47µH | CDRH8D43NP-470NC | Sumida |
| $C_{IN1}$ | 22µF/200V (electrolytic capacitor) | | |
| $C_{IN2}$ | 2.2µF/100V, 1206, X7R | GRM31CR72A225KA73L | mµRata |
| $C_{OUT}$ | 22µF/25V, 1206, X5R | C3216X5R1E226M | TDK |
| $C_{FF}$ | 47pF/50V, 0603, C0G | C1608C0G1H470J | TDK |
| $C_{BS}$ | 100nF/50V, 0603, X7R | C1608X7R1H104K | TDK |
| $R_H$ | 100kΩ, 1%, 0603 | | |
| $R_L$ | 13.7kΩ, 1%, 0603 | | |
| $R_{ENH}$ | 10kΩ, 1%, 0603 | | |
| $R_{ENL}$ | 1MΩ, 1%, 0603 | | |
| $R_{BS}$ | 10Ω, 1%, 0603 | | |
| D | 3A/200V | SS320 | |

## Recommended Component Values for Typical Applications

| $V_{OUT}$(V) | $R_H$(kΩ) | $R_L$(kΩ) | $C_{FF}$(pF) | L(Rated/Saturating Current) | $C_{OUT}$ |
|---|---|---|---|---|---|
| 5 | 100 | 13.7 | 47 | 47µH/CDRH8D43NP-470NC | 22µF/25V, 1206, X5R |
| 12 | 100 | 5.23 | 47 | 68µH/CDRH8D43NP-680NC | 22µF/25V, 1206, X5R |

## Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation.

- **Input Capacitors:** Place the input capacitors very close to the IN and GND pins, minimizing the loop formed by these connections. The input capacitor should be connected to the IN and GND pins with a wide copper plane.
- **Output Capacitors:** Guarantee the $C_{OUT}$ negative sides are connected to the GND pin by wide copper traces instead of vias, in order to achieve better accuracy and stability of the output voltage.
- **Feedback Network:** Place the feedback components ($R_H$, $R_L$, and $C_{FF}$) as close to the FB pin as possible. Avoid routing the feedback line near LX or other high-frequency signals, as it is noise-sensitive. Use a Kelvin connection to connect with $C_{OUT}$ rather than the inductor output terminal.
- **LX Connection:** Keep the LX area small to prevent excessive EMI, while providing a wide copper trace to minimize parasitic resistance and inductance.
- **Control Signals:** It is not recommended to connect control signals directly to $V_{IN}$. A resistor in the range of 1kΩ to 1MΩ should be used if the lines are pulled high to $V_{IN}$.
- **GND Vias:** Place an adequate number of vias on the GND layer around the device for better thermal performance. The exposed GND pad should be connected to a copper area larger than its size. Place multiple GND vias on it for heat dissipation.
- **PCB Board:** To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the GND pin. A ground plane is highly recommended if board space allows. Connect the ground pad to a large copper area to enhance thermal performance.

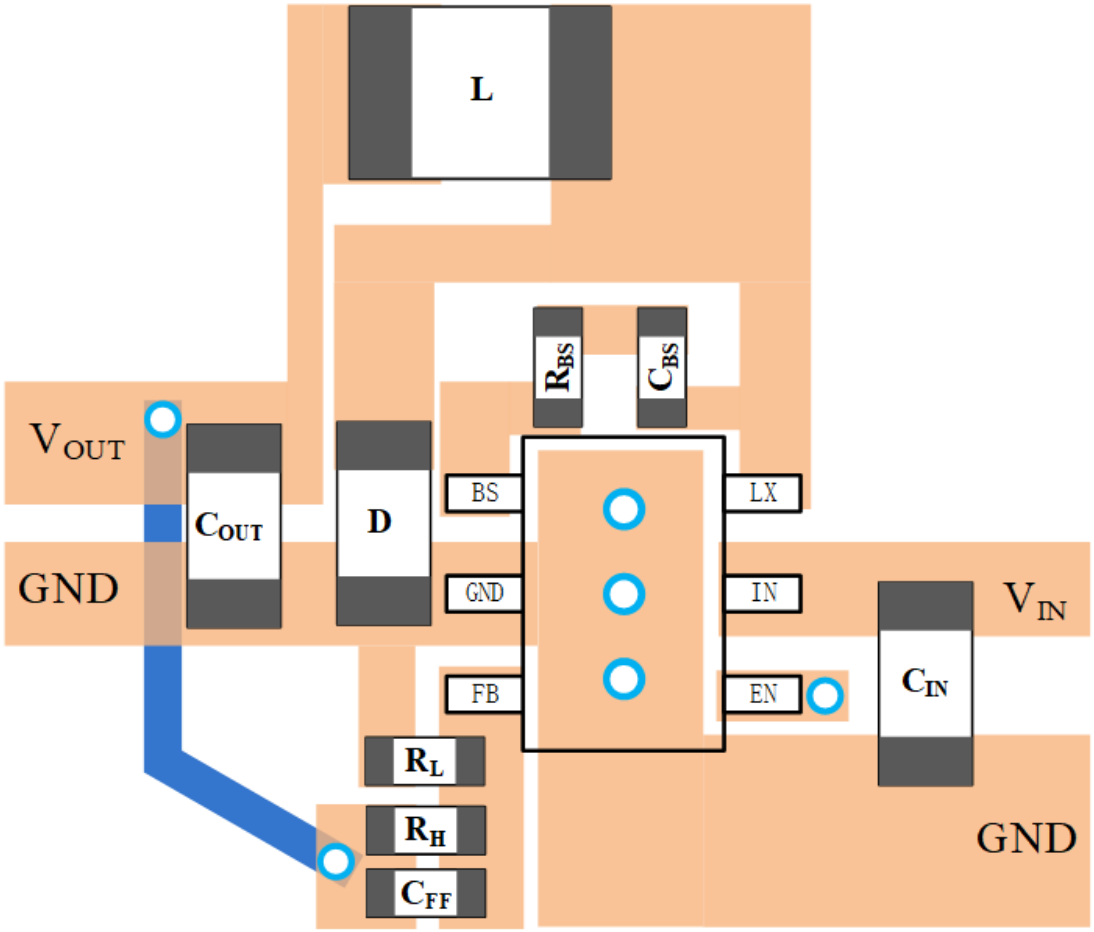
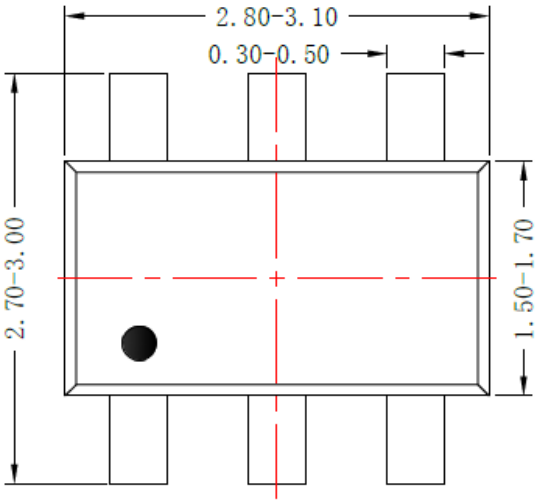
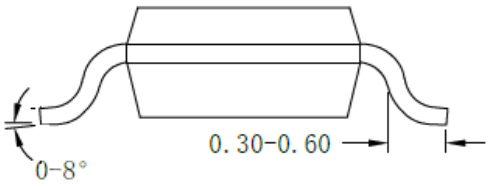



*Figure 4. Suggested PCB Layout*

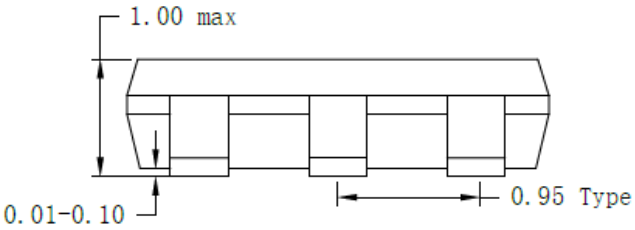
# TSOT23-6 Package Outline and PCB Layout



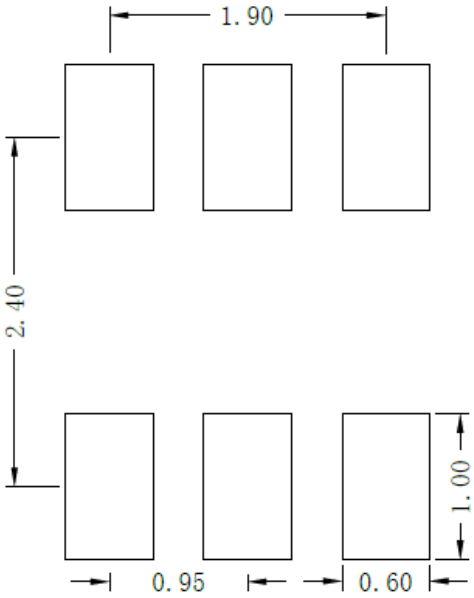

**Top view**




**Side view**




**Front view**

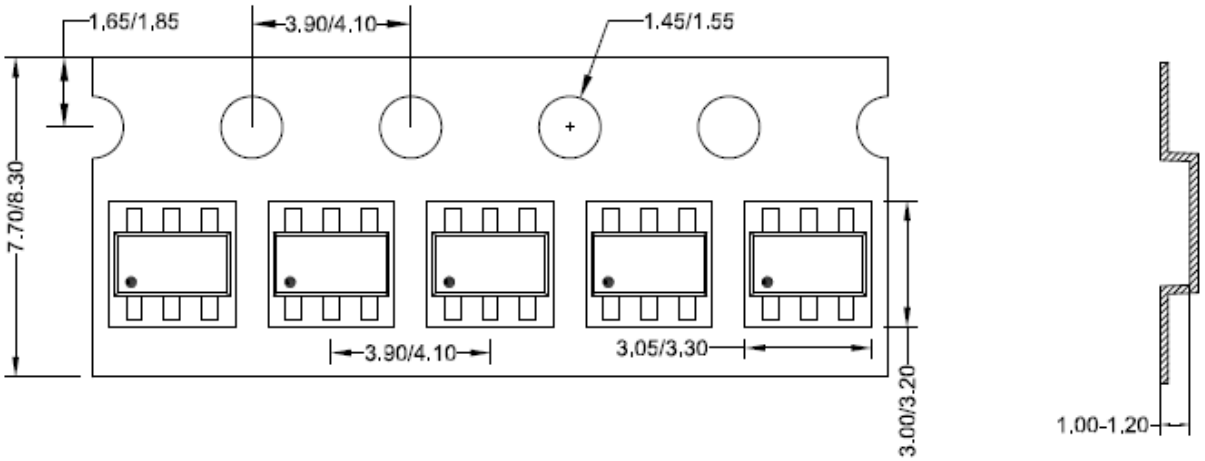



**Recommended pad layout (reference only)**

***Note:*** *All dimensions are in millimeters and exclude mold flash and metal burr.*

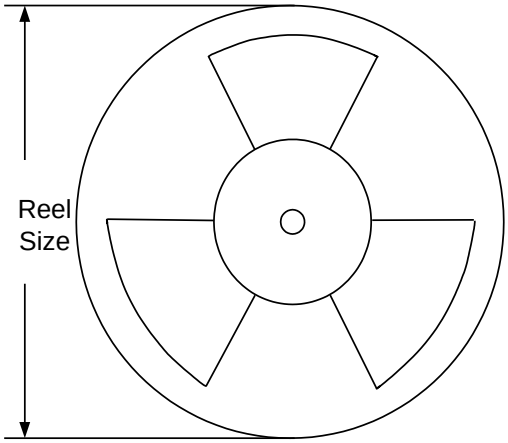
# Taping and Reel Specification

## TSOT23-6 taping orientation




**Feeding direction** ⟶

## Carrier tape and reel specification for packages




| Package types | Tape width (mm) | Pocket pitch(mm) | Reel size (Inch) | Trailer length(mm) | Leader length (mm) | Qty per reel |
|---|---|---|---|---|---|---|
| TSOT23-6 | 8 | 4 | 7" | 280 | 160 | 3000 |

Others: NA

# Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

| Date | Revision | Change |
|---|---|---|
| Aug.31, 2023 | Revision 1.0 | Language improvements for clarity. |
| Nov.14, 2022 | Revision 0.9E | Updated the lead width of package (Page 8) |
| Jan.18, 2022 | Revision 0.9D | 1. The Absolute Maximum Ratings of the FB pin changed from (-0.3V to $V_{IN}$+0.3V) to (-0.3V to 24V). (Page 3)<br>2. Update the test conditions of FB Input Current in EC table. |
| Jun.10, 2021 | Revision 0.9C | Update the test conditions for the EC table:<br>$V_{IN}$ changed from 20V to 48V |
| Jul. 03, 2020 | Revision 0.9B | Add a 10Ω resistor in series with the ceramic capacitor between the BS and the LX pin. |
| Feb. 20, 2019 | Revision 0.9A | Max. value of shutdown current changed from 14μA to 20μA in EC table (Page3) |
| Jul. 13, 2018 | Revision 0.9 | Initial Release |

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