SY21036

High-Efficiency, 40V Input, 1A Synchronous Step-Down Regulator

General Description

The SY21036 high-efficiency synchronous step-down DC/DC converter operates using a clock-control and peak-current-mode control architecture and can deliver 1A load current over a wide input voltage range from 4.5V to 40V. It integrates a main switch and a synchronous switch with low $R_{DS(ON)}$ to minimize the conduction loss and features very low quiescent current to achieve high efficiency under light load.

The 2MHz switching frequency permits low output-voltage ripple and reduces external inductor and capacitor sizes. The SY21036 also provides thermal shutdown, hiccup short-circuit protection, and internal soft-start to limit inrush current during power-on.

The SY21036 is available in a compact SOT23-6 package.

Features

- 4.5 to 40V Input Voltage Range
- 1A Output Current Capability
- Low $R_{DS(ON)}$ for Internal Switches: 380mΩ Top, 180mΩ Bottom
- 2MHz Fixed Switching Frequency
- 0.8V ±1.0% Reference Voltage
- Low Quiescent Current
- Internal Soft-Start Limits Inrush Current
- Hiccup Mode Short-Circuit Protection
- Thermal Shutdown and Auto-Recovery
- Compact Package: SOT23-6

Applications

- LCD-TV
- Set-Top Box
- Notebook
- Storage
- High-Power AP Router
- Networking

Typical Applications

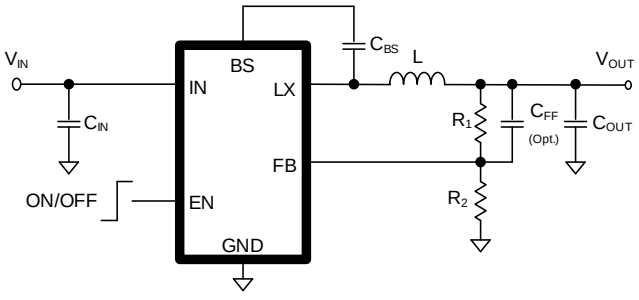


Figure 1. Schematic Diagram

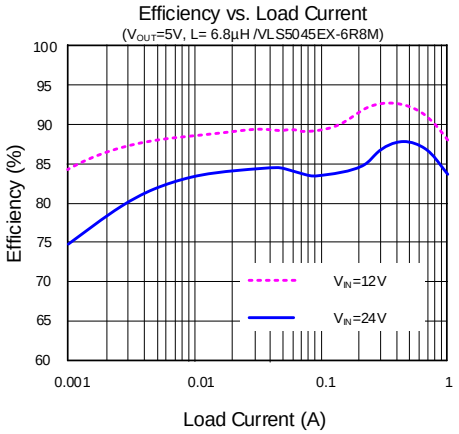


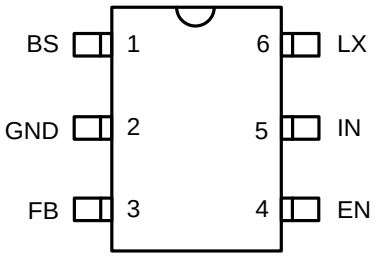
Figure 2. Efficiency vs. Load Current

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY21036ABC	SOT23-6 RoHS-Compliant and Halogen-Free	**lu*xyz***

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	BS	Bootstrap pin. Supply for the high-side gate driver. Connect a 0.1μF ceramic capacitor between the BS and the LX pin .
2	GND	Ground pin.
3	FB	Output feedback pin. Connect this pin to the center point of the output resistor-divider (as shown in Figure 1) to program the output voltage: $V_{OUT} = 0.8 \times (1 + R1/R2)$
4	EN	Enable control pin. Pull this pin high to turn on the IC. Do not leave floating.
5	IN	Input pin. Decouple this pin to the GND pin with at least a 1μF ceramic capacitor.
6	LX	Inductor pin. Connect this pin to the switching node of the inductor.

Block Diagram

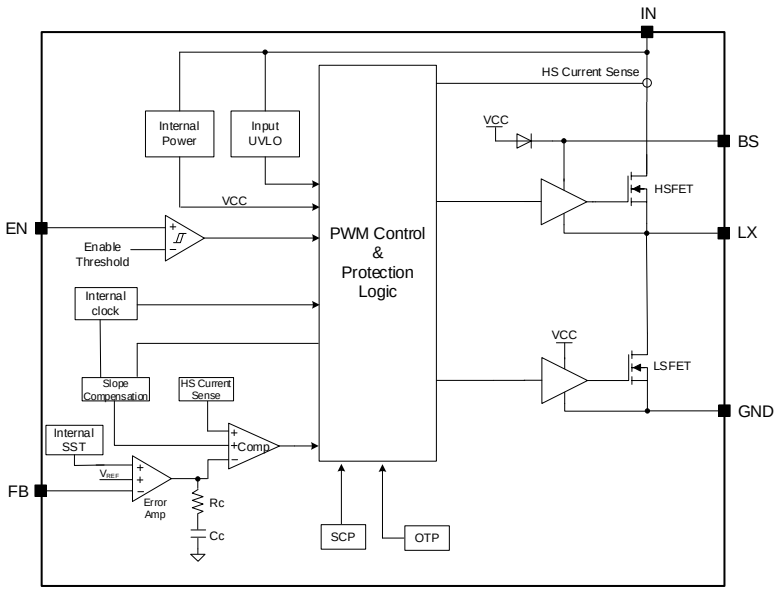


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN	-0.3	40	V
LX, FB, EN	-0.3	40	
BS-LX	-0.3	4	
Dynamic LX Voltage in 10ns Duration	GND - 5	IN + 3	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10sec)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Max	Unit
θ_{JA} Junction-to-ambient Thermal Resistance	100	°C/W
θ_{JC} Junction-to-case Thermal Resistance	30	
P_D Power Dissipation T_A = 25°C	0.4	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	4.5	40	V
Junction Temperature, Operating	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, I_{OUT} = 1A, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Input Voltage Range	V_{IN}		4.5		40	V
	Input UVLO Threshold	V_{UVLO_R}		3.6	4	4.4	V
	Input UVLO Hysteresis	V_{HYS}			0.6		V
	Quiescent Current	I_Q	I_{OUT} = 0,V_{FB} = V_{REF} × 105%	12	22	28	μA
	Shutdown Current	I_{SHDN}	EN = 0		1	2	μA
Output	Feedback Reference Voltage	V_{REF}		0.792	0.8	0.808	V
	FB Input Current	I_{FB}	V_{FB} = 3.3V	-50		50	nA
	Output UVP Threshold	V_{UVP}			50		% V_{REF}
	Output UVP Wait Time	t_{WAIT}			60		μs
	Soft-Start Time	t_{SS}			1		ms
MOSFET	Top FET R_{ON}	$R_{DS(ON),TOP}$			380		mΩ
	Top FET Peak Current Limit	$I_{LIM,TOP}$		1.6		2.5	A
	Bottom FET R_{ON}	$R_{DS(ON),BOT}$			180		mΩ
Enable(EN)	EN Rising Threshold	V_{ENH}		1.4			V
	EN Falling Threshold	V_{ENL}				1	V
Frequency	Switching Frequency	f_{SW}		1.6	2	2.4	MHz
	Min On-Time	t_{ON}			80		ns
	Min Off-Time	t_{OFF}			100		ns
OTP	Thermal Shutdown Temperature	T_{SD}			150		°C
	Thermal Shutdown Hysteresis	T_{HYS}			15		°C

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

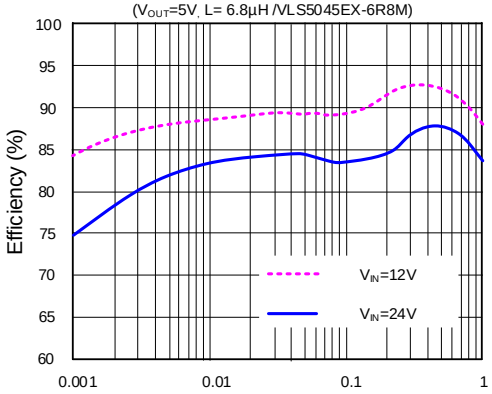
Note 2: Package thermal resistance is measured in the natural convection at T_A = 25°C on a two-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

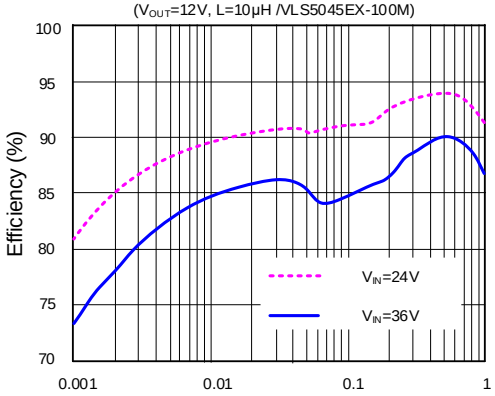
Typical Performance Characteristics

(T_A = 25℃, V_{IN} = 12V, V_{OUT} = 5V, L = 6.8µH, C_{OUT} = 22µF, unless otherwise noted)

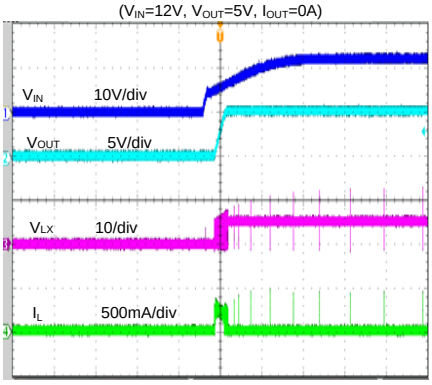
Efficiency vs. Load Current
(V_{OUT}=5V, L= 6.8µH /VLS5045EX-6R8M)



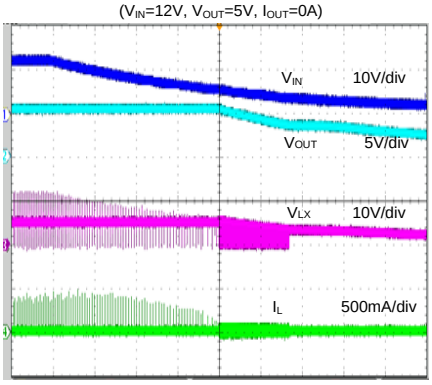
Efficiency vs. Load Current
(V_{OUT}=12V, L=10µH /VLS5045EX-100M)



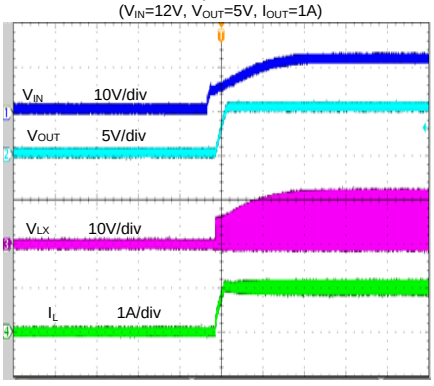
Startup from V_{IN}
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0A)



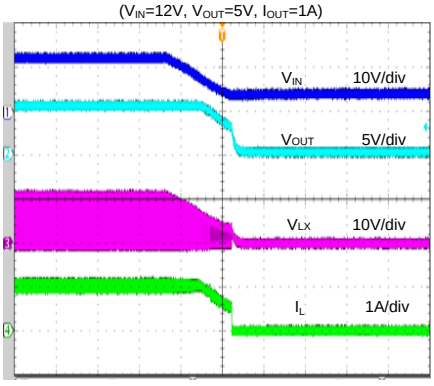
Shutdown from V_{IN}
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0A)



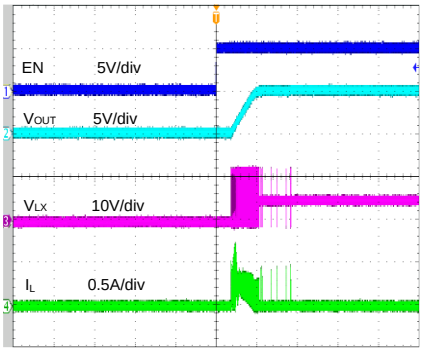
Startup from V_{IN}
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=1A)



Shutdown from V_{IN}
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=1A)

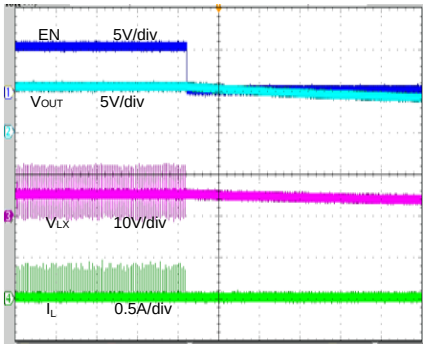


Startup from Enable
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0A)



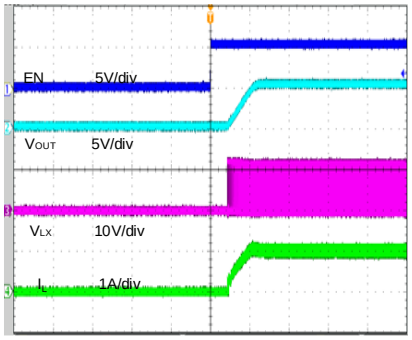
Time (800µs/div)

Shutdown from Enable
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0A)



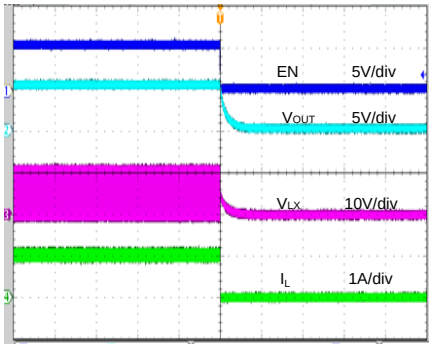
Time (100ms/div)

Startup from Enable
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=1A)



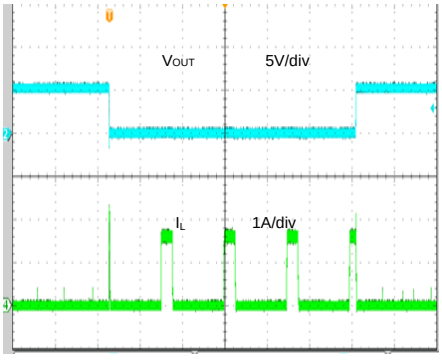
Time (800µs/div)

Shutdown from Enable
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=1A)



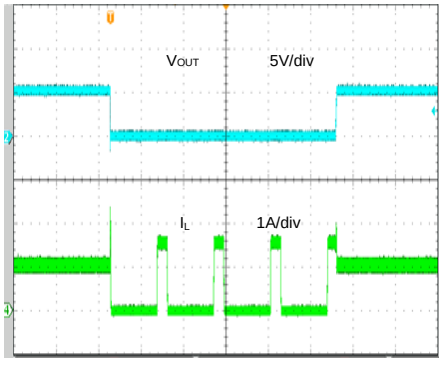
Time (800µs/div)

Short Circuit Protection
(V_{IN}=12V, V_{OUT}=5V, 0A to Short)



Time (4ms/div)

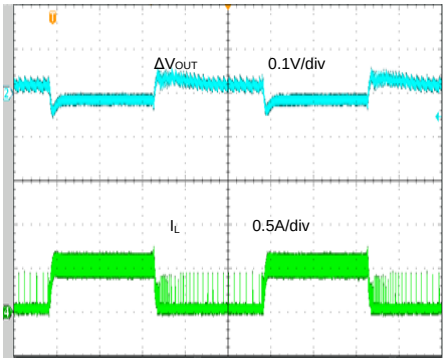
Short Circuit Protection
(V_{IN}=12V, V_{OUT}=5V, 1A to Short)



Time (4ms/div)

Load Transient

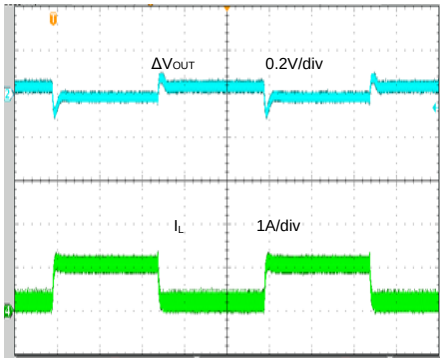
(V_{IN}=12V, V_{OUT}=5V, 0A to 0.5A)



Time (200µs/div)

Load Transient

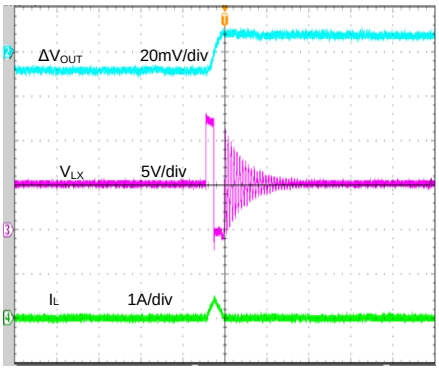
(V_{IN}=12V, V_{OUT}=5V, 0.1A to 1A)



Time (200µs/div)

Output Ripple

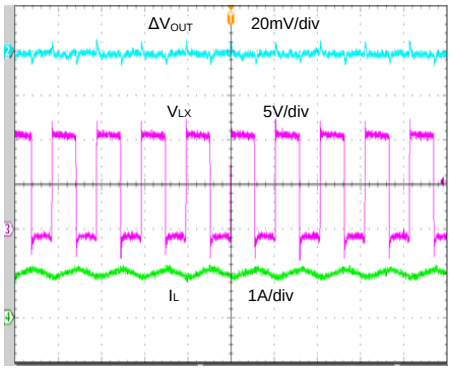
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0A)



Time (2µs/div)

Output Ripple

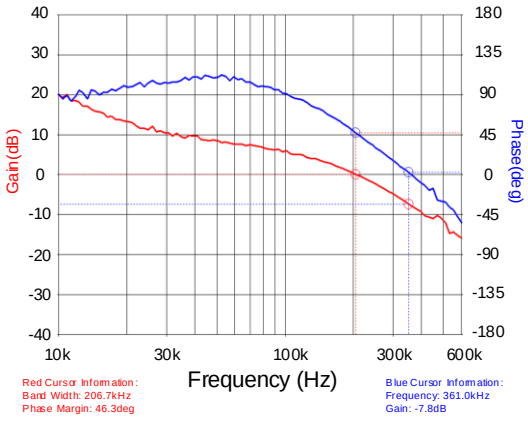
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}= 1A)



Time (400ns/div)

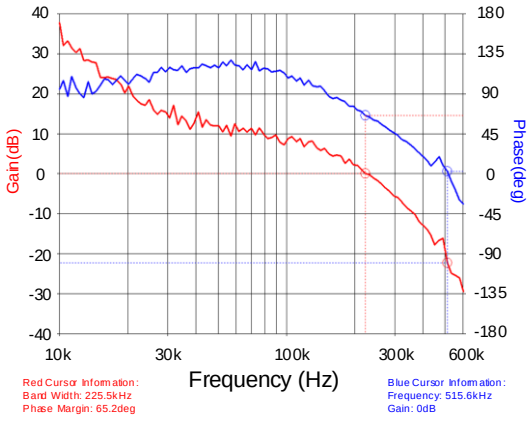
Bode Plot

(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=1A)



Bode Plot

(V_{IN}=24V, V_{OUT}=12V, I_{OUT}=1A)



Detailed Description

The SY21036 high-efficiency synchronous step-down DC/DC can deliver 1A load current over a wide input voltage range from 4.5V to 40V. It integrates a main switch and synchronous switch with low $R_{DS(ON)}$ to minimize conduction loss and features very low quiescent current to achieve high efficiency under light load.

The 2MHz switching frequency permits low output-voltage ripple and reduces external inductor and capacitor sizes. The SY21036 also provides thermal shutdown, hiccup short-circuit protection, and internal soft-start to limit inrush current during power-on.

Fixed Frequency and Peak Current Control

The SY21036 uses a fixed frequency and peak current mode control strategy. The feedback voltage is compared with the internal reference to produce compensation voltage V_{COMP}. The top MOSFET turns on the rising edge of the clock. When the top MOSFET's current sense signal V_{CS} reaches V_{COMP}, it turns off and the bottom MOSFET turns on until a new clock cycle starts. Internal slope compensation is used to avoid sub-harmonic oscillation when the duty cycle is larger than 50%.

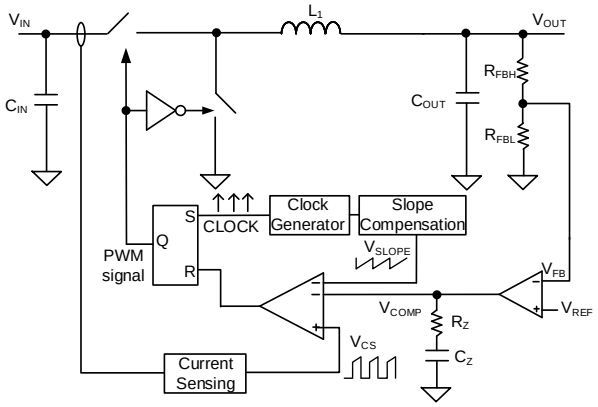


Figure 4. Loop Control Architecture

Minimum Duty Cycle and Maximum Duty Cycle

There is no minimum duty cycle limitation. Because the switching frequency is fixed at 2MHz, the on-time will be limited to the minimum on-time.

The SY21036 can support approximately 90% maximum duty cycle operation when T_J = -40–125°C and f_{SW} = 2MHz.

Input Undervoltage Lockout (UVLO)

To prevent operation before all internal circuitry is ready, and to ensure that the power and synchronous rectifier switches work reliably, the device incorporates input undervoltage lockout protection. The SY21036 remains in a low-current state and all switching actions are inhibited until V_{IN} exceeds the UVLO (rising) threshold. At that time, if EN is enabled, the device will start up by initiating a soft-start ramp. If V_{IN} falls below V_{UVLO} by less than the input UVLO hysteresis, switching actions will again be suppressed.

If required, increasing the default input UVLO threshold is possible by connecting a resistor-divider to the EN pin as shown in Figure 5.

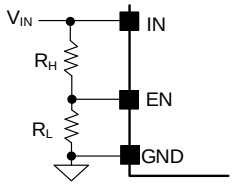


Figure 5. UVLO Adjustment

Enable Control

The EN input is a high-voltage-capable input with logic-compatible threshold. When EN is driven above 1.4V, normal device operation is enabled. When driven to less than 1V, the device will shut down.

It is not recommended to connect EN and IN directly. Use a resistor with a value between 10kΩ and 1MΩ if EN is pulled high to V_{IN}.

Startup and Shutdown

The SY21036 incorporates an internal soft-start circuit to smoothly ramp the output to the desired voltage whenever the device is enabled. Internally, the soft-start circuit clamps the output at a low voltage and then allows the output to rise to the desired voltage over approximately 1ms, which avoids high current flow and transients during startup. The startup and shutdown sequences are shown in Figure 6.

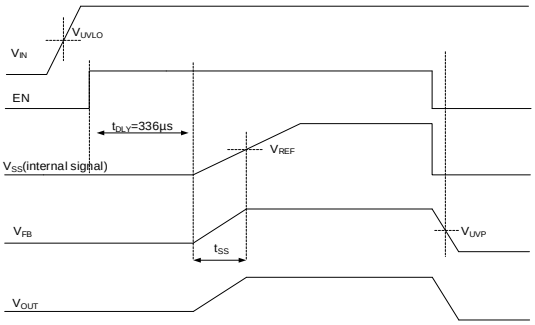


Figure 6. Startup and Shutdown Sequences

External Bootstrap Capacitor Connection

The SY21036 integrates a floating power supply for the gate driver that operates the high-side power switch. Proper operation requires a 0.1µF low-ESR ceramic capacitor connected between the BS and LX pins, as shown in Figure 7.

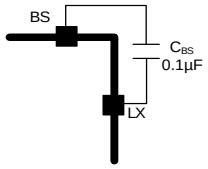


Figure 7. Bootstrap Capacitor Connection

Fault-Protection Modes

Output Current Limit

The SY21036 also incorporates a cycle-by-cycle "peak" current limit (top-FET current limit). The high-side power switch current is monitored during t_{ON} time. If the monitored current exceeds the top-FET current limit, the high-side power switch will be turned off, the low-side synchronous rectifier will be turned on, and t_{ON} will be inhibited.

Output Undervoltage Protection (UVP)

If V_{OUT} is less than approximately 50% of the target output voltage for approximately 60µs (when the output short-circuits or the load current is much higher than the maximum current capacity), the output undervoltage protection (UVP) will be triggered, and the device will enter hiccup protection mode. The hiccup on-time is 1.24ms, and the hiccup off-time is 4.4ms. If the output fault conditions are removed, the device will return to normal operation after the subsequent hiccup off-time, as shown in Figure 8.

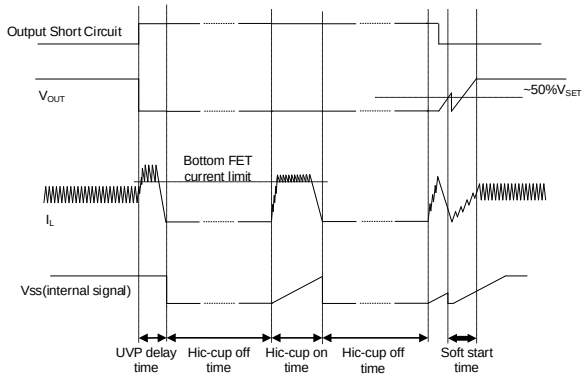


Figure 8. Output Undervoltage Protection

To avoid output overshoot, the internal soft-start circuit voltage V_{SS} will be pulled low temporarily when V_{FB} exceeds the UVP threshold with the output fault conditions removed during hiccup on-time, and then the V_{SS} will rise smoothly to ramp the output to the desired voltage during a new soft-start cycle.

Overtemperature Protection (OTP)

The SY21036 includes overtemperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds 150°C. Once the junction temperature cools by approximately 15°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature will not exceed the OTP threshold.

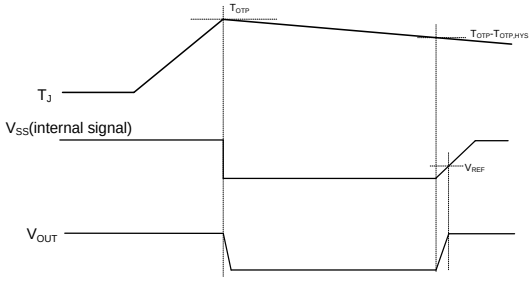


Figure 9. Overtemperature Protection

Application Information

Feedback Resistor-Divider R1 and R2

Choose R1 and R2 to program the proper output voltage. A value between 10kΩ and 1MΩ is recommended for both resistors to minimize power consumption under light loads. For example, if V_{SET} is 5V and R1 = 100kΩ, then R2 can be calculated using the following equation:

$$R_2 = \frac{0.8V}{V_{SET} - 0.8V} \times R_1$$

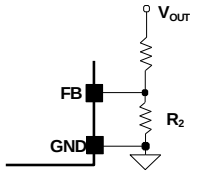


Figure 10. Feedback Resistor Selection

With a calculated value of 19.04kΩ for R2, a standard 1% 19.1kΩ resistor is selected.

Input Capacitor Selection

Input filter capacitors reduce the ripple voltage on the input, filter the switched current drawn from the input supply, and reduce potential EMI. When selecting an input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating higher than the system requirements. X5R series ceramic capacitors are most often selected due to their small size, low cost, surge-current capability, and high RMS current ratings over a wide temperature and voltage range. However, systems that are powered by a wall adapter or other long and therefore inductive cabling may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum, or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1-D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplicity, use an input capacitor with an RMS current rating greater than 50% of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1-D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. A single 10µF X5R capacitor is sufficient in most applications.

Inductor Selection

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage.

This architecture operates well over a wide range of inductor values. This flexibility allows for optimization to find the best trade-off of efficiency, cost, and size for a particular application. Selecting a low inductor value will help reduce size and cost, and enhance transient response, but will increase peak inductor ripple current, reducing efficiency and increasing output voltage ripple. The low DC resistance (DCR) of these low-value inductors may help reduce DC losses and increase efficiency. On the other hand, higher inductor values tend to have higher DCR and will slow transient response.

A reasonable compromise between size, efficiency, and transient response can be determined by selecting a ripple current (ΔI_L) approximately 20–50% of the desired full output load current. Start calculating the approximate inductor value by selecting the input and output voltages, the operating frequency (f_{SW}), the maximum output current ($I_{OUT,MAX}$), and estimated ΔI_L as a percentage of that current:

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Use this inductance value to determine the actual inductor ripple current (ΔI_L) and required peak-current inductor current $I_{L,PEAK}$.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L_1}$$

$$I_{L,PEAK} = I_{OUT,MAX} \times \frac{\Delta I_L}{2}$$

Select an inductor with a saturation current and thermal rating in excess of $I_{L,PEAK}$.

For maximum efficiency, select an inductor with a low DCR that meets the inductance, size, and cost targets. Low-loss ferrite materials should be considered.

Inductor Design Example

Consider a typical design for a device providing $5V_{OUT}$ at 1A from $24V_{IN}$, operating at 2MHz and using target inductor ripple current (ΔI_L) of 40% or 0.4A. First determine the approximate inductance value:

$$L_1 = \frac{5V \times (24V - 5V)}{24V \times 2MHz \times 0.4A} = 4.948\mu H$$

Next, select the nearest standard inductance value (in this case 6.8µH) and calculate the resulting inductor ripple current (ΔI_L):

$$\Delta I_L = \frac{5V \times (24V - 5V)}{24V \times 2MHz \times 6.8\mu H} = 0.291A$$

$$I_{L,PEAK} = 1A + \frac{0.291A}{2} = 1.146A$$

The resulting 0.291A ripple current is approximately 29.1% (0.291A/1A), well within the 20–40% target.

$$I_{L,PEAK,RVS} = \frac{0.291A}{2} = 0.146A$$

Finally, select an available inductor with a saturation current higher than the resulting $I_{L,PEAK}$ of 1.146A.

Output Capacitor Selection

Ceramic and POS types are most often selected due to their small size and low cost. Total capacitance is determined by the transient response and output voltage ripple requirements of the system.

Output Ripple

During steady operation, the output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitors ESR (ESR ripple), as well as the stored charge (capacitive ripple). When considering total ripple, both should be considered.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Consider a typical application with ΔI_L = 0.291A using one 22µF ceramic capacitor, with an ESR of 6mΩ (typ.).

$$V_{RIPPLE,ESR} = 0.291A \times 6m\Omega = 1.74\ mV$$

$$V_{RIPPLE,CAP} = \frac{0.291}{8 \times 22\mu F \times 2MHz} = 0.826mV$$

Total ripple = 2.566mV. The actual capacitive ripple may be higher than the calculated value because the capacitance decreases with the voltage on the capacitor. Using a 150µF 40mΩ POS cap, the result is as follows:

$$V_{RIPPLE,ESR} = 0.291A \times 40m\Omega = 11.64mV$$

$$V_{RIPPLE,CAP} = \frac{0.291A}{8 \times 150\mu F \times 2MHz} = 0.12mV$$

Total ripple = 11.76mV.

Output Transient Undershoot/Overshoot

If very fast load transients must be supported, consider the effect of the output capacitor on the output transient undershoot and overshoot. If the capacitors have low capacitance, this might result in insufficient stored energy for load transients. Output-transient undershoot and overshoot have two causes: voltage changes caused by the ESR of the output capacitor, and voltage changes caused by the output capacitance and inductor current slew rate.

ESR undershoot or overshoot may be calculated as $V_{ESR} = \Delta I_{OUT} \times ESR$. Using the ceramic capacitor example above and a fast load transient of ± 0.5A, V_{ESR} = ±0.5A × 6mΩ = ±3mV. The POS capacitor result with the same load transient is V_{ESR} = ±0.5A × 40mΩ = ±20mV.

Capacitive undershoot (load increasing) is a function of the output capacitance, load step, inductor value, input-output voltage difference, and maximum duty factor. During a fast load transient, the maximum duty factor is a function of t_{ON} and the minimum t_{OFF}. The maximum duty factor D_{MAX} may be calculated as:

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF,MIN}}$$

Given this, the capacitive undershoot may be calculated as:

$$V_{UNDERSHOOT,CAP} = -\frac{L_1 \times \Delta I_{OUT}^2}{2 \times C_{OUT} \times (V_{IN,MIN} \times D_{MAX} - V_{OUT})}$$

Consider a 0.5A load increase using the ceramic capacitor case when V_{IN} = 24V. At V_{OUT} = 5V, the result is t_{ON} = 104ns, $t_{OFF,MIN}$ = 100ns, D_{MAX} = 104 / (104+ 100) = 0.510, and:

$$V_{UNDERSHOOT,CAP} = -\frac{6.8\mu H \times (1A)^2}{2 \times 22\mu F \times (24V \times 0.510 - 5V)} = -21.35mV$$

Using the POS capacitor case, the above result is:

$$V_{UNDERSHOOT,CAP} = -\frac{6.8\mu H \times (1A)^2}{2 \times 150\mu F \times (24V \times 0.510 - 5V)} = -3.13mV$$

Capacitive overshoot (load decreasing) is a function of the output capacitance, inductor value, and output voltage.

$$V_{OVERSHOOT,CAP} = \frac{L_1 \times \Delta I_{OUT}^2}{2 \times C_{OUT} \times V_{OUT}}$$

Consider a 0.5A load decrease using the ceramic capacitor case above. At V_{OUT} = 5V the result is:

$$V_{OVERSHOOT,CAP} = \frac{6.8\mu H \times (0.5A)^2}{2 \times 22\mu F \times 5V} = 7.7mV$$

Using the POS capacitor case, the above result is:

$$V_{OVERSHOOT,CAP} = \frac{6.8\mu H \times (0.5A)^2}{2 \times 150\mu F \times 5V} = 1.13mV$$

Combine the ESR and capacitive undershoot and overshoot to calculate the expected total overshoot and undershoot for a given application.

Load-Transient Considerations

The SY21036 uses the Instant-PWM™ architecture to achieve good stability and fast transient responses. In applications with high step load current, adding an RC feed-forward compensation network R_{FF} and C_{FF} may further speed up the load-transient responses. R_{FF} = 1kΩ and C_{FF} = 68pF have been shown to perform well in most applications. Increasing C_{FF} will speed up the load-transient response if there is no stability issue.

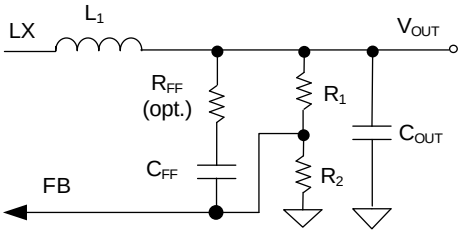


Figure 11. Feed-Forward Network

Note that when C_{OUT} > 500µF and minimum load current is low, using the feed-forward values R_{FF} = 1kΩ and C_{FF} = 2.2nF is recommended to provide sufficient ripple to the FB node for reliable operation.

Thermal Design Considerations

The maximum power dissipation depends on multiple factors: PCB layout, IC package thermal resistance, local airflow, and the junction temperature relative to ambient. The maximum power dissipation may be calculated as:

$$P_{D,MAX} = \frac{(T_{J,MAX} - T_A)}{\theta_{JA}}$$

Where, $T_{J,MAX}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

To comply with the recommended operating conditions, the maximum junction temperature is 125℃. The junction to ambient thermal resistance θ_{JA} is layout dependent. For the SOT23-6 package the thermal resistance θ_{JA} is 100°C /W when measured on a standard Silergy four-layer thermal test board. These standard thermal test layouts have a very large area with long 2-oz. copper traces connected to each IC pin and very large, unbroken 1-oz. internal power and ground planes.

To meet the performance of the standard thermal test board in a typical tiny evaluation board area, wide copper traces are required well-connected to the IC's backside pads leading to exposed copper areas on the component side of the board as well as good thermal via from the exposed pad connecting to a wide middle-layer ground plane, and perhaps, to an exposed copper area on the board's solder side.

The maximum power dissipation at T_A = 25°C may be calculated using the following formula:

$$P_{D,MAX} = \frac{(125°C - 25°C)}{(100°C / W)} = 1W$$

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J,MAX}$ and thermal resistance θ_{JA}. Use the derating curve in Figure 12 below to calculate the effect of rising ambient temperature on the maximum power dissipation.

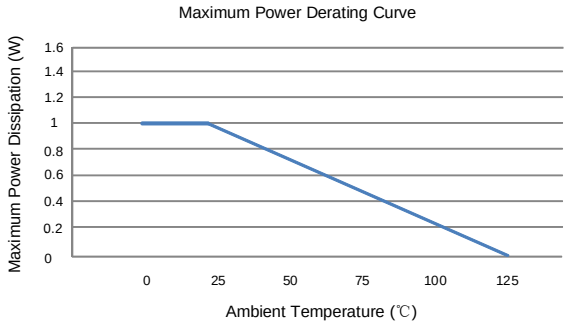
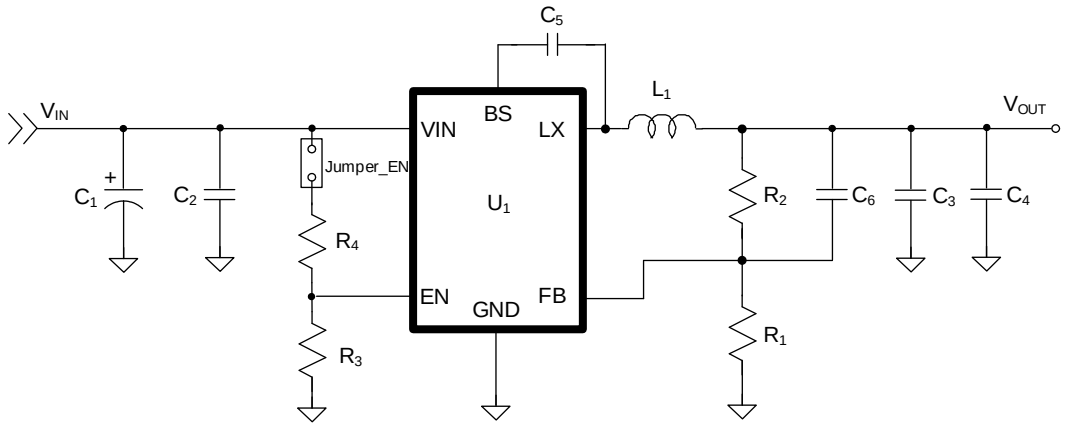


Figure 12. Maximum Power Dissipation

Application Schematic (V_{OUT} = 5V)



BOM List

Reference Designator	Description	Part Number	Manufacturer
U_1		SY21036ABC	Silergy
C_1	47µF/50V Electrolytic Cap		
C_2	10µF/50V/X5R, 1206	GRM31CR61H106KA12L	Mµrata
C_3	22µF/16V/X5R, 1206	GRM31CR61C226ME15L	Mµrata
C_4	NC		
C_5	0.1µF/50V/X7R, 0603	GRM188R71H104KA93D	Mµrata
C_6	68pF/50V/C0G, 0603	C1608C0G1H680J	TDK
L_1	6.8µH, inductor	VLS5045EX-6R8M	TDK
R_1	19.1kΩ, 1%, 0603		
R_2	100kΩ, 1%, 0603		
R_3	1MΩ, 1%, 0603		
R_4	10kΩ, 1%, 0603		

Recommended Components for Typical Applications

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C13 (pF)	L1/Part Number
1.2	200	100	22	1.5µH /VLP4045LT-1R5N
1.8	80.6	100	47	2.2µH /VLS5045EX-2R2N
3.3	32.4	100	47	4.7µH /VLS5045EX-4R7M
5	19.1	100	68	6.8µH /VLS5045EX-6R8M
12	7.14	100	100	10µH /VLS5045EX-100M

Layout Design

To achieve optimal design, follow these PCB layout considerations:

- Place C_{IN}, L, R1, and R2 close to the IC
- To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the GND pin. A ground plane is highly recommended if board space allows.
- Minimize the loop area formed by C_{IN}, IN, LX, and the rectifier.
- To reduce potential noise:
  - Minimize the PCB copper area connected to the LX pin.
  - R1, R2, and the trace connected to the FB pin must not be adjacent to the LX net on the PCB layout.
  - If the system chip interfacing with the EN pin has a high impedance state during shutdown mode, and the IN pin is connected directly to a power source such as a Li-ion battery, add a 1MΩ pulldown resistor between the EN and GND pins to prevent noise from falsely triggering the regulator during shutdown mode.

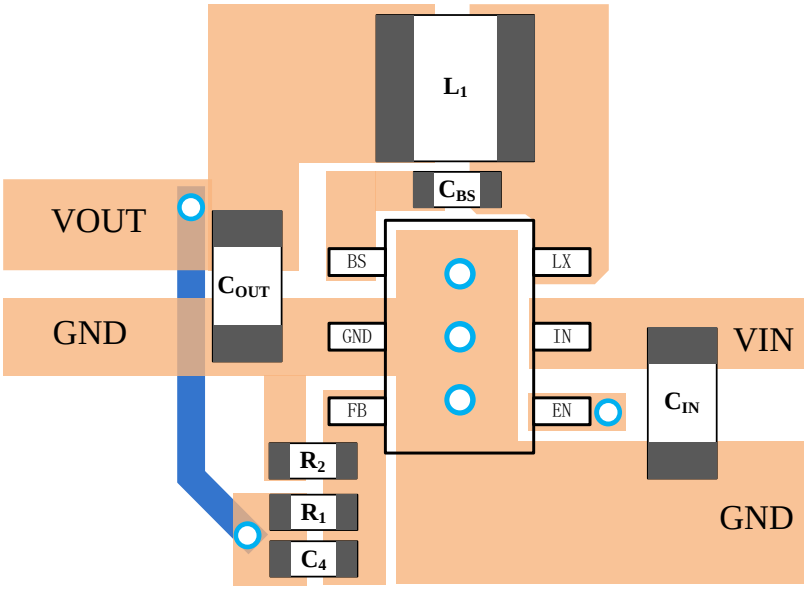
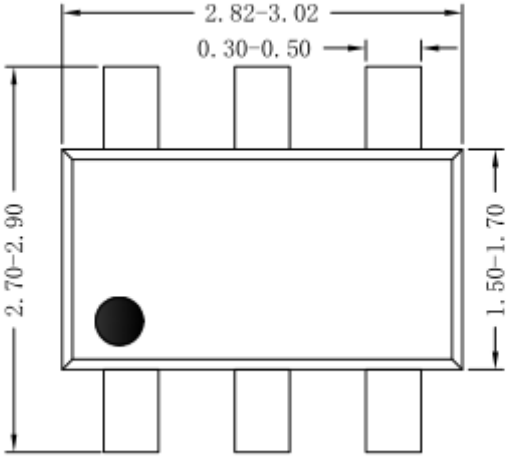
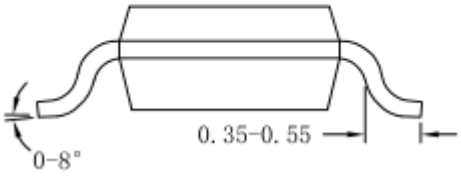


Figure 13. PCB Layout Suggestion

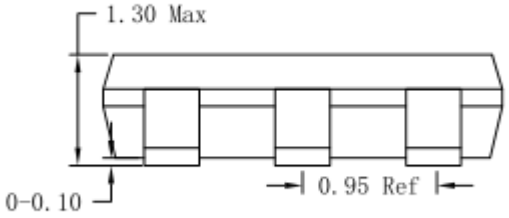
SOT23-6 Package Outline and PCB Layout



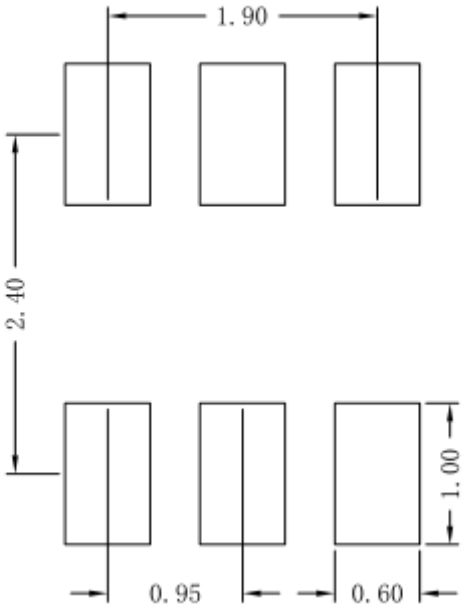
Top view



Side view



Side view

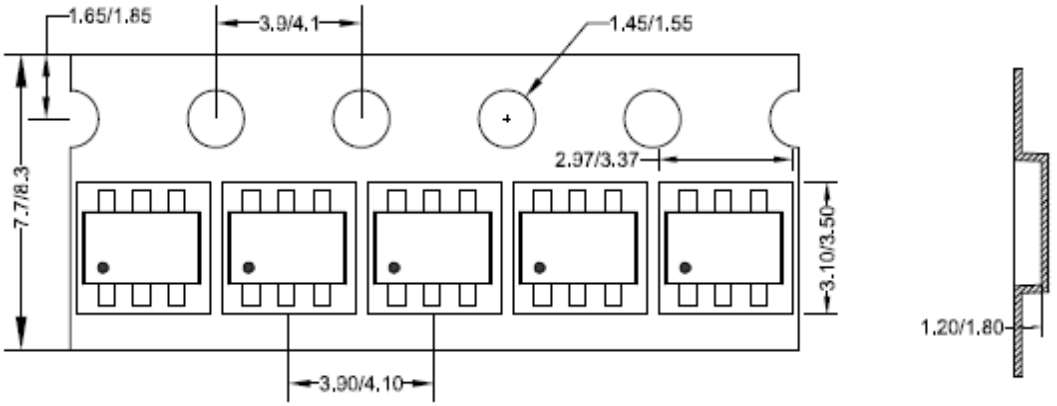


Recommended pad layout (reference only)

Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

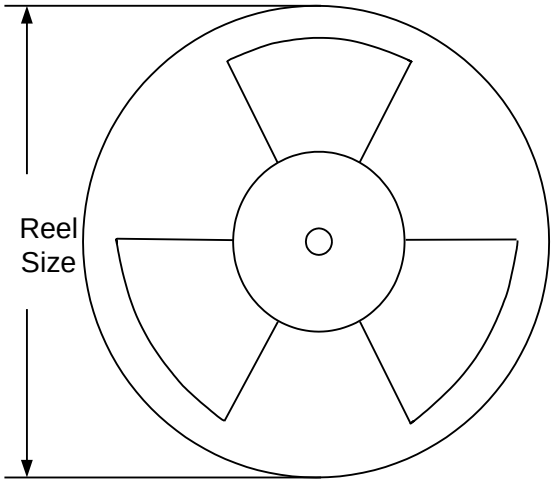
Taping and Reel Specification

SOT23-6 taping orientation



Feeding direction ⟶

Carrier tape and reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-6	**8**	**4**	**7"**	**280**	**160**	**3000**

Others: NA

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Apr.18, 2024	Revision 1.0A	1. The minimum value of Dynam.ic LX Voltage in 10ns Duration changes from IN + 3 to GND – 5 2. The maximum value of Dynamic LX Voltage in 10ns Duration changes from GND – 5 to IN + 3.
Aug.23, 2023	Revision 1.0	Language improvements for clarity.
Jun.08, 2020	Revision 0.9A	Update in the EC table (page 4) 1. The max value of the Input UVLO Threshold changes from 4.2V to 4.4V; 2. The typical value of the Quiescent Current changes from 18μA to 22μA, max value changes from 24μA to 28μA.
Nov.16, 2018	Revision 0.9	Initial Release

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