SY21051

High Efficiency, 1A, 100V Input Synchronous Buck Converter

General Description

The SY21051 high-efficiency synchronous Buck converter can deliver 1A output current over a wide input voltage range from 7V to 100V. The SY21051 employs a constant on-time and ripple-based control strategy to achieve fast transient responses. The SY21051 integrates the top FET and bottom FET with very low $R_{DS(ON)}$ to minimize the conduction loss.

Silergy's constant on-time (COT) ripple-based control method supports high input/output voltage ratios (low duty cycles), and fast transient response while maintaining a near constant operating frequency over line, load, and output voltage ranges. This control method provides stable operation without complex compensation and even with low ESR ceramic capacitors.

The SY21051 also provides cycle-by-cycle current limit, over temperature protection, and output short circuit protection.

The SY21051 is available in a compact SO8E package.

Features

- Low $R_{DS(ON)}$ for Internal MOSFETs: 500mΩ Top, 240mΩ Bottom
- 7V to 100V Input Voltage Range
- Up to 1A Output Current Capability
- Adjustable Switching Frequency
- COT Ripple-Based Control to Achieve Fast Transient Responses
- 2ms Internal Soft-start Limits the Inrush Current
- Precise ±2% 1.2V Reference
- Output Short Circuit Protection
- Cycle-by-Cycle Peak and Valley Current Limit
- Over Temperature Protection
- Output Auto-Discharge Function
- RoHS Compliant and Halogen Free
- Compact Package: SO8E

Applications

- Non-Isolated Telecommunication Buck Regulator
- Secondary High Voltage Post Regulator
- Automotive Systems

Typical Applications

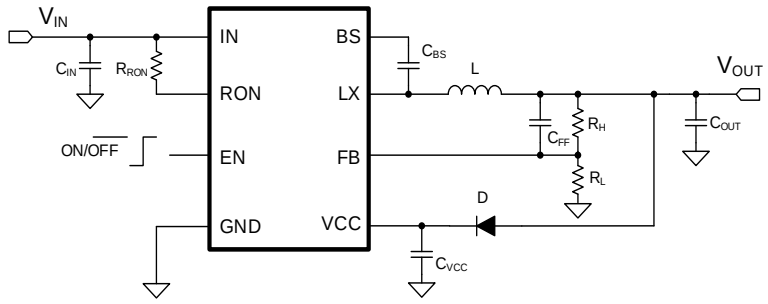


Figure 1.Typical Application Circuit

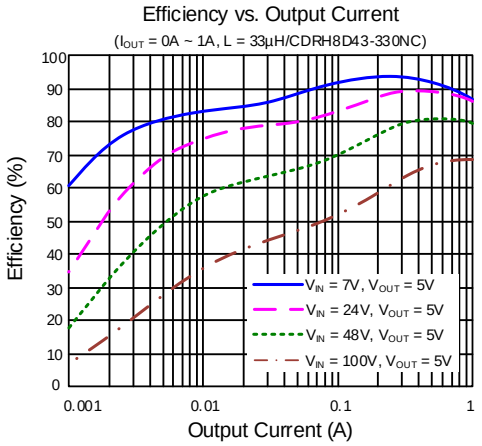


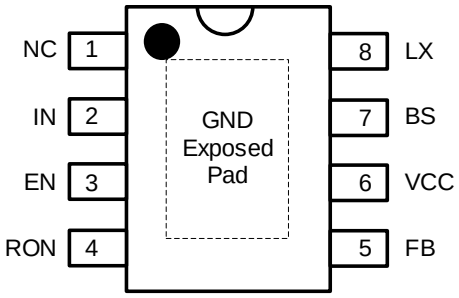
Figure 2. Efficiency vs. Output Current

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY21051FCC	SO8E RoHS Compliant and Halogen Free	**AMAxyz**

x=year code, y=week code, z= lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	NC	Not connected.
2	IN	Input pin. Decouple this pin to GND with at least a 2.2μF ceramic capacitor.
3	EN	Enable control. Pull this pin lower than EN falling threshold to disable the device, pull this pin higher than EN rising threshold to enable the device. Do not leave this pin floating.
4	RON	Connect a resistor from this pin to V_{IN} to program the switching frequency. The switching frequency can be calculated using the following formula: $f_{SW}(kHz)=\frac{11\times V_{OUT}(V)+500}{R_{RON}(M\Omega)}$
5	FB	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=1.2\times(1+R_H/R_L)$.
6	VCC	Supply input of the internal LDO.
7	BS	Bootstrap pin. Supply top FET gate driver. Connect a 0.1μF ceramic capacitor between the BS pin and the LX pin.
8	LX	Inductor pin. Connect this pin to the switching node of the inductor.
Exposed Pad	GND	Ground pin.

Block Diagram

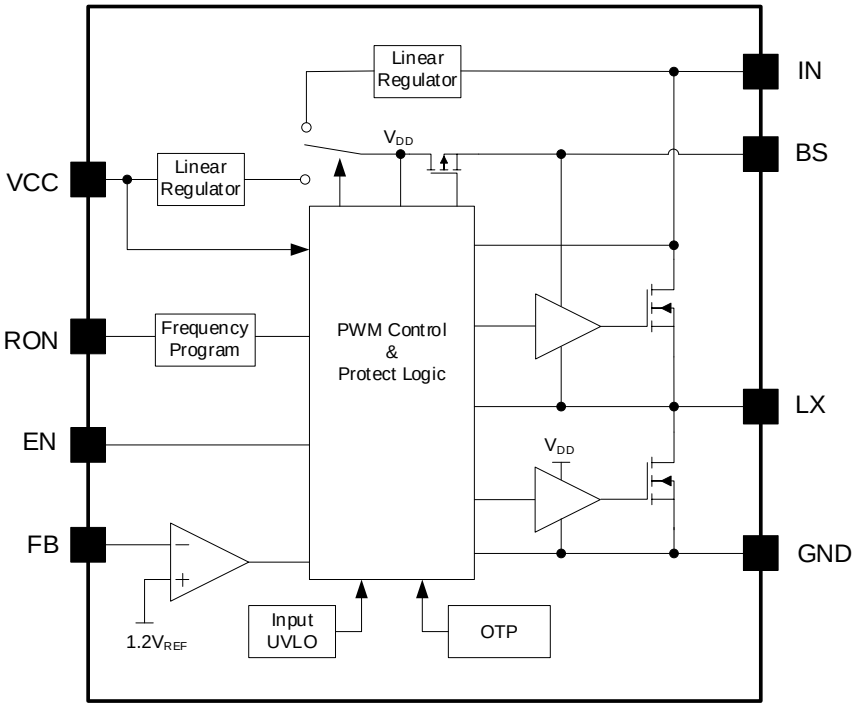


Figure3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN	-0.3	100	V
EN, RON	-0.3	V_{IN} + 0.3	
LX	-0.7	V_{IN} + 0.3	
BS-LX, FB	-0.3	6	
VCC	-0.3	30	
Dynamic LX Voltage in 10ns Duration	V_{GND} - 5	V_{IN} + 3	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering,10s.)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-ambient Thermal Resistance	30	°C/W
θ_{JC} Junction-to-case Thermal Resistance	10	
P_D Power Dissipation T_A=25°C	3.3	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	7	100	V
Output Current		1	A
Junction Temperature	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics

(V_{IN} = 48V, V_{OUT} = 12V, L = 47µH, C_{OUT} = 10µF, T_A = 25°C, I_{OUT} = 1A, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Voltage Range	V_{IN}		7		100	V
	UVLO Threshold	$V_{IN,UVLO}$	V_{IN} rising	6	6.5	7	
	UVLO Hysteresis	$V_{IN,HYS}$			0.5		
	Quiescent Current	I_Q	I_{OUT} = 0A, V_{FB} = V_{REF} × 105%			400	µA
	Shutdown Current	I_{SHDN}	EN = Low		5	10	
Output	Feedback Reference Voltage	V_{REF}		1.176	1.2	1.224	V
	FB Input Current	I_{FB}	V_{FB} = 3.3V	-50		50	nA
MOSFET	Top FET $R_{DS(ON)}$	$R_{DS(ON)1}$			500		mΩ
	Bottom FET $R_{DS(ON)}$	$R_{DS(ON)2}$			240		
	Top FET Current Limit Threshold	$I_{LMT,TOP}$			1.8		A
	Bottom FET Current Limit Threshold	$I_{LMT,BOT}$		1.1			
Enable (EN)	Rising Threshold	$V_{EN,R}$		1.11	1.21	1.31	V
	Falling Threshold	$V_{EN,F}$		1.08	1.18	1.28	
Frequency	Switching Frequency	f_{SW}	$f_{SW}(kHz)=\frac{11\times V_{OUT}(V)+500}{R_{RON}(M\Omega)}$	200		1000	kHz
	Minimum On-time	$t_{ON,MIN}$			120		ns
	Minimum Off-time	$t_{OFF,MIN}$			350		
OTP	Temperature	T_{OTP}	(Note 4)		150		°C
	Temperature Hysteresis	T_{HYS}	(Note 4)		15		

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective 4-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Paddle of SO8E package is the case position for θ_{JC} measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Guaranteed by design.

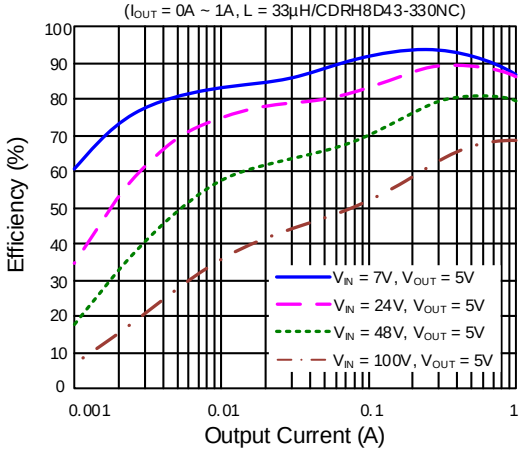
Typical Performance Characteristics

(Condition1：T_A = 25°C, V_{IN} = 48V, V_{OUT} = 5V, L = 33μH, C_{OUT} = 10μF, f_{SW} = 500kHz, unless otherwise noted)

(Condition2：T_A = 25°C, V_{IN} = 48V, V_{OUT} = 12V, L = 47μH, C_{OUT} = 10μF, f_{SW} = 500kHz, unless otherwise noted)

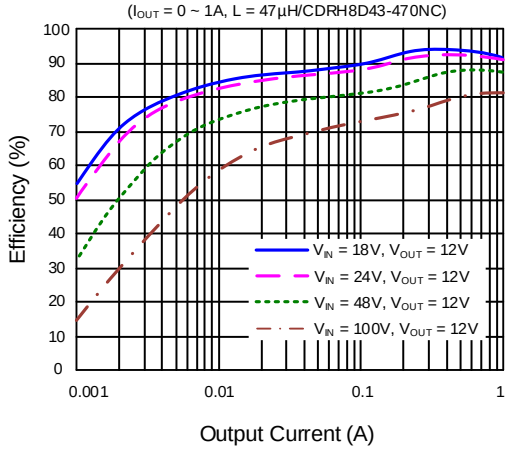
Efficiency vs. Output Current

(I_{OUT} = 0A ~ 1A, L = 33μH/CDRH8D43-330NC)



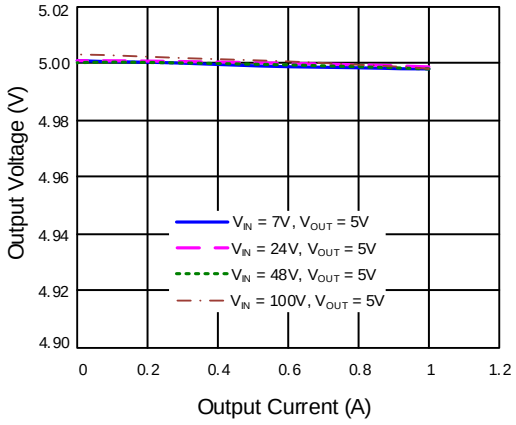
Efficiency vs. Output Current

(I_{OUT} = 0 ~ 1A, L = 47μH/CDRH8D43-470NC)



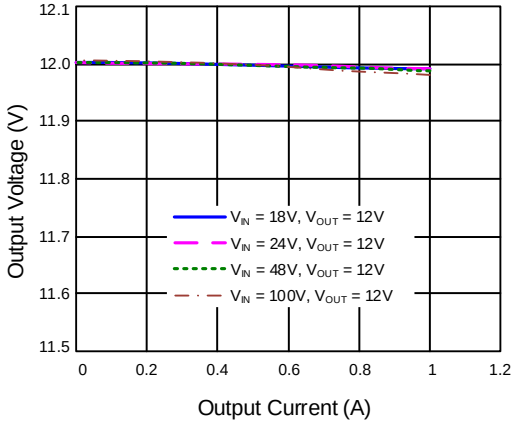
Load Regulation

(I_{OUT} = 0A ~ 1A, L = 33μH/CDRH8D43-330NC)



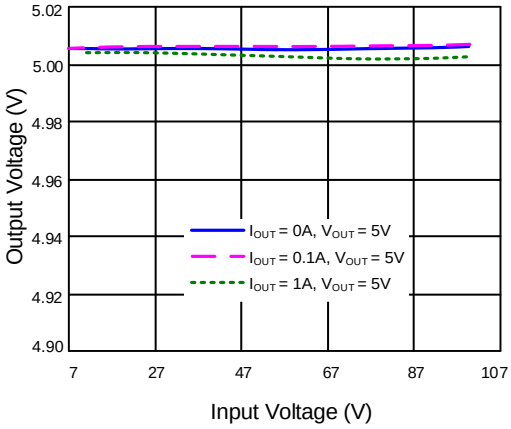
Load Regulation

(I_{OUT} = 0 ~ 1A, L = 47μH/CDRH8D43-470NC)



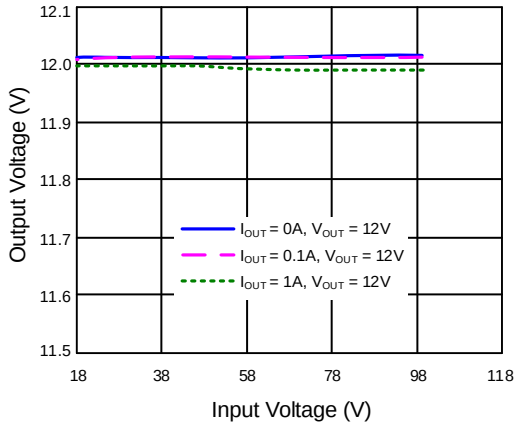
Line Regulation

(I_{OUT} = 0A ~ 1A, L = 33μH/CDRH8D43-330NC)



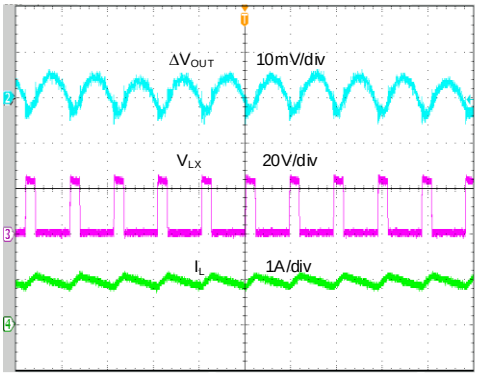
Line Regulation

(I_{OUT} = 0 ~ 1A, L = 47μH/CDRH8D43-470NC)



Output Ripple

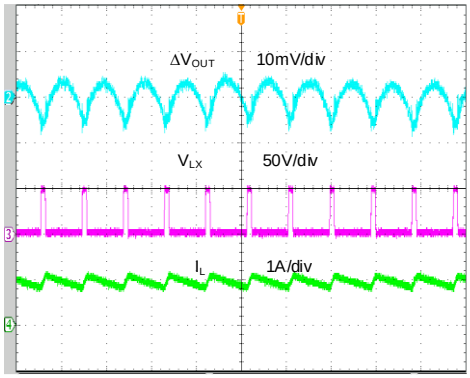
(V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 1A)



Time (2μs/div)

Output Ripple

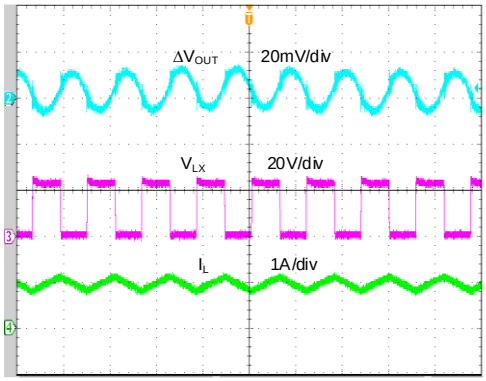
(V_{IN} = 48V, V_{OUT} = 5V, I_{OUT} = 1A)



Time (2μs/div)

Output Ripple

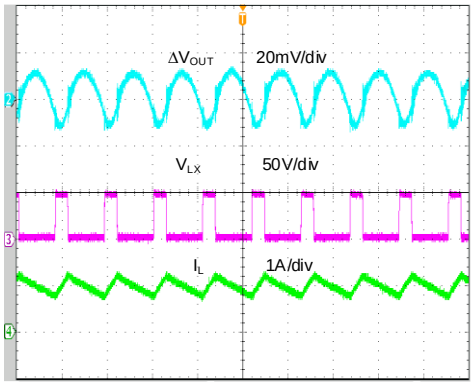
(V_{IN} = 24V, V_{OUT} = 12V, I_{OUT} = 1A)



Time (2μs/div)

Output Ripple

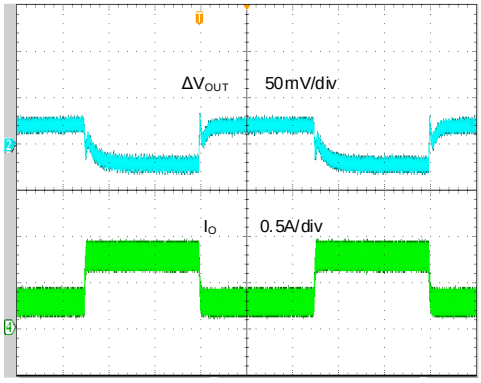
(V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 1A)



Time (2μs/div)

Load Transient

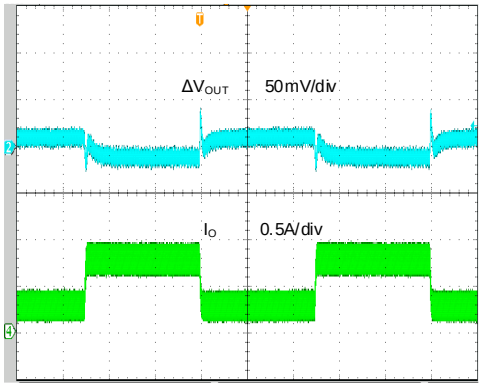
(V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 0.25A ~ 0.75A)



Time (400μs/div)

Load Transient

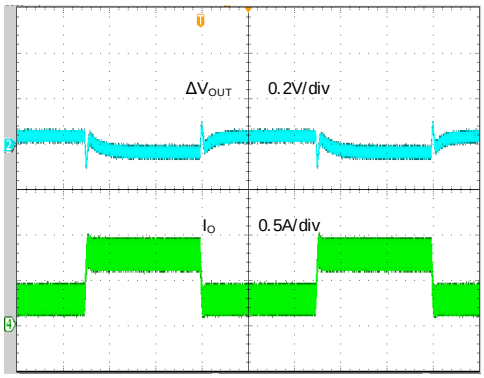
(V_{IN} = 48V, V_{OUT} = 5V, I_{OUT} = 0.25A ~ 0.75A)



Time (400μs/div)

Load Transient

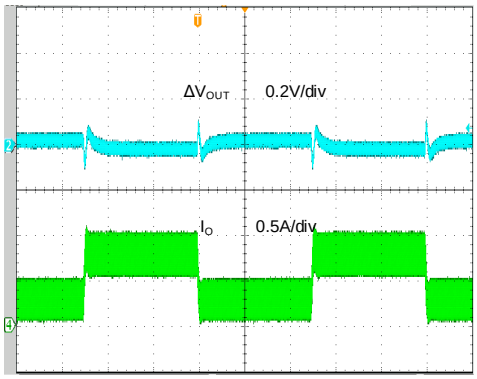
(V_{IN} = 24V, V_{OUT} = 12V, I_{OUT} = 0.25A ~ 0.75A)



Time (400μs/div)

Load Transient

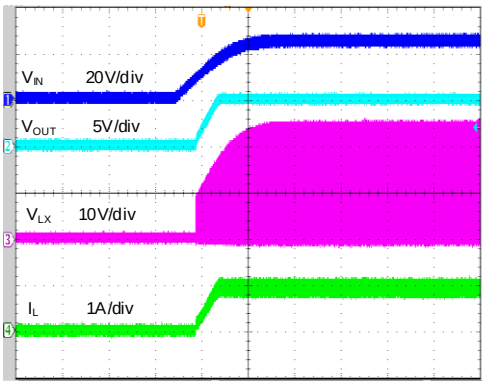
(V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 0.25A~ 0.75A)



Time (400μs/div)

Startup from V_{IN}

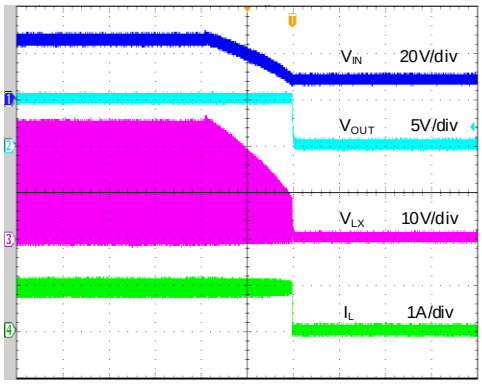
(V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 1A)



Time (4ms/div)

Shutdown from V_{IN}

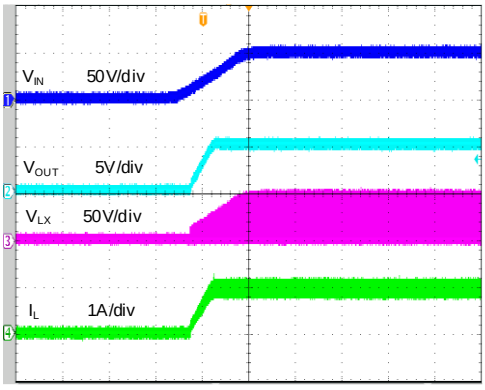
(V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 1A)



Time (4ms/div)

Startup from V_{IN}

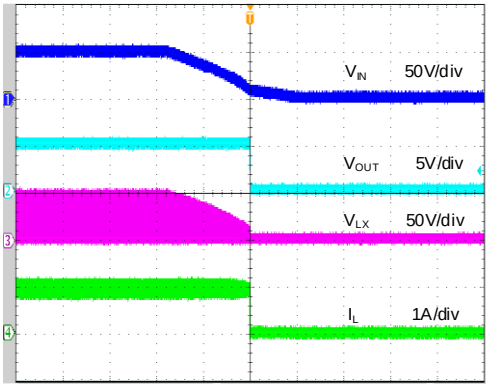
(V_{IN} = 48V, V_{OUT} = 5V, I_{OUT} = 1A)



Time (4ms/div)

Shutdown from V_{IN}

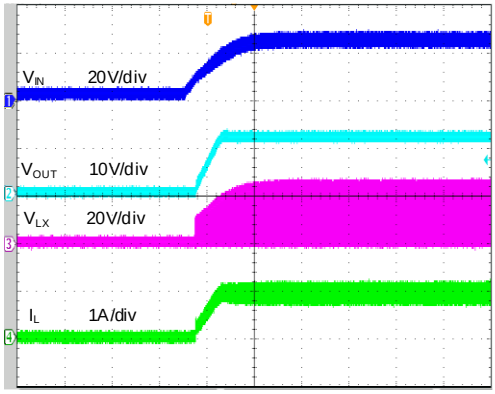
(V_{IN} = 48V, V_{OUT} = 5V, I_{OUT} = 1A)



Time (10ms/div)

Startup from V_{IN}

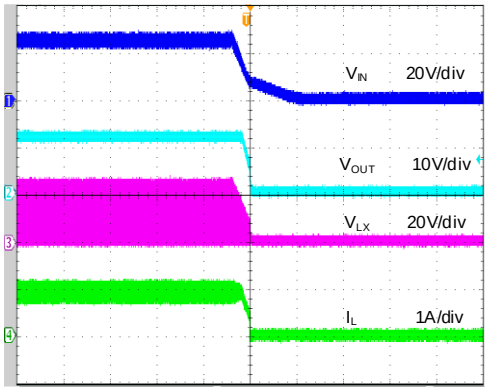
(V_{IN} = 24V, V_{OUT} = 12V, I_{OUT} = 1A)



Time (4ms/div)

Shutdown from V_{IN}

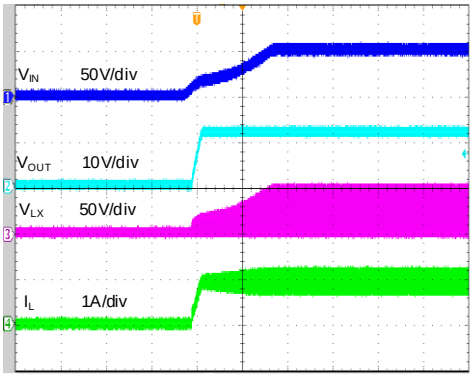
(V_{IN} = 24V, V_{OUT} = 12V, I_{OUT} = 1A)



Time (10ms/div)

Startup from V_{IN}

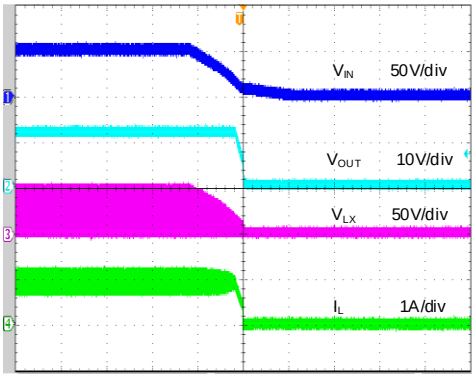
(V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 1A)



Time (10ms/div)

Shutdown from V_{IN}

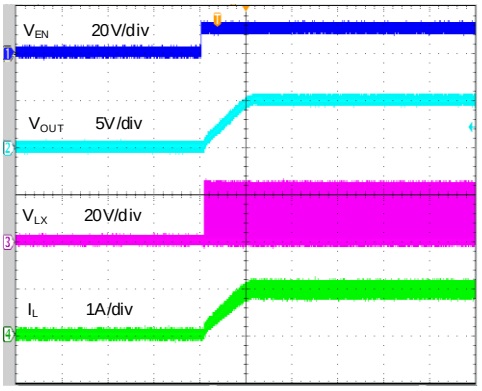
(V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 1A)



Time (10ms/div)

Startup from Enable

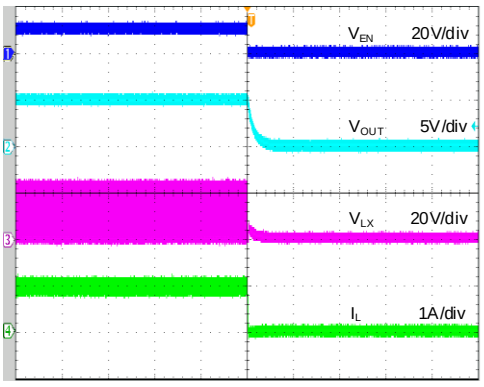
(V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 1A)



Time (2ms/div)

Shutdown from Enable

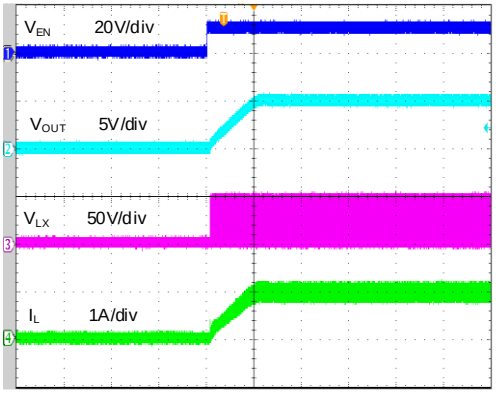
(V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 1A)



Time (400μs/div)

Startup from Enable

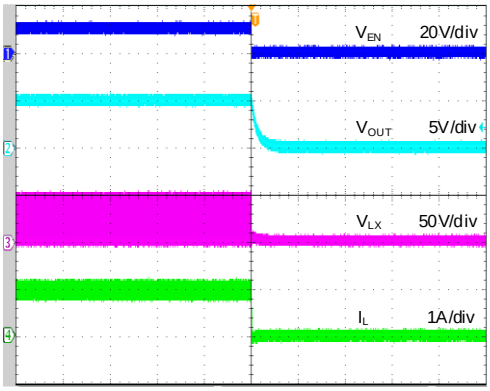
(V_{IN} = 48V, V_{OUT} = 5V, I_{OUT} = 1A)



Time (2ms/div)

Shutdown from Enable

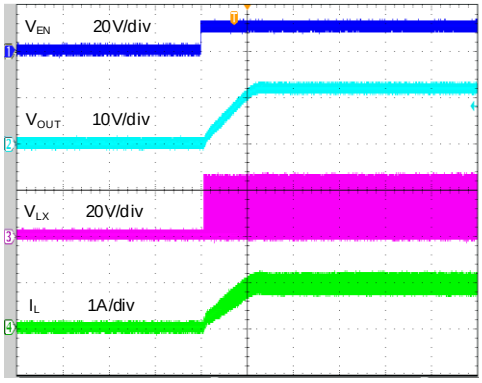
(V_{IN} = 48V, V_{OUT} = 5V, I_{OUT} = 1A)



Time (400μs/div)

Startup from Enable

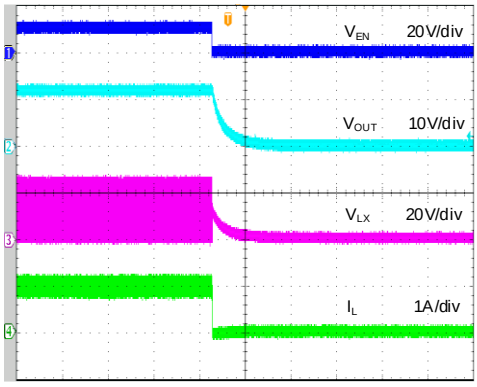
(V_{IN} = 24V, V_{OUT} = 12V, I_{OUT} = 1A)



Time (2ms/div)

Shutdown from Enable

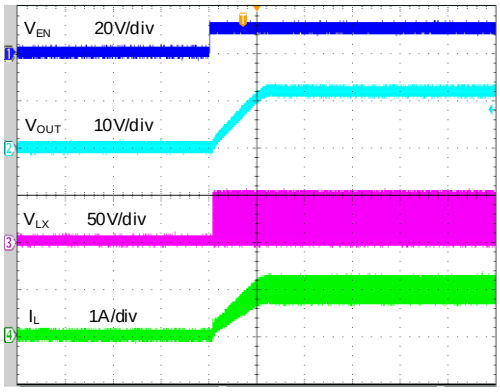
(V_{IN} = 24V, V_{OUT} = 12V, I_{OUT} = 1A)



Time (400μs/div)

Startup from Enable

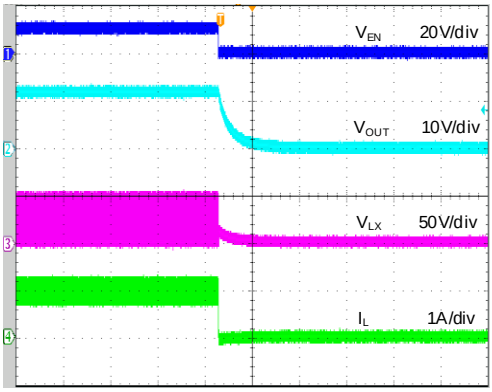
(V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 1A)



Time (2ms/div)

Shutdown from Enable

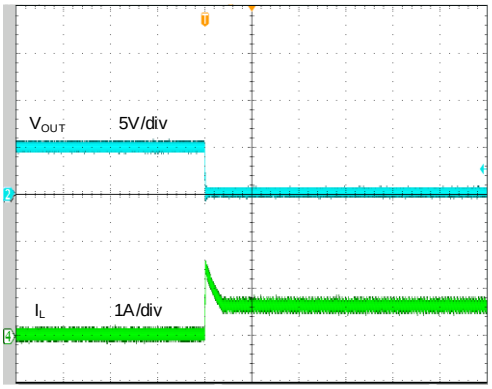
(V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 1A)



Time (400μs/div)

Short Circuit Protection

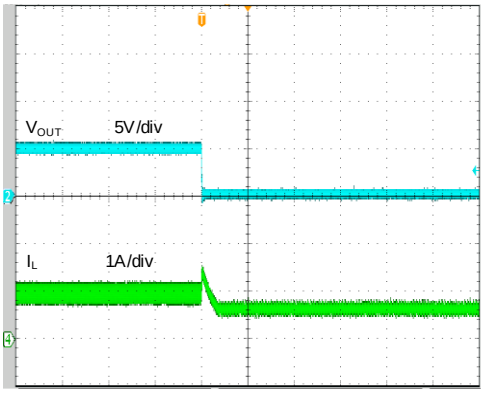
(V_{IN} = 48V, V_{OUT} = 5V, I_{OUT} = 0A ~ short)



Time (200μs/div)

Short Circuit Protection

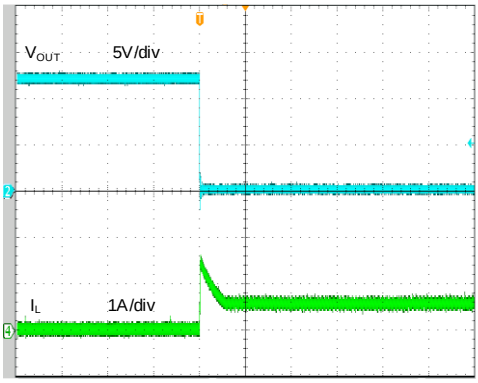
(V_{IN} = 48V, V_{OUT} = 5V, I_O = 1A ~ short)



Time (200μs/div)

Short Circuit Protection

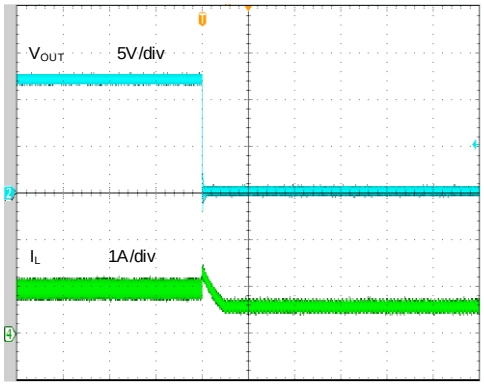
(V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 0A ~ short)



Time (200μs/div)

Short Circuit Protection

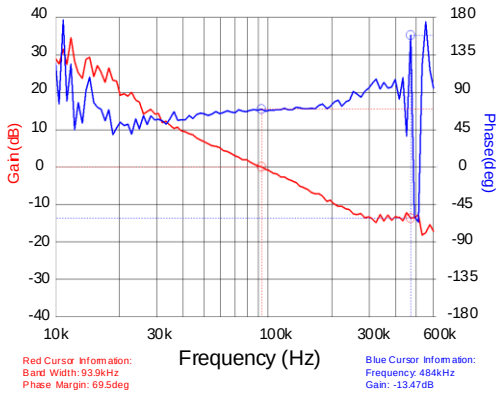
(V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 1A ~ short)



Time (200μs/div)

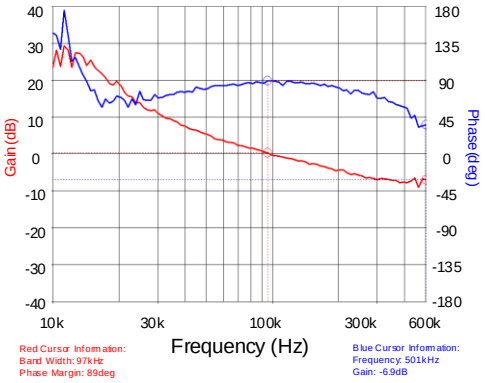
Bode Plot

(V_{IN} = 48V, V_{OUT} = 5V, I_{OUT} = 0.5A, f_{sw} = 500kHz)



Bode Plot

(V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 0.5A, f_{sw} = 500kHz)



Detailed Description

General Features

Constant On-time Architecture

Fundamental to any constant on-time (COT) architecture is the one-shot circuit or on-time generator, which determines how long to turn on the top FET. Each on-time (t_{ON}) is a "fixed" voltage ration,

$$t_{ON} = \left(\frac{V_{OUT}}{V_{IN}}\right) \times \left(\frac{1}{f_{SW}}\right)$$

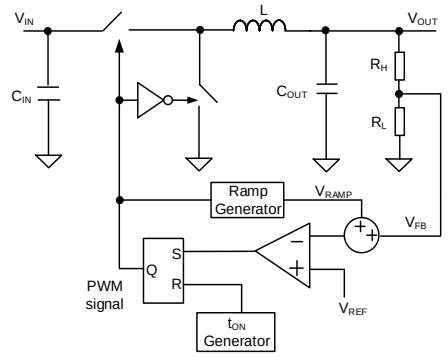
For example, considering that a hypothetical converter targets 5.1V output from a 12V input at 600kHz, the target on-time is

$$\frac{5.1V}{12V} \times \frac{1}{600kHz} = 708.33ns$$

Each t_{ON} pulse is triggered by the feedback comparator when the output voltage as measured at FB node drops below the regulated value. After one t_{ON} period, a minimum off-time ($t_{OFF,MIN}$) is imposed before any further switching is initiated, even if the output voltage is lower than the regulated value. This approach avoids making any switching decisions during the noisy periods just after switching events and while the switching node (LX) is rapidly rising or falling.

In a COT architecture, there is no fixed clock, so the top FET can turn on almost immediately after a load transient and subsequent switching pulses can be quickly initiated, ramping the inductor current up to meet load requirements with minimal delays. Traditional current mode or voltage mode control methods must simultaneously monitor the feedback voltage, current feedback and internal ramps and compensation signals to determine when to turn off the top FET and turn on the bottom FET. Considering these small signals in a switching environment are difficult to be noise-free after transmitting large current, making those architectures difficult to apply in noisy environments, even under low duty cycle operation.

Instant-PWM Operation



Silergy's COT ripple-based control strategy adds several proprietary improvements to the traditional COT architecture. Whereas most legacy based on COT implementations require a dedicated connection to the output voltage terminal to calculate the t_{ON} duration, instant-PWM control method derives this signal internally. Another improvement optimizes operation with low ESR ceramic output capacitors. In many applications it is desirable to utilize very low ESR ceramic output capacitors, but legacy COT converters may become unstable in these cases because the beneficial ramp signal that results from the inductor current flowing into the output capacitor maybe become too small to maintain stable operation. For this reason, instant-PWM synthesizes a virtual replica of this signal internally. This internal virtual ramp and the feedback voltage are combined and compared to the reference voltage. When the sum is lower than the reference voltage, the t_{ON} pulse is triggered as long as the minimum off-time has been satisfied and the inductor current as measured in the bottom FET is lower than the bottom FET current limit threshold. As the t_{ON} pulse is triggered, the bottom FET turns off and the top FET turns on. Then the inductor current ramps up linearly during the t_{ON} period. At the conclusion of the t_{ON} period, the top FET turns off, the bottom FET turns on and the inductor current ramps down linearly. This action also initiates the minimum off-time timer to ensure sufficient time for stabilizing any transient conditions and settling the feedback comparator before the next cycle is initiated. This minimum off-time is relatively short so that during high speed load transient t_{ON} can be retriggered with minimal delay, allowing the inductor current to ramp quickly to provide sufficient energy to the load side.

In order to avoid shoot-through, a dead time (t_{DEAD}) is generated internally between the top FET off and the bottom FET on period or the bottom FET off and the top FET on period.

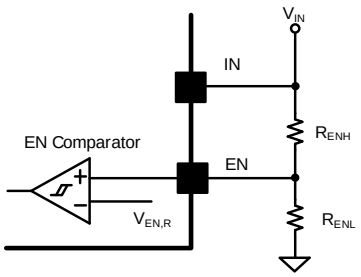
Input Under Voltage Lockout (UVLO)

To prevent operation before all internal circuitry is ready and to ensure that the top FET and bottom FET can be sufficiently enhanced, the SY21051 incorporates one input under voltage lockout protections. The SY21051 remains in a low current state and all switching actions are inhibited until V_{IN} exceeds its UVLO threshold. At that time, if EN is enabled, the device will be turned on. If V_{IN} falls below $V_{IN,UVLO}$ less than the input UVLO hysteresis, switching actions will again be suppressed.

Enable and Adjusting Input Under Voltage Lockout

The EN pin provides programmable ON/OFF control by connecting two external divided resistors, and has an accurate rising and falling threshold. The converter will

operate while the EN pin voltage exceeds the rising threshold. If the EN pin voltage is pulled below the falling threshold, the regulator will stop switching and enter shutdown state.



If the input UVLO threshold is low for some high input UVLO threshold requirement applications, use EN to adjust the input UVLO by adopting two external divided resistors.

$$V_{IN,UVLO,ADJ} = \frac{R_{ENL} + R_{ENH}}{R_{ENL}} V_{EN,R}$$

It is not recommended to connect EN to the IN node directly. A resistor with a value between 1kΩ and 1MΩ is recommended if the EN pin is pulled high to the IN node.

Soft-start

The device has a built-in soft-start to control the rise rate of the output voltage and limit the input current surge during IC startup. The typical soft-start time is 2ms.

Output Auto-Discharge Function

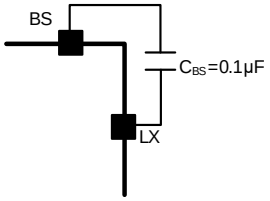
The SY21051 discharges the output voltage when the regulator shuts down from V_{IN} or EN, or over temperature protection, so that output voltage can be discharged in a minimal time, even output current is zero.

VDD Linear Regulator

The SY21051 integrates two low drop-out linear regulators to produce one internal power V_{DD}, which can power the internal gate drivers, PWM logic, analog circuitry and other blocks. After the converter is turned on, the V_{DD} can be supplied by input voltage then supplied by VCC input voltage if VCC input voltage is high enough. Connect one diode from output voltage to VCC can be one choice to reduce power consumption.

External Bootstrap Capacitor

The external bootstrap capacitor provides the gate driver voltage for the N-channel top FET. A 0.1μF low-ESR ceramic capacitor connected between the BS pin and the LX pin is recommended.



Fault Protection Modes

Over Current and Short Circuit Protection

If the top FET current exceeds the top current-limit threshold, the top FET will turn off and the bottom FET will turn on. If the bottom FET current exceeds the bottom current limit threshold, the bottom FET will continue turning on until the bottom FET current decreases below the bottom current limit threshold. As a result, both inductor peak and valley currents are limited. If the output current continues to increase, the output voltage will drop. If the output voltage falls below 33% of the regulation level, an output short condition is detected and the converter valley current limit point will decrease to half of bottom FET current limit threshold.

Over Temperature Protection (OTP)

The converter includes over temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds 150°C. Once the junction temperature cools by approximately 15°C, the device will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the OTP threshold.

Application Information

The SY21051 is highly integrated, so only the RON resistor, the feedback resistors R_H and R_L, the input capacitor C_{IN}, the output inductor L and the output capacitor C_{OUT} need to be selected for the targeted application specifications.

RON Resistor Selection

The switching frequency for this converter CCM operation is determined by the RON resistor. Connect a resistor from RON pin to V_{IN} to program the switching frequency. The switching frequency can be calculated using the following equation:

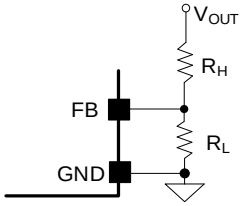
$$f_{SW}(kHz) = \frac{11 \times V_{OUT}(V) + 500}{R_{RON}(M\Omega)}$$

Feedback Resistor Divider R_H and R_L

Choose R_H and R_L to program the proper output voltage. A value between 1kΩ and 1MΩ is recommended for both resistors to minimize power consumption under light loads.

If V_{OUT} = 5V and R_H is chosen as 100kΩ, for example, then R_L can be calculated as follows:

$$R_L = \frac{1.2V}{V_{OUT} - 1.2V} R_H$$



With a calculated value of 31.6kΩ for R_L, a standard 1% 31.6kΩ resistor is selected.

Input Capacitor Selection

Input filter capacitors reduce the ripple voltage on the input, filter the switched current drawn from the input supply, and reduce EMI. When selecting an input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating higher than the system requirements. The X5R series ceramic capacitors are most often selected due to their small size, low cost, surge-current capability, and high RMS current ratings over a wide temperature and voltage range. However, systems that are powered by a wall adapter or other long and therefore inductive cabling may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum, or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplicity, use an input capacitor with an RMS current rating greater than 50% of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1 - D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. A single 2.2µF X5R capacitor is sufficient in most applications.

Inductor Selection

There are several considerations in choosing the inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{f_{SW} \times I_{OUT,MAX} \times 40\%}$$

Where f_{SW} is the switching frequency and I_{OUT_MAX} is the maximum load current.

The SY21051 is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected greater than the peak inductor current under full load condition.

$$I_{SAT\_MIN} > I_{OUT\_MAX} + \frac{V_{OUT} \times (1 - V_{OUT}/V_{IN\_MAX})}{f_{SW} \times L \times 2}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with smaller DCR to achieve a good overall efficiency.

Output Capacitor C_{OUT}

Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady-state ripple and transient requirements must be taken into consideration when selecting C_{OUT}. For the best performance, use an X5R or better grade ceramic capacitor with a 16V rating, and capacitance of at least 10µF.

For applications where the design must meet stringent ripple requirements, the following considerations must be followed.

The output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple). When calculating total ripple, consider both.

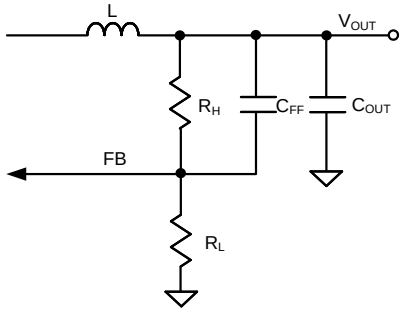
$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

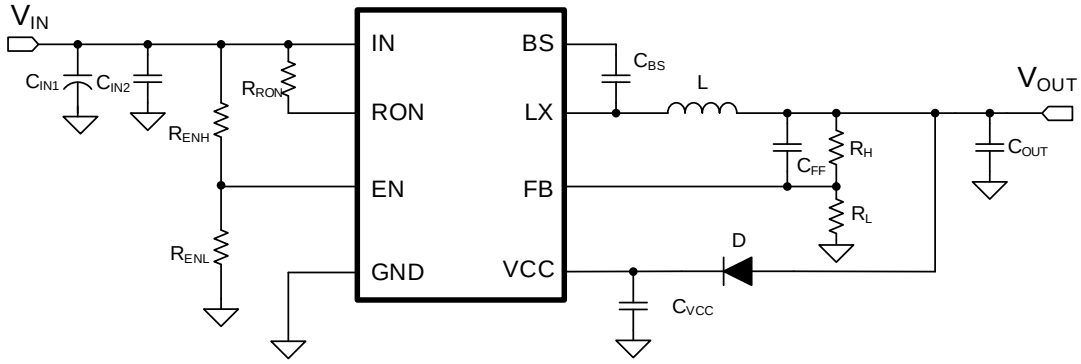
The capacitive ripple might be higher because the effective capacitance for ceramic capacitors decreases with the voltage across the terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

Load Transient Considerations

The SY21051 integrates compensation components to achieve fast transient response and improved stability. In some applications, adding a ceramic capacitor (feedforward capacitor C_{FF}) in parallel with R_H may further speed up the load transient response, and is therefore recommended for applications with large load transient step requirements.



Application Schematic (V_{OUT}=5V)



BOM List

Designator	Description	Part Number	Manufacturer
C_{IN1}	22μF/200V Electrolytic Cap		
C_{IN2}	1μF/100V/X7R, 1206	C3216X7R2E105K	TDK
C_{BS}, C_{VCC}	0.1μF/50V/X7R, 0603	C1608X7R1H104K	TDK
C_{FF}	220pF/50V/C0G, 0603	C1608C0G1H221J	TDK
C_{OUT}	10μF/25V/X5R, 1206	C3216X5R1E106M	TDK
L	33μH/2.2A, inductor	CDRH8D43NP-330NC	Sumida
D	0.2A/30V	BAT54	ON Semiconductor
R_H	100kΩ, 1%, 0603		
R_L	31.6kΩ, 1%, 0603		
R_{RON}, R_{ENL}	1MΩ, 1%, 0603		
R_{ENH}	1kΩ, 1%, 0603		

Recommend Table for Typical Applications

V_{OUT}(V)	R_H(kΩ)	R_L(kΩ)	C_{FF}(pF)	L/Part Number	C_{OUT}
5	100	31.6	220	33μH/CDRH8D43NP-330NC	10μF/25V/X5R, 1206
12	100	11.11	220	47μH/CDRH8D43NP-470NC	10μF/25V/X5R, 1206

Layout Design

The layout design of SY21051 is very important for proper operation. The guidelines for a good PCB layout are summarized below:

- **Input Capacitors:** Place the input capacitor close to the IN and GND pins, minimizing the loop formed by these connections. The input capacitor should be connected to the IN and GND using wide copper areas.
- **Output Capacitor:** Guarantee the C_{OUT} negative sides are connected with GND pin by wide copper traces instead of vias, in order to achieve better accuracy and stability of output voltage.
- **VCC Capacitor:** Place the VCC capacitor close to VCC using a short, direct copper trace to the nearest device GND pin.
- **Feedback Network:** Place the feedback components (R_H, R_L, and C_{FF}) as close to FB pin as possible. Avoid routing the feedback line near LX, BS or other high frequency signal as it is noise sensitive. Make the feedback sampling point Kelvin connect with C_{OUT} rather than the inductor output terminal.
- **LX Connection:** Keep LX area small to prevent excessive EMI, while providing wide copper traces to minimize parasitic resistance and inductance.
- **BS Capacitor:** Place the BS capacitor on the same layer as the device, keep the BS voltage path (BS, LX and C_{BS}) as short as possible.
- **GND Vias:** Place adequate number of vias on the GND layer around the device for better thermal performance. The exposed GND pad should be connected by a larger copper area than its size, place multiple GND vias on it for heat dissipation.

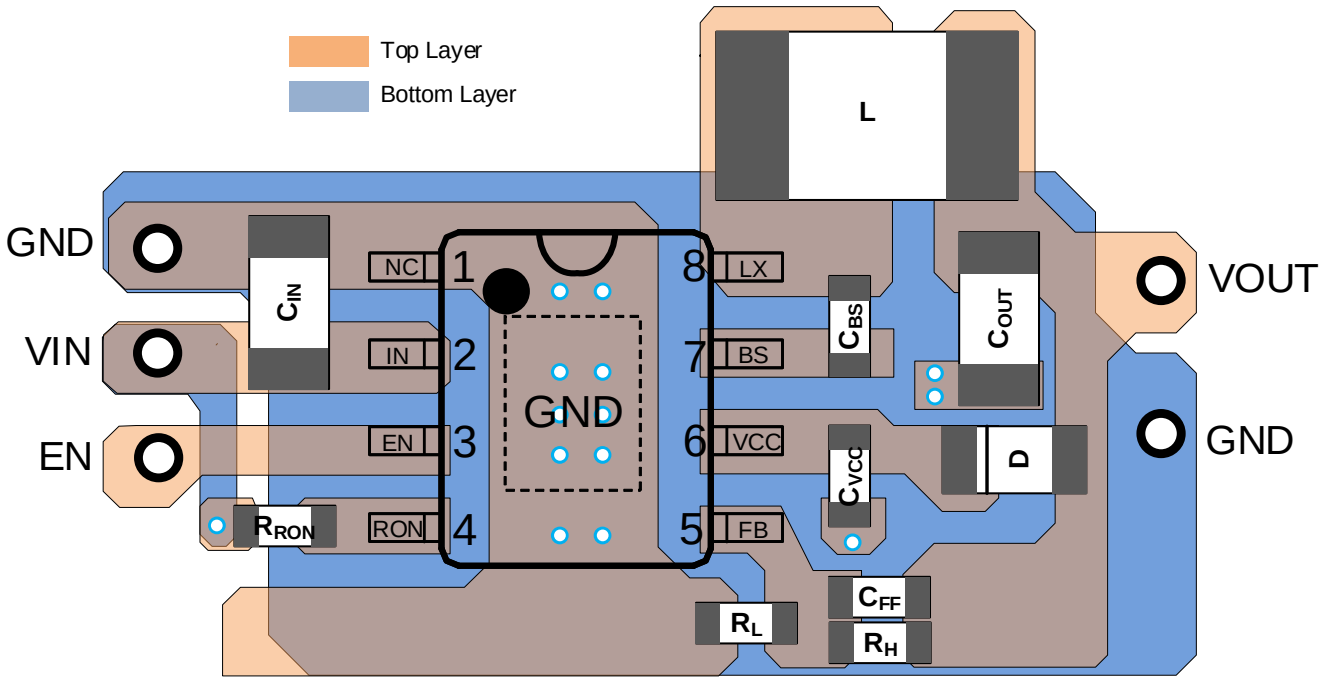
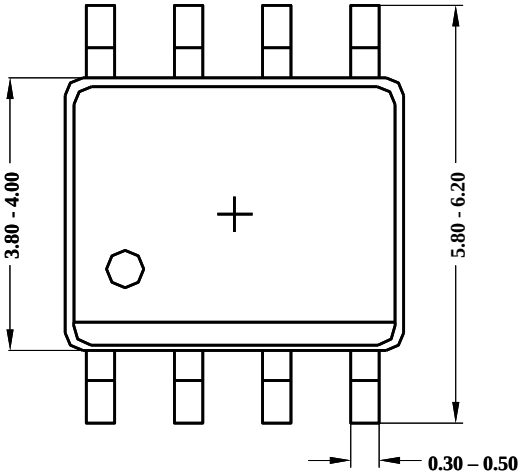
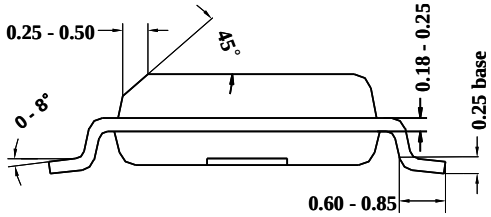


Figure4. PCB Layout Suggestion

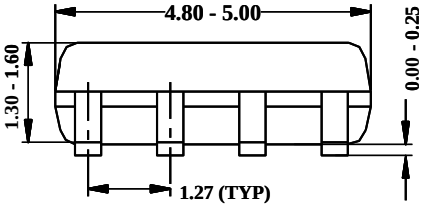
SO8E Package Outline & PCB Layout



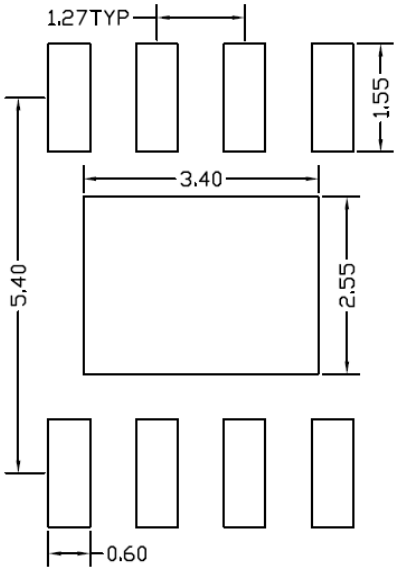
Top View



Side View



Side View

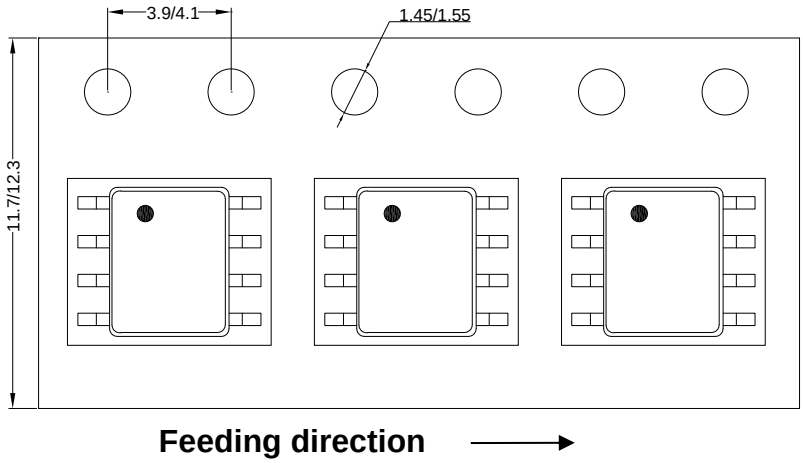


Recommended Pad Layout

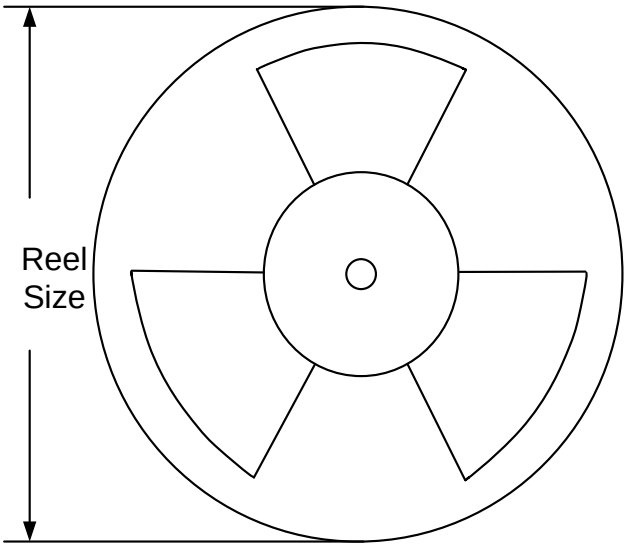
Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

SO8E Taping Orientation



Carrier Tape & Reel Specification for Packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOP8E	12	8	13"	400	400	2500

Others: NA

Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, it is not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
Dec. 29, 2014	Revision 0.9	Initial Release
Aug. 30, 2023	Revision 1.0	Production Release

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