Application Note: SY5072

BCM Boost PFC Controller

Preliminary Specification

General Description

The SY5072 is a constant voltage BCM boost controller with Power Factor Correction (PFC) function. Constant ON Time control is applied to achieve high PF and low THD without multiplier. It drives the Boost converter in the Quasi-Resonant mode for high efficiency and better EMI performance. It adopts special design to achieve quick start up and reliable protection for safety requirement.

Ordering Information

SY5072 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY5072ABC	SOT23-6	----

Features

- Valley Turn-on to Achieve Low Switching Losses
- Frequency Reduce in Light Load
- Internal High Current MOSFET Driver: 75mA Sourcing and 400mA Sinking
- MOSFET Over-Current Protection(OCP)
- Internal THD Optimization to Achieve Low THD
- Internal Transition Optimization
- RoHS Compliant and Halogen Free
- Compact Package: SOT23-6

Applications

- AC/DC Adapters
- Pre-stage for Two-stage AC/DC Converter
- LED Lighting

Typical Applications

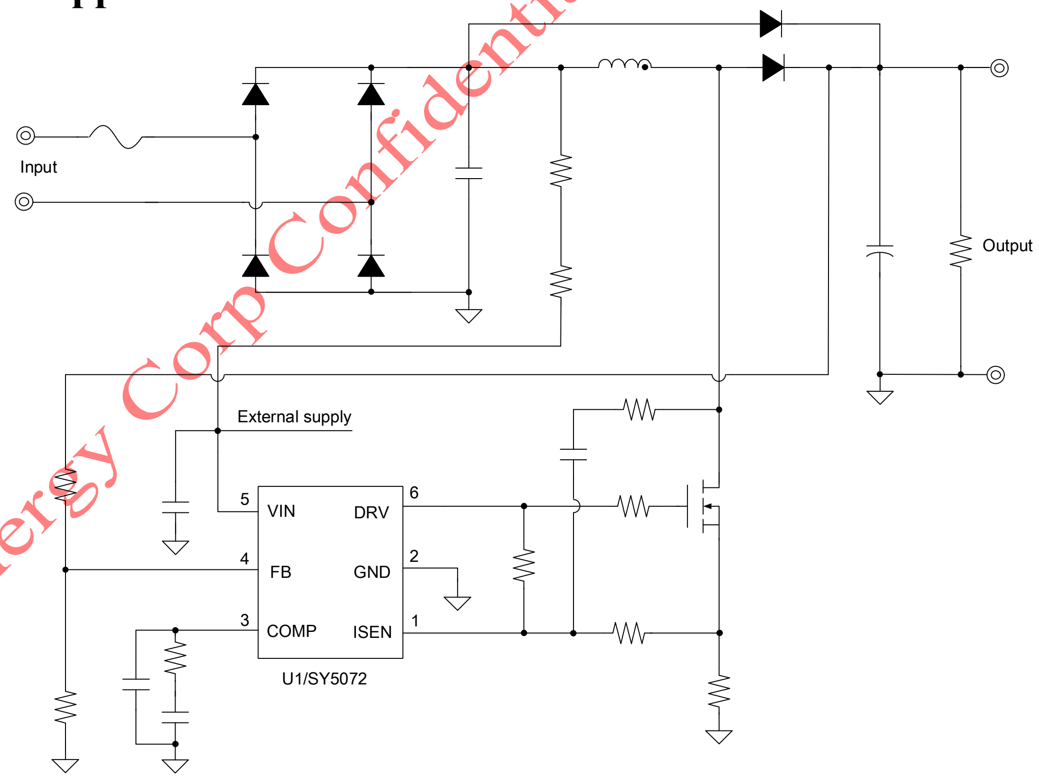
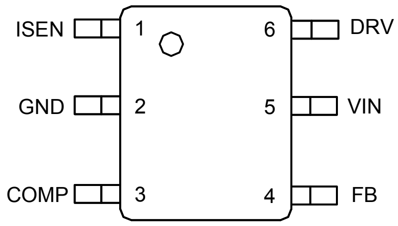


Figure 1. Schematic Diagram

Pinout (top view)



(SOT23-6)

Top Mark: dQ *xyz* **(**device code: dQ, ***x=year code, y=week code, z= lot number code*****)**

Pin	Name	Description
1	ISEN	Current limit and Zero-crossing sense PIN.
2	GND	Ground pin.
3	COMP	Loop compensation pin. Connect a RC network across this pin and ground to stabilize the control loop.
4	FB	Feedback pin. This pin receives output feedback voltage. The internal reference is 1.25V.
5	VIN	Power supply pin.
6	DRV	Gate driver pin. Connect this pin to the gate of primary MOSFET with a resistor.

Absolute Maximum Ratings (Note 1)

VIN -- -0.3V to 28V
DRV -- -0.3V to 25V
ISEN, COMP, FB -- 3.6V
Power Dissipation, @ T_A = 25°C SOT23-6 -- 0.6W
Package Thermal Resistance (Note 2)
SOT23-6,θ_{JA}--- 170°C/W
SOT23-6,θ_{JC}--- 130°C/W
Temperature Range -- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) -- 260°C
Storage Temperature Range --- -65°C to 150°C

Recommended Operating Conditions (Note 3)

VIN, DRV -- 9V~22V
Absolute maximum range--- -40°C to 150°C

Block Diagram

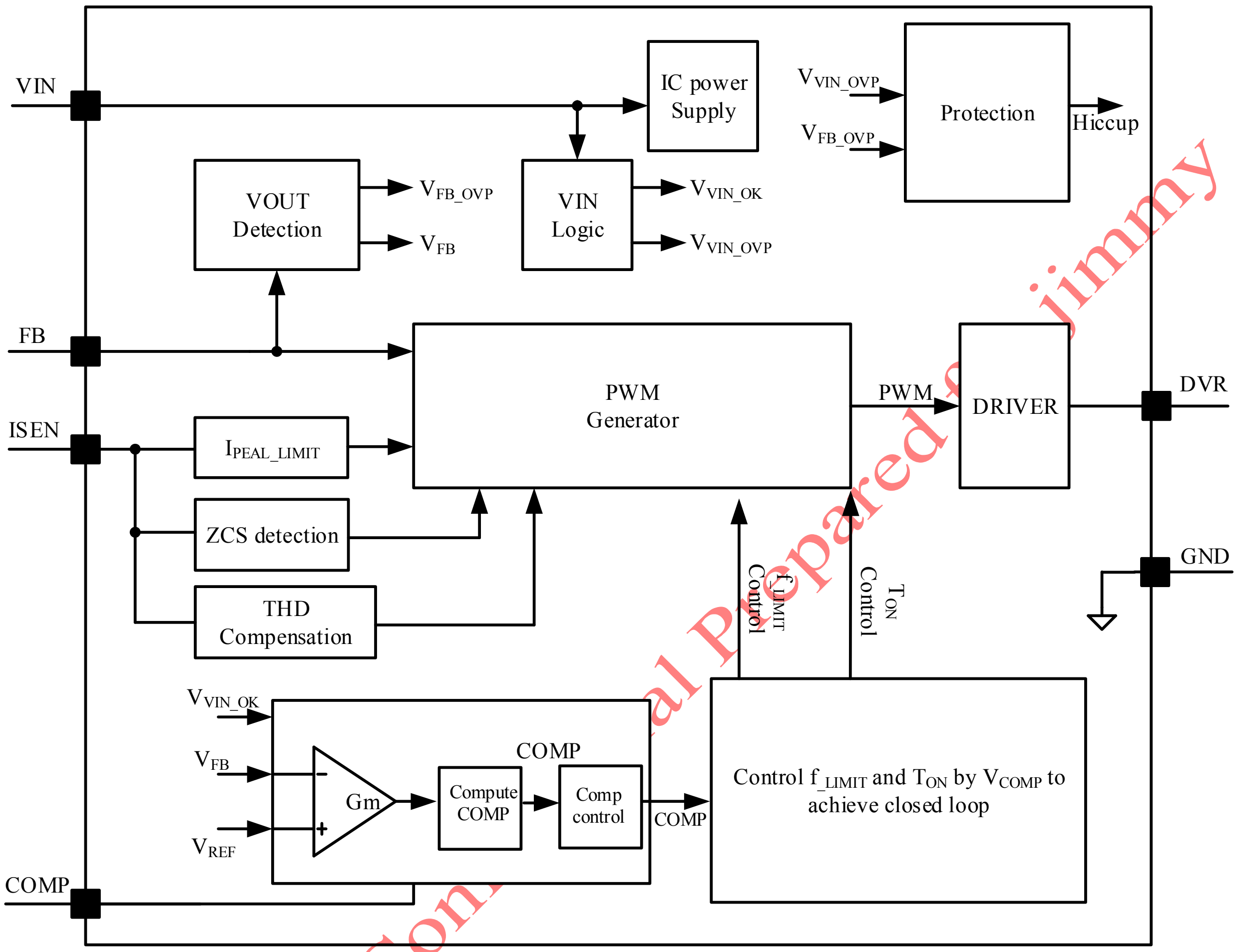


Figure2. Block Diagram

Electrical Characteristics

(V_{IN} = 12V (Note 3), T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
VIN Turn-on Threshold	V_{VIN_ON}			14.6		V
VIN Turn-off Threshold	V_{VIN_OFF}			7.5		V
VIN OVP Voltage	V_{VIN_OVP}			24.5		V
Start up Current	I_{ST}	$V_{VIN}<V_{VIN\_ON}$		1.9		µA
Quiescent Current	I_Q	No Switching		0.45		mA
Discharge Current in Protection Mode	I_{VIN_P}	$V_{VIN}>V_{VIN\_OVP}$		5.0		mA
Error Amplifier Section						
Current Limit Voltage	V_{ISEN_LIMIT}			1.00		V
V_{FB} at Fast Start up	V_{FB_LOW}			1.10		V
Internal Reference Voltage	V_{REF}		1.225	1.250	1.275	V
OVP Voltage Threshold	V_{FB_OVP}			1.35		V
Gate Driver Voltage	V_{Gate}			12		V
Typical Source Current	I_{SOURCE}			75		mA
Typical Sink Current	I_{SINK}			400		mA
Max ON Time	T_{ON_MAX}	Vcomp=2.5V		24		µs
Min ON Time	T_{ON_MIN}			0.45		µs
Thermal Section						
Thermal Shutdown Temperature	T_{SD}			155		℃

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: Increase VIN pin voltage gradually higher than $V_{VIN,ON}$ voltage then turn down to 12V.

Operation

SY5072 is a constant voltage boost controller with Power Factor Correction (PFC) function designed to drive cost-effective pre-converter to comply with line current harmonic limits.

SY5072 operates in boundary conduction mode (BCM) suitable for applications up to 150 W. Its voltage mode (constant on time control) scheme enables it to obtain near unity power factor without line voltage sensing network.

To achieve higher efficiency and better EMI performance, SY5072 drives Boost MOSFET in the Quasi-resonant mode, which means to turn on the power MOSFET at voltage valley.

Integrate THD compensation which is adjustable for different application to achieve low THD.

Better line transition and load transition due to internal optimization.

The start-up current of SY5072 is rather small (1.9μA typically) and frequency reduce in light load to reduce the standby power loss further.

SY5072 integrates suitable Source 75mA/Sink 400mA gate driver for fast switching which is good for EMI improvement and IC power-loss.

SY5072 provides reliable protections such as Over Voltage Protection (OVP), Over Current Protection (OCP), Over Temperature Protection (OTP), etc.

SY5072 is available with SOT23-6 package for now.

Applications Information

Start up

After AC supply or DC BUS is powered on, the capacitor C_{VIN} across VIN and GND pin is charged up by BUS voltage through a start-up resistor R_{ST}. The low startup current consumption (=1.9uA) enables minimized standby power dissipation.

Once V_{VIN} rises up to V_{VIN-ON}, the internal blocks start to work and V_{VIN} decreases due to the power consumption of IC till the external supply or the auxiliary winding of Boost inductor can afford V_{VIN}. SY5072 includes an under voltage lockout (UVLO) which ensures working till V_{VIN} decreases to be less than $V_{VIN-OFF}$. This hysteresis ensures sufficient time to wait for the V_{IN} supplied from the external supply or the auxiliary winding.

The entire start up procedure is divided into two sections as shown in Fig.5, wherein, t_{STC} is the C_{VIN} charged up section, and t_{STO} is the output voltage built-up section. The start-up time t_{ST} composes of t_{STC} and t_{STO}. Usually t_{STO} is much smaller than t_{STC}.

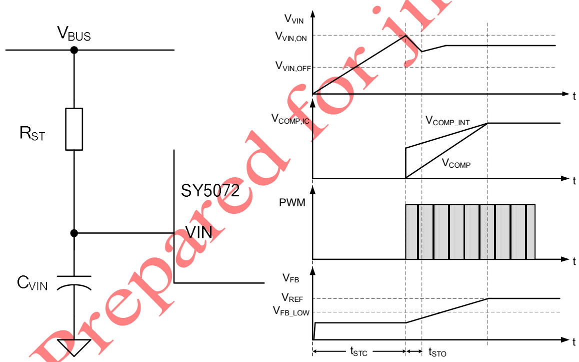


Figure3. Start up

If V_{FB} is lower than certain threshold V_{FB_LOW}, which means the output voltage is not built up, V_{COMP} is pulled up by a big resistor (Rg) to high clamped V_{COMP_INT}; and hold at this level until V_{FB} is near to V_{REF}. This operation is aimed to build up enough output voltage as soon as possible. The simple logical diagram shown as Figure 4.

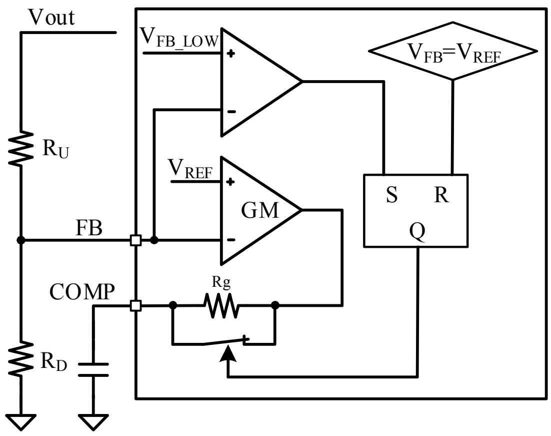


Figure4. Startup logical diagram

If R_{ST} is connected between rectified BUS line and VIN pin, then the design of R_{ST} and C_{VIN} can follow the rules shown below (same as when R_{ST} is connected between output terminal and VIN pin):

(a) Preset start-up resistor R_{ST}, make sure that the current through R_{ST} is larger than I_{ST} and smaller than 1mA.

$$\frac{V_{BUS}}{1mA} < R_{ST} < \frac{V_{BUS}}{I_{ST}} \quad (1)$$

Wherein, V_{BUS} is the BUS line voltage.

(b) Select C_{VIN} to obtain an ideal start up time t_{ST} (t_{ST}>>t_{STO}), and ensure the output voltage is built up at one time.

$$C_{VIN} = \frac{(\frac{V_{BUS}}{R_{ST}} - I_{ST}) \times t_{ST}}{V_{VIN\_ON}} \quad (2)$$

(c) If the energy stored in C_{VIN} is not enough for IC building up the output voltage smoothly, try to increase C_{VIN} and decrease R_{ST}. Then go back to step (a) and redo such design flow till the ideal start up procedure is obtained.

Shut down

After AC supply or DC BUS is powered off, the energy stored in the BUS capacitor will be discharged. If the auxiliary winding cannot provide enough energy to VIN pin, V_{VIN} will drop down.

Once V_{VIN} is lower than V_{VIN_OFF}, IC stops working and V_{COMP} will be discharged to zero.

Quasi-resonant Operation

QR mode operation provides low turn-on switching losses in MOSFET.

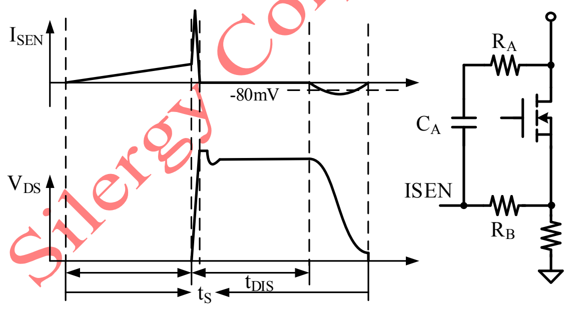


Figure5. QR mode operation

The voltage across drain and source of Boost MOSFET V_{DS} is reflected by RC (R_A&C_A) which is connected between the drain of MOSFET and I_{SEN} pin. A resistor (R_B) is connected between I_{SEN} and I_{SEN} resistor to detect negative voltage if the I_{SEN} voltage decreases to -80mV. Approximate the inductor current is crossing zero. The MOSFET is turned on after 500nS delay when crossing zero has been detect.

The capacitor C_A is need for ZCS detect. The larger the capacitance capacity, the greater the capacitance loss. Thus, C_A=10pF and RA=1K is recommend.

The resistor R_B is use for amplifying resonance signal and easy for ISEN pin to detect crossing zero signal.

Error Amplifier Regulation

SY5072 regulates the boost output voltage using a trans-conductance internal error amplifier (EA). The inverting terminal of the EA is pinned out to FB, the non-inverting terminal is connected to an internal 1.25V voltage reference, and the EA output is pinned out to COMP (Fig.6).

The R_k is a parasitic resistance that is good for loop control and the resistance is about 8K.

Because of the trans-conductance error amplifier employing, the FB pin can also be used to detect the output over voltage condition and under voltage condition.

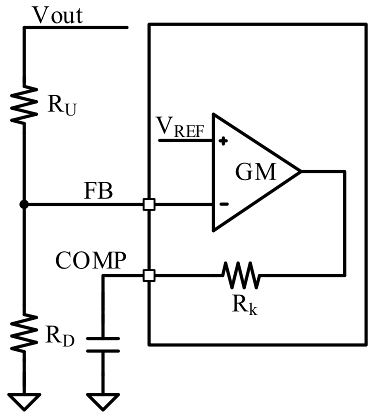


Figure.6 Output voltage feedback circuit

A resistor divider (R_U and R_{DOWN}) scales down the Boost output voltage (V_{OUT}) and connects to the FB pin. If the output voltage is less than the regulation, then the control voltage (V_{COMP}) increases the on time of the driver, which increases the power transferring from the input to the output. If V_{OUT} is higher than the regulation, the V_{COMP} decreases the on time to limit the power transferring.

The output voltage is regulated by equation (3).

$$V_{OUT} = V_{REF} \times \left(\frac{R_U + R_D}{R_D} \right) \qquad (3)$$

Over Voltage Protection (OVP)

Because of the extremely low bandwidth of PFC's voltage loop, there is a risk of overshoots at output side during startup, load steps, and line steps. For reliable operation, the over voltage protection (OVP) is necessary to prevent output voltage from exceeding the ratings of the PFC stage components.

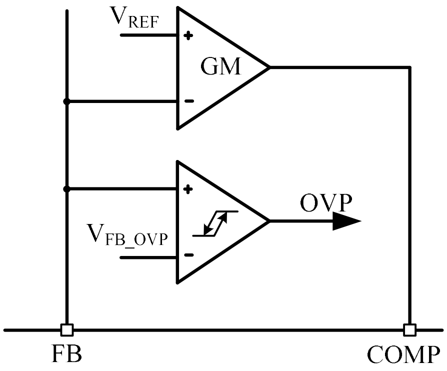


Figure.7 Output protection circuit

SY5072 detects the over voltage condition (V_{FB_OVP}) and disables the driver until V_{OUT} decreases to a safe level, which ensures that V_{OUT} is within the PFC stage component ratings. An internal comparator connected to the FB pin provides the OVP protection.

OVP threshold V_{FB_OVP} is 8% above the regulation voltage reference. The OVP voltage is calculated using equation (4).

$$V_{OUT} = V_{FB\_OVP} \times \left(\frac{R_U + R_D}{R_D} \right) \qquad (4)$$

The value of Cbulk is sized to ensure that OVP is not inadvertently triggered by the 100 Hz or 120 Hz ripple of V_{OUT}.

In the steady states, the minimum value of Cbulk is calculated using equation (5) and assume that the ESR of output capacitor is insignificant.

$$C_{bulk} \geq \frac{P_{OUT}}{2 \times \pi \times V_{ripple(peak-peak)} \times f_{line} \times V_{OUT}} \qquad (5)$$

Wherein, $V_{ripple(peak-peak)}$ is the peak-to-peak output voltage ripple and usually selected in the range of 3.0% of the output voltage; f_{line} is the ac line frequency (50Hz or 60Hz).

Frequency reduction

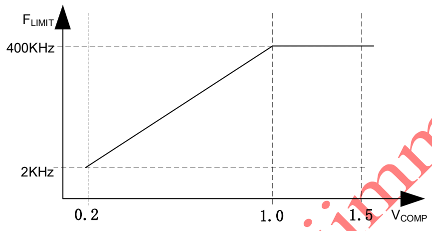


Figure.8 Frequency reduction

Frequency reduction depends on Vcomp:

When Vcomp > 1.0V, frequency limited at 400 KHz;

When Vcomp < 1.0V, frequency will slowly reduce from 400 KHz to 2 KHz.

Special Design for Transition

To have good transition performance, special design is integrate into SY5072.

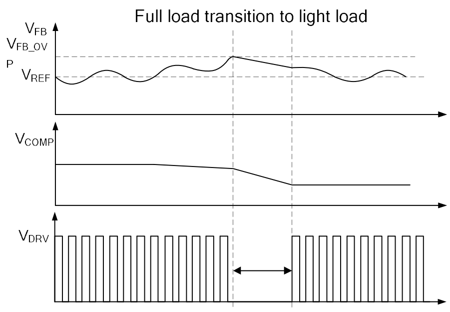


Figure.9 Load transition (Full load to light load)

When VSEN touch V_{FB_OVP}, IC will stop DRV to decrease output energy, and then V_{COMP} decrease by loop to reach a new balance.

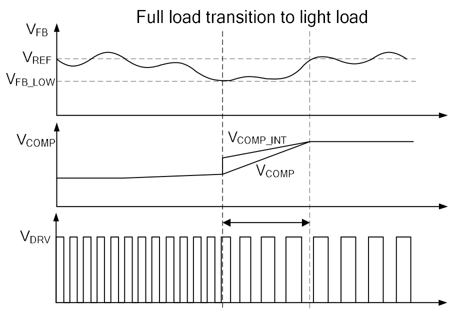


Figure.10 Load transition (light load to Full load)

When FB touch V_{FB_LOW}, a big resistor will be connected to COMP(refer to startup logic), thus, V_{COMP_INT} will higher than V_{COMP}, the ON time of the DRV increase suddenly to expedite output energy until FB reach V_{REF} and V_{COMP} equal to V_{COMP_INT} again. V_{COMP} reach a new balance.

Line transition is similar to Load transition. If input voltage changes from low to high, it can refer to Full load to light load; if input voltage changes from high to light, it can refer to light load to Full load.

Over Current Protection (OCP)

The dedicated ISEN pin of SY5072 limits the MOSFET peak current cycle by cycle if the voltage of the ISEN pin exceeds V_{ISNE_LIMIT}.

The maximum power inductor current (I_{PK_MAX}) occur in minimum input voltage when full load. So R_{ISEN} could be selected by:

$$R_{sense} = \frac{90\% \times V_{ISEN\_LIMIT}}{I_{PK\_MAX}} \quad (6)$$

Where V_{ISEN_LIMIT} is a protection for transformer (If V_{ISEN} touch this voltage, gate will turn off), and I_{PK_MAX} is the maximum power inductor in steady.

Internal THD Compensation

Because of the existence of the inductance and the capacitance C_{ds} of the MOSFET, when inductance current is zero, they begin LC resonant. Before the MOSFET switch on, there is a part of negative current in inductance current.

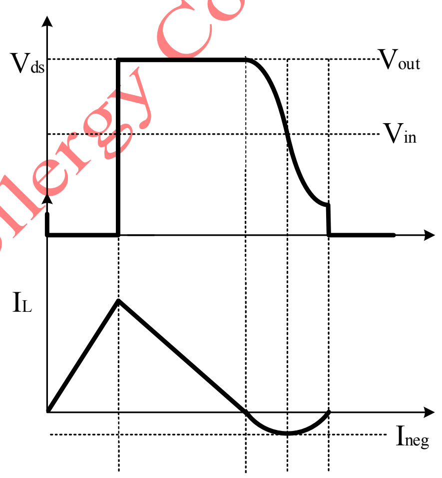


Figure.11 current of inductance

The term i_{neg} is a function of V_{in}, V_{out}, L and C_{ds}. In fact, during the resonance we can assume no loss and use energy conservation to calculate it:

$$i_{neg} = (V_{out} - V_{in}) \times \sqrt{C_{ds}/L} \quad (7)$$

From a power frequency period, the waveform of inductance current is shown in Figure 12.

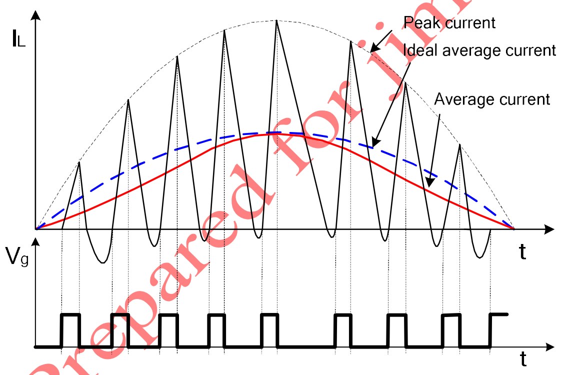


Figure.12 average current waveform of inductance

Ideal average current which controlled by COT is a sin wave following the input voltage. But the actual average current has been distorted. That is bad for THD performance.

THD compensation helps to remove the effect of negative current to achieve better THD. The analog implementation example shown in Figure 13 is similar to a standard COT with the addition of a voltage comparator with fixed threshold (200mV).

Ton generator does not work until ISEN larger than fixed threshold (200mV). After that, comparator output will be set high to enable the Ton generator and Ton generator begin to work. The compensation current ΔI can be calculated using equation (8):

$$\Delta I = 200mV/R_S \quad (8)$$

If $\Delta I = i_{neg}$,the effect of the negative current will be offset and THD will be optimized.

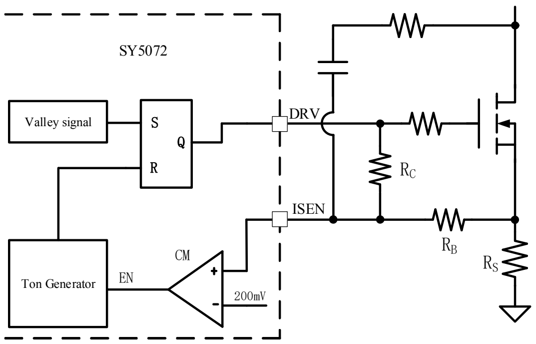


Figure.13 THD compensation logic

Actually, different applications will have different LC parameters and Ineg will be difference. The SY5072 support external parameter modification to change the compensation current and achieve the optimal THD. External parameter is the resistor R_B and R_C. Shown in the figure 13.

Assume R_C>>R_B and the compensation △ I can be calculated using equation (9).

$$\Delta I = (200mV - V_{DRV} / R_C \times R_B) / R_S \quad (9)$$

Different applications need different ΔI . R_C is the discharge resistor of MOSFET and 10K is the recommend. Then changing R_B can achieve ideal THD preferment.

Power Device Design

MOSFET and Diode

When the operation condition is maximum voltage input and full load output, the MOSFET and Boost diode suffer the maximum voltage stress. Considering the output voltage, the overvoltage magnitude, and the derating margin for safety, 600V device is commonly selected.

When the operation condition is minimum voltage input and full load output, the semiconductor devices suffer the maximum current stress.

Peak current of inductor:

$$I_L(peak) = \frac{2\sqrt{2} \times P_{OUT}}{\eta \times V_{IN\_MIN}} \quad (10)$$

Peak current of MOSFET:

$$I_{MOSFET(peak)} = I_{DIODE(peak)} = I_{L(peak)} \quad (11)$$

RMS current of inductor:

$$I_{L(rms)} = \frac{2 \times P_{OUT}}{\sqrt{3} \times \eta \times V_{IN\_MIN}} \quad (12)$$

RMS current of MOSFET:

$$I_{MOSFET(rms)} = \frac{2}{\sqrt{3}} \times \frac{P_{out}}{\eta \times V_{IN\_MIN}} \times \sqrt{1 - (\frac{\sqrt{2} \times 8 \times V_{IN\_MIN}}{3 \times \pi \times V_{OUT}})} \quad (13)$$

RMS current of DIODE:

$$I_{DIODE(rms)} = \frac{4}{3} \times \frac{P_{OUT}}{\eta \times \sqrt{V_{IN\_MIN} \times V_{OUT}}} \times \sqrt{\frac{2 \times \sqrt{2}}{\pi}} \quad (14)$$

AVE current of DIODE:

$$I_{DIODE(ave)} = I_{OUT} = \frac{P_{OUT}}{V_{OUT}} \quad (15)$$

Wherein, P_{OUT} is the output power, V_{OUT} is the output voltage, V_{IN_MIN} is the minimum input AC voltage, is the estimated efficiency.

Boost inductor

Once the minimum frequency $f_{s,\min}$ is set, the inductance can be induced. According to BCM operating principle, boost inductor is calculated using equation (15).

$$L_{MAX} = \frac{V_{IN}^2 \times (V_{OUT} - \sqrt{2} \times V_{IN})}{2 \times f_{sw\_MIN} \times P_{IN} \times V_{OUT}} \quad (16)$$

Wherein, $f_{s,\min}$ is the preset minimum switching frequency, V_{IN} is input voltage.

Once the inductance is induced, we can calculate the winding turns for a specific core. The design rules are shown below.

(a) Select the magnetic core and identify the effective area Ae;

(b) Preset the maximum magnetic flux ΔB normally within 0.22-0.26T;

(c) Calculate primary winding turns N using equation (17);

$$N = \frac{L \times I_{L(peak)}}{Ae \times \Delta B} \quad (17)$$

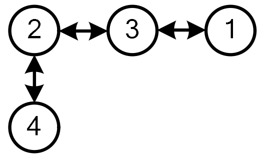
Then select an appropriate wire diameter, grind the core to get required inductance with calculated turns number.

Layout

(a) To achieve better EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to the BUS line capacitor first, then to the switching circuit.

(b) The circuit loop of all switching circuit should be kept small: power loop and auxiliary power loop.

(c) The connection of primary ground is recommended as:



Ground ① : ground of BUS line capacitor
Ground ② : ground of bias supply capacitor
Ground ③ : ground node of current sample resistor.
Ground ④ : ground of signal trace

(d) bias supply trace should be connected to the bias supply capacitor first instead of GND pin. The bias supply capacitor should be put beside the IC.

(e) Loop of 'Source pin – current sample resistor – GND pin' should be kept as small as possible.

(f) The resistor divider connected to FB pin is recommended to be put beside the IC.

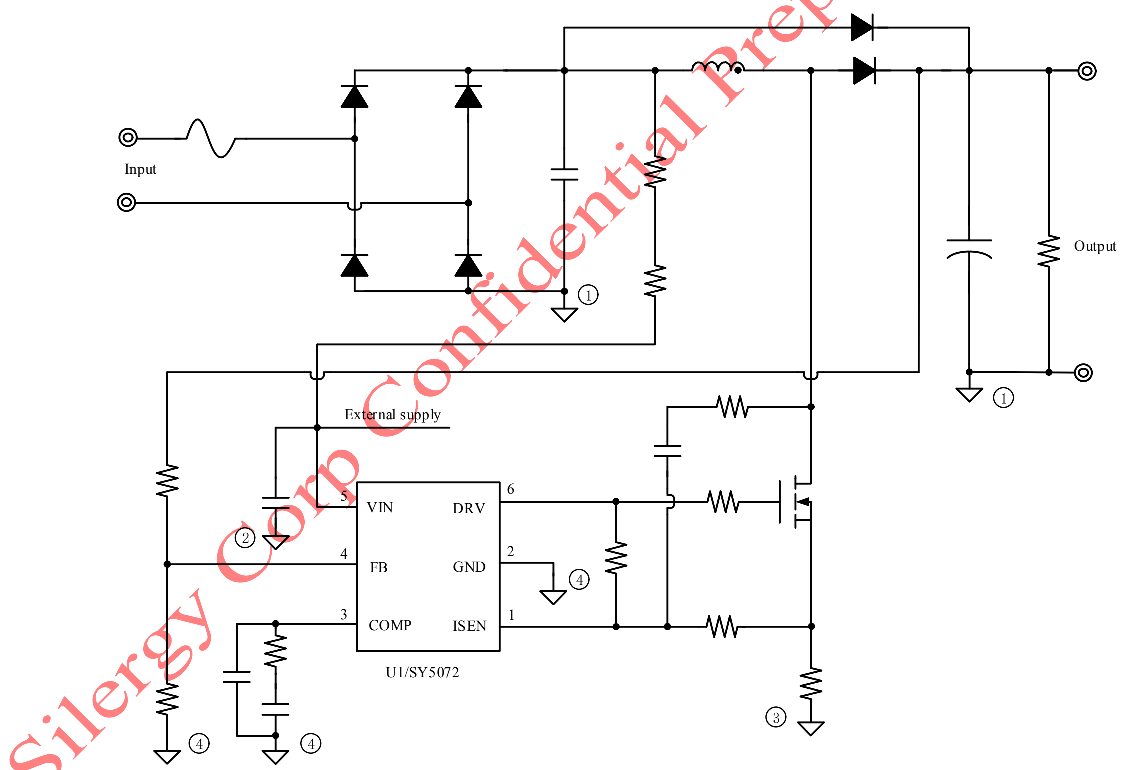


Figure.14 Recommended connection of GND

Design Example

A design example of typical application is shown below step by step.

#1. Identify Design Specification

Design Specification			
V_{AC_MIN}	90VAC	V_{AC_MAX}	264VAC
V_{OUT}	420V	I_{OUT}	140mA
P_{OUT}	60W	η	95%
f_{s_min}	30kHz		

#2. Current calculation （peak and rms value ）

$$I_L(peak)=\frac{2\sqrt{2}\times P_{OUT}}{\eta\times V_{IN\_MIN}}=\frac{2\sqrt{2}\times 60}{0.95\times 90}=1.98A$$

$$I_{L(rms)}=\frac{2\times P_{OUT}}{\sqrt{3}\times\eta\times V_{IN\_MIN}}=\frac{2\times 60}{\sqrt{3}\times 0.95\times 90}=0.81A$$

$$I_{MOSFET(rms)}=\frac{2}{\sqrt{3}}\times\frac{P_{out}}{\eta\times V_{IN\_MIN}}\times\sqrt{1-(\frac{\sqrt{2}\times 8\times V_{IN\_MIN}}{3\times\pi\times V_{OUT}})}=\frac{2}{\sqrt{3}}\times\frac{60}{0.95\times 90}\times\sqrt{1-(\frac{\sqrt{2}\times 8\times 90}{3\times\pi\times 420})}=0.70A$$

$$I_{DIODE(rms)}=\frac{4}{3}\times\frac{P_{OUT}}{\eta\times\sqrt{V_{IN\_MIN}\times V_{OUT}}}\times\sqrt{\frac{2\times\sqrt{2}}{\pi}}=\frac{4}{3}\times\frac{60}{0.95\times\sqrt{90\times 420}}\times\sqrt{\frac{2\times\sqrt{2}}{\pi}}=0.41A$$

$$I_{DIODE(ave)}=I_{OUT}=\frac{P_{OUT}}{V_{OUT}}=\frac{60}{420}=0.14A$$

#3. ISEN resistor

$$R_S=\frac{0.9\times V_{ISEN\_LIMIT}}{I_{L(peak)}}=\frac{0.9\times 0.55}{0.98A}=0.50$$

#4. Inductor Design （N and L）

(a) f_{s_min} is preset to 35kHz ;

(b) Compute inductor L with minimum and maximum input voltage ;

$$L_1=\frac{V_{IN}^2\times(V_{OUT}-\sqrt{2}\times V_{IN})}{2\times f_{sw\_MIN}\times P_{IN}\times V_{OUT}}=\frac{90^2\times(420-\sqrt{2}\times 90)}{2\times 35000\times\frac{60}{0.95}\times 420}=1277uH$$

$$L_1=\frac{V_{IN}^2\times(V_{OUT}-\sqrt{2}\times V_{IN})}{2\times f_{sw\_MIN}\times P_{IN}\times V_{OUT}}=\frac{264^2\times(420-\sqrt{2}\times 264)}{2\times 35000\times\frac{60}{0.95}\times 420}=1751uH$$

Choosing 1200uH for simply calculation.

(c) core selection;

PQ20/20 (PC40) is selected first.

$$N=\frac{L\times\frac{V_{ISEN\_LIMIT}}{R_S}}{Ae\times\Delta B}=\frac{1200\times10^{-6}\times\frac{0.55}{0.5}}{64\times0.32}\approx64$$

(d) wire selection;

According to rms current calculated before, and current density of 5A/mm2, we can get the wire diameter needed.

$$d=\sqrt{\frac{ILrms}{5}\times\frac{4}{\pi}}=\sqrt{\frac{0.81}{5}\times\frac{4}{\pi}}\approx0.45mm$$

So the diameter of wire for inductor is 0.3*2mm.

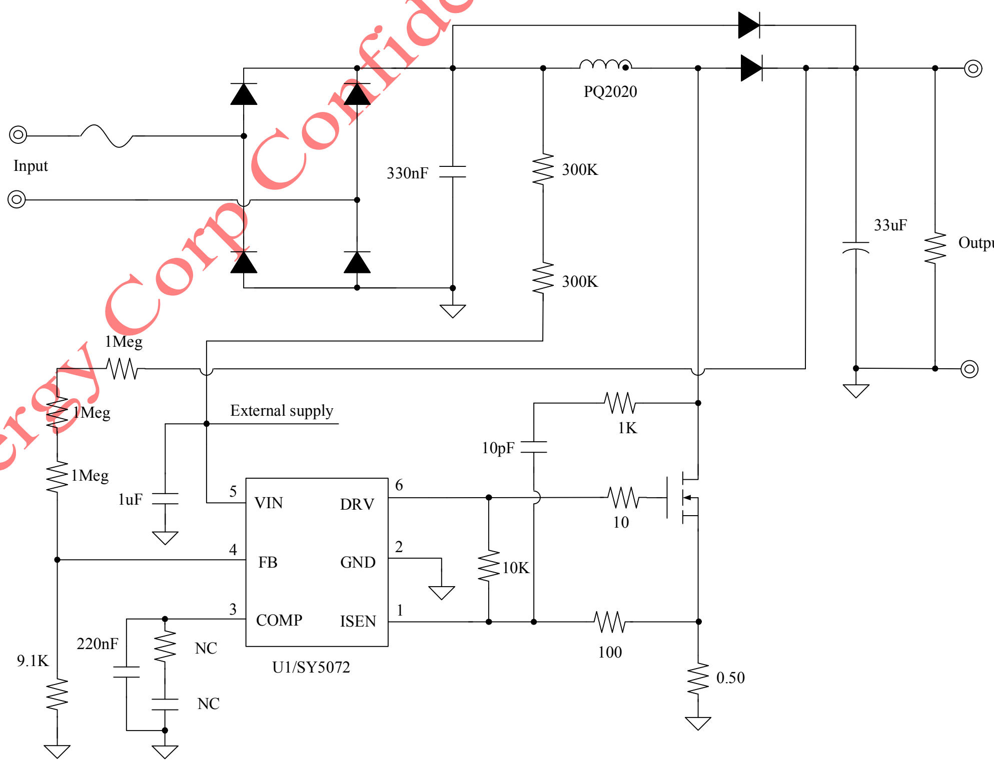
#5. Voltage feedback

R_U is set to 3MΩ to reduce resistor loss. Then R_D is calculated as

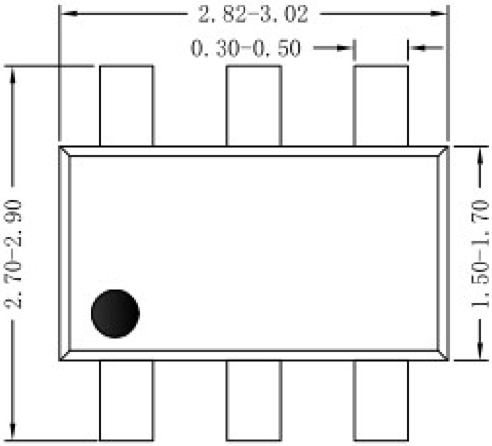
$$R_D=\frac{V_{REF}\times R_U}{V_{OUT}-V_{REF}}=\frac{1.25\times300000}{420-1.25}\approx9.1\text{K}$$

So R_D = 9.1K.

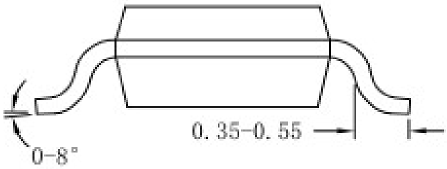
#6. Recommended Schematic and Parameters



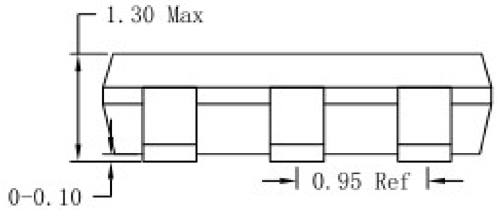
SOT23-6 Package outline & PCB layout design



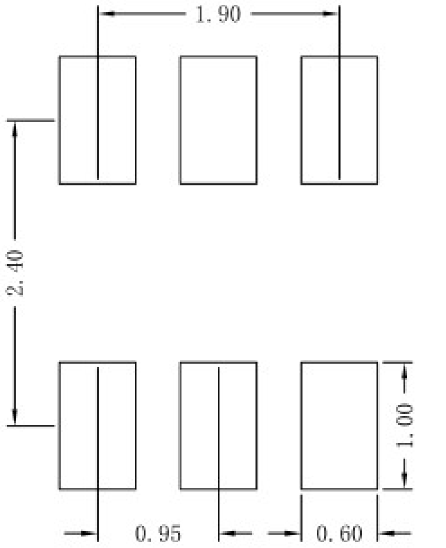
Top View



Side View



Side View



Recommended Pad Layout

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**