

## 2.5V/3.3V, 2.5 GHz Differential Two-Channel Precision CML Delay Line

### Features

- Guaranteed AC Parameters over Temperature:
  - $f_{MAX} > 2.5$  GHz
  - $t_r / t_f < 120$  ps
  - Propagation Delay  $< 384$  ps
- Delay Either Clock or Data
- 50 ps Increments
- $\pm 350$ ps total delay
- Source Terminated CML Outputs
- Fully Differential I/O
- Wide Supply Voltage Range: 2.3V to 3.6V
- Available in a tiny 32-pin EPAD-TQFP package

### Applications

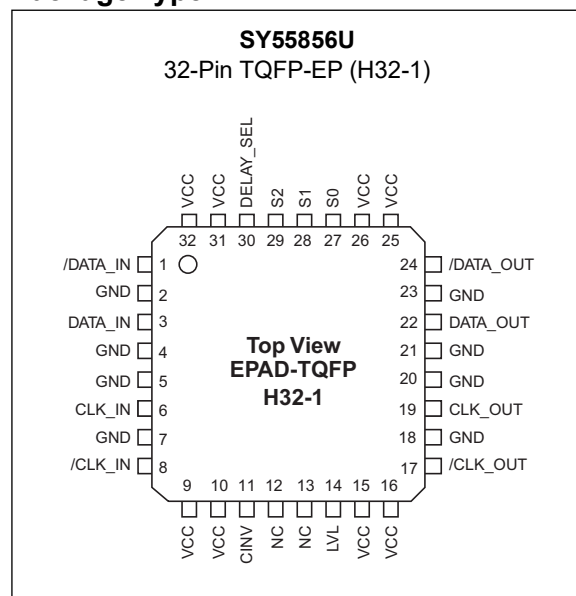
- Data Communication Systems
- Telecom Systems
- High-Speed Backplanes
- Signal De-Skewing
- Pulse Alignment
- Digitally Controlled Delay Lines

### General Description

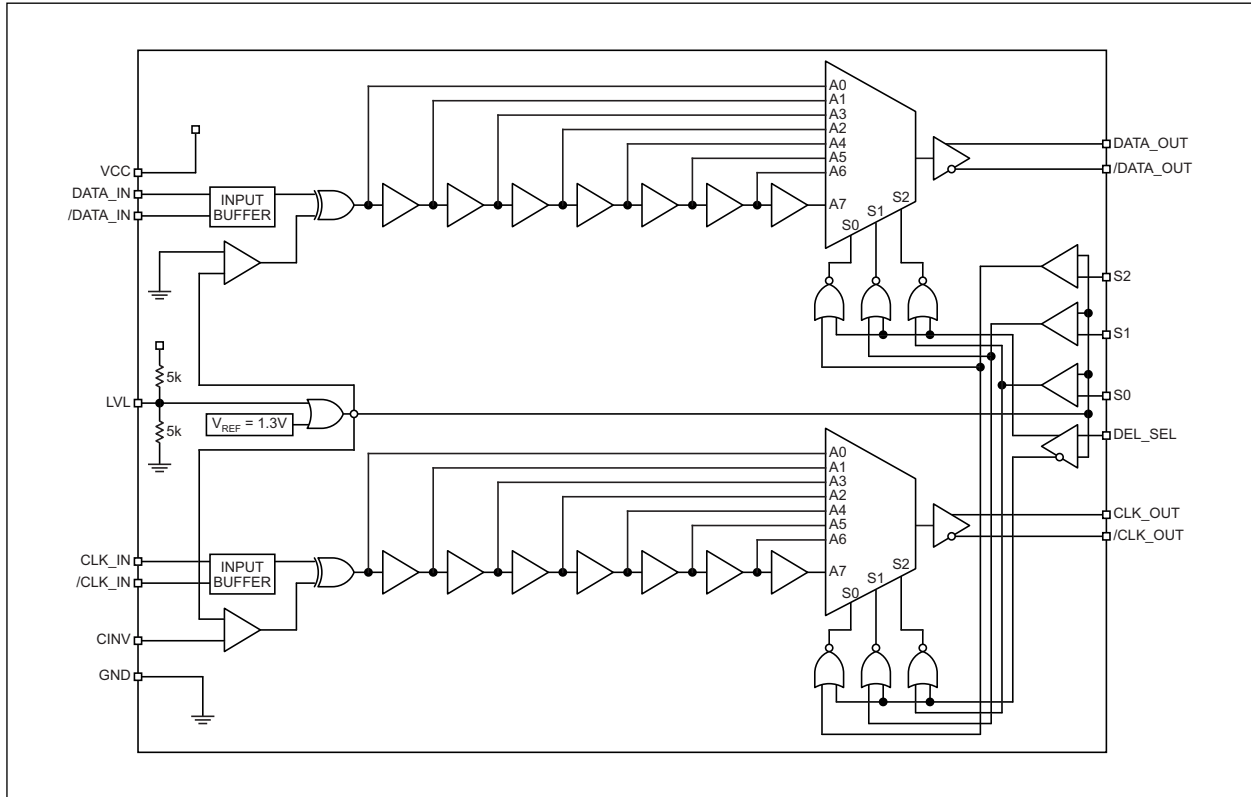
The SY55856U is a 2.5 GHz, two-channel, fully differential CML (Current Mode Logic) delay line. The device is optimized to adjust the relative delay between two channels, such as clock and data, in 50 ps increments. Both inputs may be adjusted in either direction in seven increments of 50 ps, for a total adjustment range of  $\pm 350$  ps. In addition, the clock input maybe inverted through the CINV control pin.

The SY55856U inputs are designed to accept single-ended or differential CML signals. The differential CML outputs are optimized for 50 $\Omega$  loads (50 $\Omega$  source terminated), thus only requires a single 100 $\Omega$  resistor across the output pair. Output rise and fall time is an extremely fast 110 ps (max) and the differential swing is 400 mV. The maximum throughput of the SY55856U is guaranteed to exceed 2.5 GHz (5 Gbps).

### Package Type



## Functional Block Diagram



## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

Power Supply Voltage, $V_{CC}$ .....	-0.5V to +6.0V
Input Voltage, $V_{IN}$ .....	-0.5V to $V_{CC}$ +5.0V
CML Output Voltage, $V_{OUT}$ .....	-0.5V to $V_{CC}$ +5.0V

† **Notice:** Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

### DC CHARACTERISTICS

Electrical Characteristics: $V_{CC}$ = 2.3V to 3.6V; GND = 0V; $T_A$ = -40°C to +85°C unless otherwise stated.						
Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Voltage	$V_{CC}$	2.3	—	3.6	V	—
Power Supply Current	$I_{CC}$	—	115	140	mA	No Load
<b>VT Inputs Note 1</b>						
Analog Input	$V_{ILVL}$	$V_{TCL}$	—	$V_{CC} - 0.1$	V	Note 2
VT Input High Voltage	$V_{IHVT}$	$V_{SW} + 0.1$	—	$V_{CC}$	V	Note 3, Note 4
VT Input Low Voltage	$V_{ILVT}$	0.0	—	$V_{SW} - 0.1$	V	Note 3, Note 4
Input Switching Threshold Differential Voltage	$V_{IST}$	100	50	—	mV	Note 5
Threshold Clamp Voltage	$V_{TCL}$	1.2	—	1.4	V	—

**Note 1:** DC parameters are guaranteed after thermal equilibrium has been established.

- 2:** The LVL input determines the voltage switching threshold that differentiates logic high from logic low for the VT inputs S0, S1, S2, DELAY\_SEL, and CINV. LVL may be driven to  $V_{CC}$ , but this is not useful, as the VT inputs could then not get high enough to reliably indicate logic high. Also, as shown in Figure 3, the LVL input internally clamps at  $V_{TCL}$ . If LVL is left unconnected, the VT inputs will switch at about the maximum of  $(V_{CC} + GND)/2$  ( $= V_{CC}/2$ ) and  $V_{TCL}$ .
- 3:** VT inputs are S0, S1, S2, DELAY\_SEL, and CINV.
- 4:**  $V_{SW}$  is the threshold switching voltage. It is equal to the voltage at the LVL pin, when this voltage is above  $V_{TCL(MAX)}$ .  $V_{SW}$  is some value between  $V_{TCL(MIN)}$  and  $V_{TCL(MAX)}$  when the voltage at the LVL pin is below  $V_{TCL(MAX)}$ .
- 5:**  $V_{IST}$  is the voltage difference needed to guarantee a stable logic level. Logic high must be at least  $V_{IST}$  above  $V_{SW}$ . Logic low must be at most  $V_{IST}$  below  $V_{SW}$ . Thus, the minimum input swing on a given VT input pin, that is,  $|V_{IHVT} - V_{ILVT}|$ , must be at least  $2 \times V_{IST}$ .

## CML DC CHARACTERISTICS

Electrical Characteristics: $V_{CC} = 2.3V$ to $3.6V$ ; $GND = 0V$ ; $T_A = -40^{\circ}C$ to $+85^{\circ}C$ unless otherwise stated.						
Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Differential Input Voltage	$V_{ID}$	100	—	—	mV	—
Input High Voltage	$V_{IH}$	1.6	—	$V_{CC}$	V	—
Input Low Voltage	$V_{IL}$	1.5	—	$V_{IH} - 0.1$	V	—
Output High Voltage	$V_{OH}$	$V_{CC} - 0.040$	$V_{CC} - 0.010$	$V_{CC}$	V	No Load
Output Low Voltage	$V_{OL}$	$V_{CC} - 1.00$	$V_{CC} - 0.800$	$V_{CC} - 0.65$	V	No Load
Output Voltage Swing <a href="#">Note 1</a>	$V_{OUT}$ (Swing)	0.650	0.800	1.00	V	No Load
		—	0.400	—		50 $\Omega$ Environment
Output Source Impedance (CLK_OUT, /CLK_OUT and DATA_OUT, /DATA_OUT)	$R_{OUT}$	40	50	60	$\Omega$	—

**Note 1:**  $V_{OUT(SWING)}$  is defined as the swing on one output of a differential pair, that is  $|V_{OH} - V_{OL}|$  on one pin. The swing for common mode noise immunity purposes is  $2 \times V_{OUT(SWING)}$ . Actual voltage levels and differential swing will depend on customer termination scheme. Typically, a 400 mV swing is available in a 50 $\Omega$  environment. Refer to [Figure 4-1](#) for more details.

## AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{CC} = 2.3V$ to $3.6V$ ; $GND = 0V$ ; $T_A = -40^{\circ}C$ to $85^{\circ}C$ , unless otherwise stated. (Note 1)						
Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Maximum Frequency	$f_{MAX}$	2.5	—	—	GHz	—
Delay Step Size	$\Delta t$	36	—	52	ps	—
Delay Line Insertion Delay	$t_{PLH}, t_{PHL}$	232	—	384	ps	Note 2
Delay Line Range	$t_{DELAY}$	250	—	365	ps	$T_A = -40^{\circ}C$
		290	—	420		$T_A = +25^{\circ}C$
		335	—	465		$T_A = +85^{\circ}C$
Output Jitter	$t_{JITTER}$	—	—	<1	ps <sub>RMS</sub>	—
Delay Line Duty Cycle Skew ( $t_{PLH} - t_{PHL}$ )	$t_{SKEW}$	—	—	50	ps	—
Duty Cycle	DC	45	—	55	%	—
CML Output Rise/Fall time (20% to 80%)	$t_r/t_f$	—	—	100	ps	$T_A = -40^{\circ}C$
		—	—	110		$T_A = +25^{\circ}C$
		—	—	120		$T_A = +85^{\circ}C$

**Note 1:** Tested using the 50 $\Omega$  load, as shown in Figure 4-1.

**2:** Delay line insertion delay is the minimum input-to-output delay with select control set to S2:S0 = 0 for CLK\_OUT and S2:S0 = 7 for DATA\_OUT. This resulting delay is the inherent propagation delay.

## TEMPERATURE SPECIFICATIONS

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
<b>Temperature Ranges</b>						
Operating Temperature Range	$T_A$	-40	—	+85	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 20 sec.
Storage Temperature Range	$T_S$	-55	—	+125	°C	—
<b>Package Thermal Resistance (Note 1)</b>						
Thermal Resistance, 7x7 TQFP-EP-32Lead	$\theta_{JA}$	—	28	—	°C/W	Still-Air
			20			500 lpm
	$\theta_{JC}$	—	4	—	°C/W	Junction-to-case

**Note 1:** Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.  $\psi_{JB}$  and  $\theta_{JA}$  values are determined for a 4-layer board in still-air number, unless otherwise stated.

## 2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 2-1](#).

**TABLE 2-1: PIN FUNCTION TABLE**

Pin Number	Pin Name	Description
1, 3	/DATA_IN, DATA_IN	CML Input (Differential). This is one of the CML inputs, the data in signal. A delayed version of this signal appears at DATA_OUT, /DATA_OUT.
2, 4, 5, 7, 18, 20, 21, 23	GND	Ground.
22, 24	/DATA_OUT, DATA_OUT	CML Output (Differential). This is one of the CML outputs, the data output. It is a delayed version of DATA_IN, /DATA_IN.
6, 8	CLK_IN, /CLK_IN	CML Input (Differential). This is one of the differential CML inputs, the clock in signal. A delayed version of this input appears at CLK_OUT, /CLK_OUT.
17, 19	CLK_OUT, /CLK_OUT	CML Output (Differential). This is one of the CML outputs, the clock output. It is a delayed, copy of CLK_IN, /CLK_IN.
9, 10, 15, 16 25, 26, 31, 32	VCC	Power supply.
11	CINV	VT Input (Single Ended). This is the clock inversion select signal. This input optionally inverts the CLK_IN, /CLK_IN signal which results in an inverted CLK_OUT, /CLK_OUT. A voltage below the VT threshold results in no inversion. A voltage above the threshold value results in an inversion from the clock input to the clock output. Refer to the <a href="#">VT (Variable Threshold) Inputs</a> section.
14	LVL	Analog Input. This input determines what level differentiates logic high from logic low. This input affects the behavior of the CINV, S0, S1 and S2 inputs. Please refer to the <a href="#">VT (Variable Threshold) Inputs</a> section for more details. For the control interface, see <a href="#">Figure 3-3</a> . For TTL control interface, see <a href="#">Figure 3-4</a> .
30	DELAT_SEL	VT Input (Single Ended). CML compatible control logic. This is the delay path control input. Logic high delays the clock signal with respect to the data signal. A logic low delays the data signal with respect to the clock signal. Inputs S2, S1 and S0 control amount of delay.
27, 28, 29	S0, S1, S2	VT Input (Single Ended). CML compatible control logic. This is the delay selection control input. These three bits define how much relative delay will occur between the data and clock signals, as per the truth table shown in <a href="#">Table 2-3</a> . For the control logic interface, see <a href="#">Figure 3-3</a> . For TTL control interface, see <a href="#">Figure 3-4</a> . S0 = LSB.
12, 13	NC	No connect.

## TRUTH TABLES

TABLE 2-2: INPUT TO OUTPUT CONNECTIVITY

DATA_IN	CLK_IN	CINV	DATA_OUT	/DATA_OUT	CLK_OUT	/CLK_OUT
0	0	0	0	1	0	1
0	0	1	0	1	1	0
0	1	0	0	1	1	0
0	1	1	0	1	0	1
1	0	0	1	0	0	1
1	0	1	1	0	1	0
1	1	0	1	0	1	0
1	1	1	1	0	0	1

TABLE 2-3: NOMINAL DIFFERENTIAL DELAY VALUES

S2	S1	S0	DATA_OUT (D_SEL = 0) (ps)	/DATA_OUT (D_SEL = 1) (ps)
0	0	0	350	0
0	0	1	300	50
0	1	0	250	100
0	1	1	200	150
1	0	0	150	200
1	0	1	100	250
1	1	0	50	300
1	1	1	0	350

**Note:** Table 2-3 defines the approximate relative delay between the two paths. For example, if S2, S1, S0 = 000 and an edge appears at CLK\_IN at the same instant as an edge appears at DATA\_IN, then an edge at CLK\_OUT will appear about 350 ps earlier than an edge at DATA\_OUT. That is, negative values imply CLK\_OUT being shifted early with respect to DATA\_OUT. Likewise, a positive value in the third column implies that CLK\_OUT is shifted late with respect to DATA\_OUT. Please consult the [AC Electrical Characteristics](#) section for more precise delay values.



## 3.0 FUNCTIONAL DESCRIPTION

### 3.1 Establishing Static Logic Inputs

The true pin of a CML input pair is internally biased to ground through a 75 kΩ resistor. The complement pin of a CML input pair is internally biased halfway between  $V_{CC}$  and ground by a voltage divider consisting of two 75 kΩ resistors. To keep a CML input at static logic zero at  $V_{CC} > 3.0V$ , leave both inputs unconnected. For  $V_{CC} \leq 3.0V$ , connect the complement input to  $V_{CC}$  and leave the true input unconnected. To make an input static logic one, connect the true input to  $V_{CC}$ , and leave the complement input unconnected. These are the only safe ways to cause CML inputs to be at a static value. In particular, no CML input should be directly connected to ground. All NC pins in the figures below should be left unconnected.

### 3.2 VT (Variable Threshold) Inputs

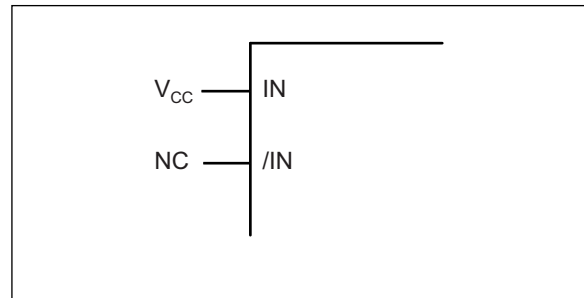
Five inputs to SY55856U, CINV, DELAY\_SEL, S0, S1, and S2, are variable threshold inputs. The LVL input determines the Voltage threshold that differentiates logic high from logic low for these five inputs only. If LVL is left unconnected, the VT inputs will switch at about:

**EQUATION 3-1:**

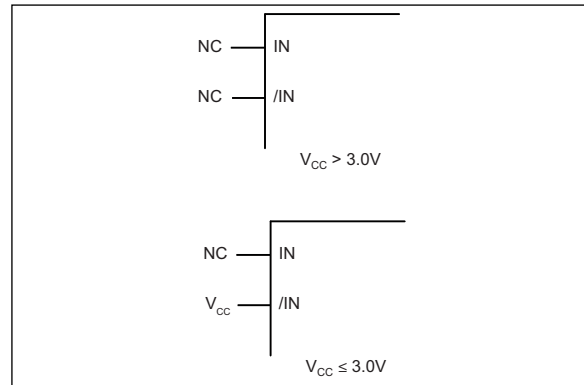
$$\frac{V_{CC} + GND}{2}$$

or  $V_{TCL}$ , whichever is higher. To obtain a logic switching threshold different from this, the LVL input must be driven with the actual desired threshold voltage. The user may drive the LVL pin with any voltage between  $V_{CC} - 0.1V$  and ground. For example, driving LVL with a voltage set at  $V_{CC} - 0.1V$  causes the VT inputs to accept single ended PECL outputs and switch appropriately.

Note that VT inputs are internally clamped so that the threshold will not fall below  $V_{TCL}$  Volts. Since driving the LVL input to ground causes the threshold to be somewhere between  $V_{TCL(MIN)}$  and  $V_{TCL(MAX)}$ , it is expected that the user will keep the Voltage at the LVL pin at or above  $V_{TCL(MAX)}$ . Please refer to [Figure 3-3](#) for clarification.

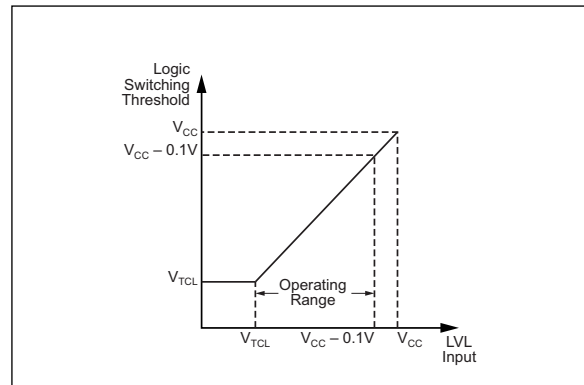


**FIGURE 3-1:** Hard Wiring a Logic "1".

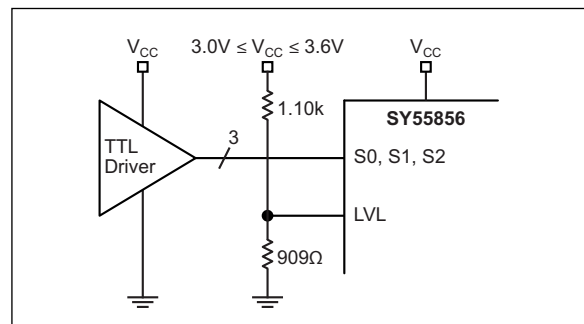


**FIGURE 3-2:** Hard Wiring Logic "0".

**Note:** For [Figure 3-1](#) & [Figure 3-2](#), IN is either the DATA\_IN or the CLK\_IN input. /IN is either the /DATA\_IN or /CLK\_IN input.



**FIGURE 3-3:** Logic Switching Threshold.

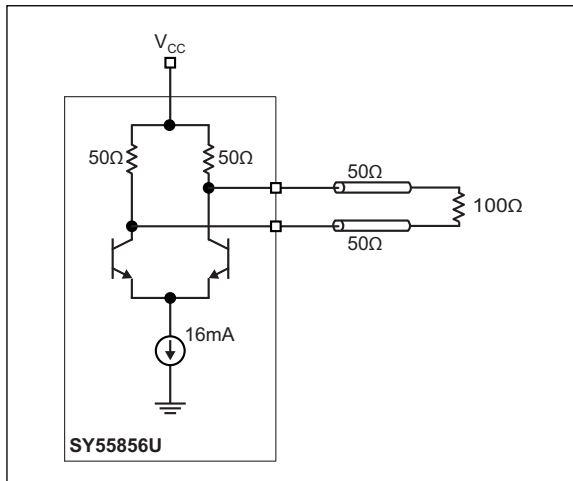


**FIGURE 3-4:** Interfacing TTL-to-CML Select (CINV, DELAY\_SEL, S0, S1, S2).

## 4.0 CML TERMINATION

All CML inputs accept a CML output from any other member of this family. All CML outputs are source terminated  $50\Omega$  differential drivers as shown in [Figure 4-1](#). SY55856U expects its inputs to be externally terminated.

SY55856U inputs are designed to accept a termination resistor between the true and complement inputs of a CML differential input pair, as shown in [Figure 4-1](#).

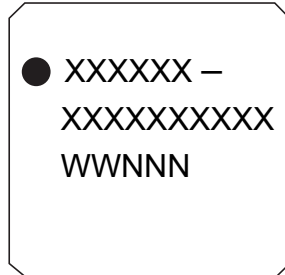


**FIGURE 4-1:**  $50\Omega$  Load CML Output.

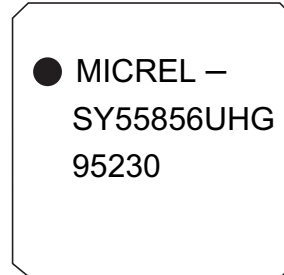
## 5.0 PACKAGING INFORMATION

### 5.1 Package Marking Information

32-Lead TQFP\*



Example



<b>Legend:</b>	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
<b>Note:</b>	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (¯) and/or Overbar (˘) symbol may not be to scale.	

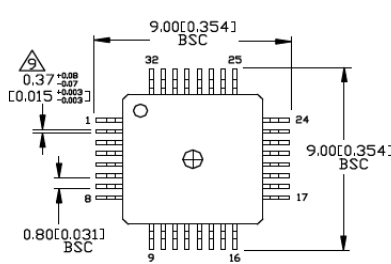
## 32-Lead TQFP-EP Package Outline and Recommended Land Pattern

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

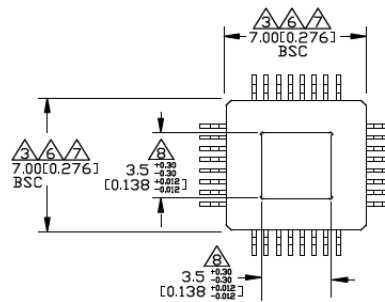
**TITLE**

32 LEAD TQFP 7X7 mm EPAD PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

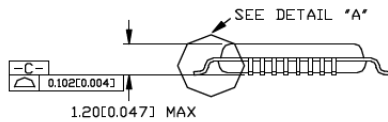
<b>DRAWING #</b>	TQFP7X7-32LD-PL-1	<b>UNIT</b>	MM [INCH]
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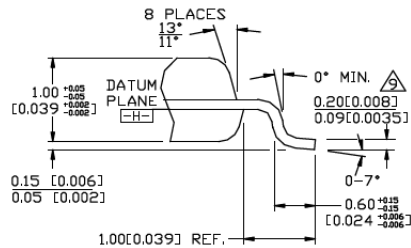
TOP VIEW



BOTTOM VIEW



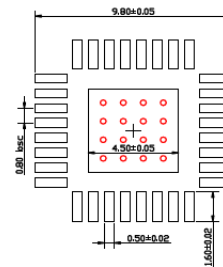
SIDE VIEW



DETAIL "A"

**NOTES:**

1. DIMENSIONS ARE IN MM(INCHES).
2. CONTROLLING DIMENSION: MM.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.254 [0.010].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN.
6. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE [H].
7. PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.
8. EXPOSED PAD SHALL BE COPLANAR WITH PACKAGE BOTTOM WITHIN 0.05mm.
9. EXPOSED PAD: Cu WITH Sn/Pb PLATING.
10. DIMENSION INCLUDES LEAD FINISH.
11. RED CIRCLES IN LAND PATTERN REPRESENT THERMAL VIAS. RECOMMENDED SIZE IS 0.30MM DIAMETER, CONNECT TO GND.



RECOMMENDED LAND PATTERN

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

## APPENDIX A: REVISION HISTORY

### Revision A (October 2023)

- Converted Micrel document SY55856U to Microchip data sheet template DS20006334A.
- Minor text changes throughout.

NOTES:

## PRODUCT IDENTIFICATION SYSTEM

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<u>PART #.</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>XX</u>	
Device	Supply Voltage Range	Package	Junction Temperature Range	Special Processing	
<b>Device:</b> SY55856: 2.5V/3.3V, 2.5 GHz Differential Two-Channel Precision CML Delay Line					<b>Examples:</b> a) SY55856UHG: SY55856, 2.5V/3.3V Output Voltage, 32-Lead TQFP-EP, -40°C to +85°C Temperature Range, 250/Tray
<b>Supply Voltage:</b> U = 2.5V/3.3V					<b>Note 1:</b> Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
<b>Package:</b> H = 32-Lead TQFP-EP					
<b>Temperature Range:</b> G = -40°C to +85°C (NiPdAu Lead Free)					
<b>Special Processing:</b> <blank>= 250/Tray					

NOTES:



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