



## FEATURES

- Precision 1:2, 400mV LVPECL fanout buffer
- Low jitter performance:
  - 55fs<sub>RMS</sub> phase jitter (typ)
- Accepts an input signal as low as 100mV
- Guaranteed AC performance over temperature and voltage:
  - >6GHz f<sub>MAX</sub> clock
  - <80ps t<sub>r</sub>/t<sub>f</sub> times
  - <250ps t<sub>pd</sub>
  - <15ps max. skew
- Unique input termination and V<sub>T</sub> pin accepts DC-coupled and AC-coupled differential inputs: LVPECL, LVDS and CML
- 400mV LVPECL compatible outputs
- Power supply 2.5V ±5% and 3.3V ±10%
- -40°C to +85°C temperature range
- Available in 16-pin (3mm x 3mm) QFN package



Precision Edge®

## DESCRIPTION

The SY58013U is a 2.5V/3.3V precision, high-speed, fully differential 1:2 LVPECL fanout buffer. Optimized to provide two identical output copies with less than 15ps of skew and only 55fs<sub>RMS</sub> phase jitter, the SY58013U can process clock signals as fast as 6GHz or data patterns up to 10.7Gbps.

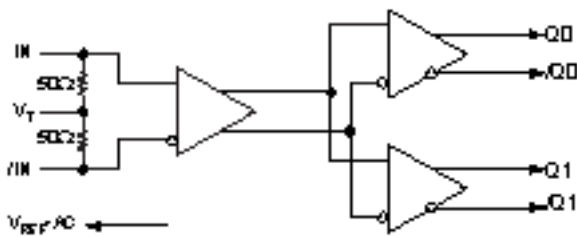
The differential input includes Micrel's unique, 3-pin input termination architecture that interfaces to LVPECL, LVDS, and CML differential signals, (AC- or DC-coupled) as small as 100mV without any level-shifting or termination resistor networks in the signal path. For AC-coupled input interface applications, an on-board output reference voltage (V<sub>REF-AC</sub>) is provided to bias the V<sub>T</sub> pin. The outputs are 400mV LVPECL compatible, with extremely fast rise/fall times guaranteed to be less than 80ps.

The SY58013U operates from a 2.5V ±5% supply or 3.3V ±10% supply and is guaranteed over the full industrial temperature range (-40°C to +85°C). For applications that require greater output swing or CML compatible outputs, consider the SY58012U 1:2 fanout buffer with 800mV LVPECL outputs, or the SY58011U 1:2 fanout buffer with 400mV CML outputs. The SY58013U is part of Micrel's high-speed, Precision Edge® product line. Datasheets and support documentation can be found on Micrel's web site at [www.micrel.com](http://www.micrel.com).

## APPLICATIONS

- All SONET and All GigE clock distribution
- Fibre Channel clock and data distribution
- Backplanes
- Data distribution: OC-48, OC-48+FEC, XAU1
- High-end, low-skew, multiprocessor synchronous clock distribution

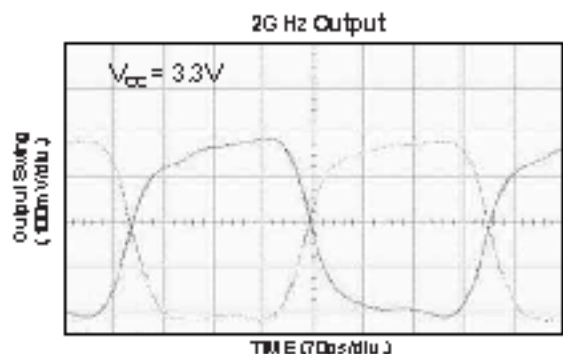
## FUNCTIONAL BLOCK DIAGRAM



United States Patent No. RE44,134

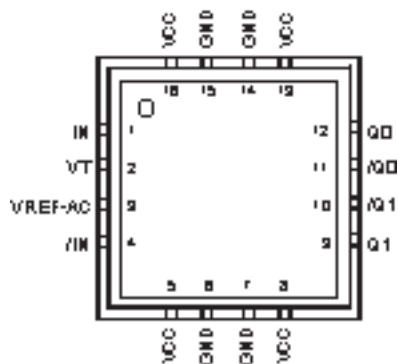
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## TYPICAL PERFORMANCE



2GHz with 100mV Input

**PACKAGE/ORDERING INFORMATION**



**16-Pin QFN**

**Ordering Information<sup>(1)</sup>**

Part Number	Package Type	Operating Range	Package Marking
SY58013UMG <sup>(3)</sup>	QFN-16 Pb-Free	Industrial	013U with Pb-Free bar-line indicator
SY58013UMGTR <sup>(2, 3)</sup>	QFN-16 Pb-Free	Industrial	013U with Pb-Free bar-line indicator

**Notes:**

1. Contact factory for die availability. Dice are guaranteed at  $T_A = 25^\circ\text{C}$ , DC electricals only. All devices are Pb-Free.
2. Tape and Reel.
3. Pb-Free package recommended for new designs.

**PIN DESCRIPTION**

Pin Number	Pin Name	Pin Function
1, 4	IN, /IN	Differential Input: This input pair is the signal to be buffered. Each pin is internally terminated with 50 ohms to the $V_T$ pin. Note that this input will default to an indeterminate state if left open. See <i>"Input Interface Applications"</i> section.
2	VT	Input Termination Center-Tap: Each input terminates to this pin. The $V_T$ pin provides a center-tap for each input (IN, /IN) to a termination network for maximum interface flexibility. See <i>"Input Interface Applications"</i> section.
3	VREF-AC	Reference Output Voltage: This output biases to $V_{CC} - 1.2\text{V}$ . It is used for AC-coupled inputs (IN, /IN). Connect $V_{REF-AC}$ directly to the $V_T$ pin. Bypass with $0.01\mu\text{F}$ low ESR capacitor to $V_{CC}$ . Maximum current source or sink is 0.5mA. See <i>"Input Interface Applications"</i> section.
5, 8, 13, 16	VCC	Positive Power Supply: Bypass with $0.1\mu\text{F}/0.01\mu\text{F}$ low ESR capacitors as close to the $V_{CC}$ pins as possible.
6, 7, 14, 15	GND, (Exposed Pad)	Ground. Exposed pad must be connected to a ground plane that is the same potential as the ground pin.
12, 11 9, 10	Q0, /Q0, Q1, /Q1	LVPECL Differential Output Pairs: Differential buffered output copy of the input signal. The output swing is typically 400mV. Unused output pairs may be left floating with no impact on jitter. See <i>"LVPECL Output Termination"</i> section.

**Absolute Maximum Ratings**(Note 1)

Power Supply Voltage ( $V_{CC}$ ) ..... -0.5V to +4.0V  
 Input Voltage ( $V_{IN}$ ) ..... -0.5V to  $V_{CC}$   
 Output Current ( $I_{OUT}$ )  
     Continuous ..... 50mA  
     Surge ..... 100mA  
 $V_T$  Current  
     Source or sink current on  $V_T$  pin .....  $\pm 100$ mA  
 Input Current  
     Source or sink current on (IN, /IN) .....  $\pm 50$ mA  
 $V_{REF}$  Current  
     Source or sink current on  $V_{REF-AC}$ , **Note 4** .....  $\pm 1.5$ mA  
 Soldering, (20 sec.) ..... 260°C  
 Storage Temperature Range ( $T_{STORE}$ ) ..... -65 to +150°C

**Operating Ratings**(Note 2)

Power Supply Voltage ( $V_{CC}$ ) ..... +2.375V to +3.60V  
 Operating Temperature Range ( $T_A$ ) ..... -40°C to +85°C  
 Package Thermal Resistance, **Note 3**  
     QFN ( $\theta_{JA}$ )  
         Still-Air ..... 60°C/W  
         500lpfm ..... 54°C/W  
     QFN ( $\psi_{JB}$ ) ..... 33°C/W

**DC ELECTRICAL CHARACTERISTICS**(Note 5)

$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{CC}$	Power Supply Voltage		2.375		3.60	V
$I_{CC}$	Power Supply Current	Max. $V_{CC}$ , no load		75	90	mA
$V_{IH}$	Input HIGH Voltage	IN, /IN, Note 6	$V_{CC}-1.6$		$V_{CC}$	V
$V_{IL}$	Input LOW Voltage	IN, /IN	0		$V_{IH}-0.1$	V
$V_{IN}$	Input Voltage Swing	IN, /IN; see Figure 1a	0.1		1.7	V
$V_{DIFF\_IN}$	Differential Input Voltage	IN, /IN; see Figure 1b	0.2			V
$R_{IN}$	In to $V_T$ Resistance		40	50	60	ohms
$V_{REF-AC}$	Output Reference Voltage		$V_{CC}-1.3$	$V_{CC}-1.2$	$V_{CC}-1.1$	V
IN to $V_T$					1.28	V

**LVPECL DC ELECTRICAL CHARACTERISTICS**(Note 5)

$V_{CC} = 3.3V \pm 10\%$  or  $V_{CC} = 2.5 \pm 5\%$ ;  $R_L = 50\text{ohms}$  to  $V_{CC}-2V$ ;  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ , unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{OH}$	Output HIGH Voltage	Q0, /Q0, Q1, /Q1	$V_{CC}-1.145$	$V_{CC}-1.020$	$V_{CC}-0.895$	V
$V_{OL}$	Output LOW Voltage	Q0, /Q0, Q1, /Q1	$V_{CC}-1.545$	$V_{CC}-1.420$	$V_{CC}-1.295$	V
$V_{OUT}$	Output Voltage Swing	Q0, /Q0, Q1, /Q1; see Figure 1a	200	400		mV
$V_{DIFF\_OUT}$	Differential Output Voltage Swing	Q0, /Q0, Q1, /Q1; see Figure 1b	400	800		mV

- Note 1.** Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
- Note 2.** The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
- Note 3.** Thermal performance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.
- Note 4.** Due to the limited drive capability, use for input of the same package only.
- Note 5.** The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
- Note 6.**  $V_{IH}$  (min) not lower than 1.2V.

**AC ELECTRICAL CHARACTERISTICS(**Note 7)

$V_{CC} = 2.5V \pm 5\%$  or  $3.3V \pm 10\%$ ;  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ ;  $R_L = 50ohms$  to  $V_{CC}-2V$ , unless otherwise stated.

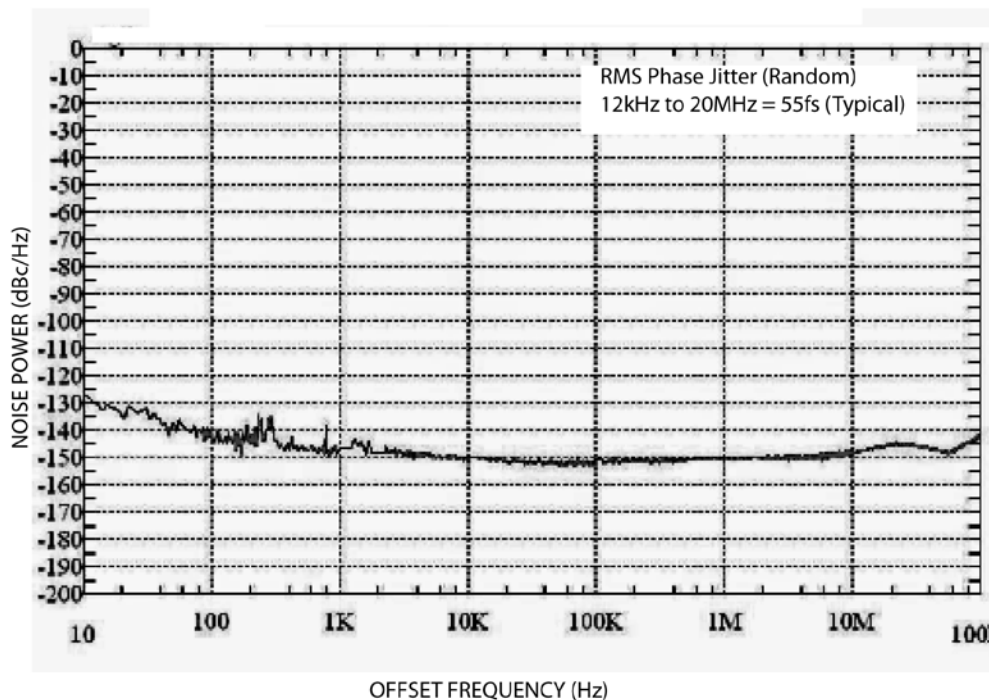
Symbol	Parameter	Condition	Min	Typ	Max	Units
$f_{MAX}$	Maximum Operating Frequency	NRZ Data		10		Gbps
		$V_{OUT} \times 200mV$ Clock	6			GHz
$t_{pd}$	Propagation Delay	$V_{IN} \times 100mV$	100	180	250	ps
$t_{CHAN}$	Channel-to-Channel Skew	<b>Note 8</b>		4	15	ps
$t_{SKEW}$	Part-to-Part Skew	<b>Note 9</b>			100	ps
$t_{JITTER}$	Random Jitter	Output = 622MHz Integration Range: 12kHz-20MHz		55		fs
$t_r, t_f$	Output Rise/Fall Time	20% to 80%, at full output swing	20	50	80	ps

**Note 7.** High frequency AC electricals are guaranteed by design and characterization.

**Note 8.** Skew is measured between outputs of the same bank under identical transitions.

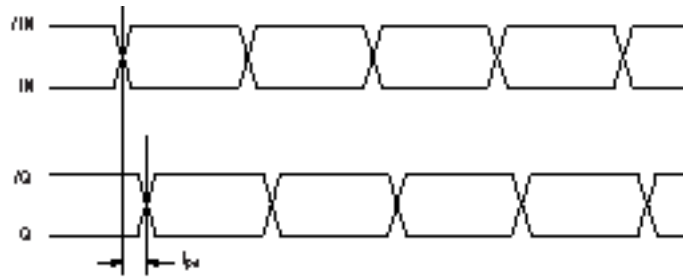
**Note 9.** Skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.

**PHASE NOISE**



Phase Noise Plot: 622MHz @ 3.3V

**TIMING DIAGRAM**



**SINGLE-ENDED AND DIFFERENTIAL SWINGS**

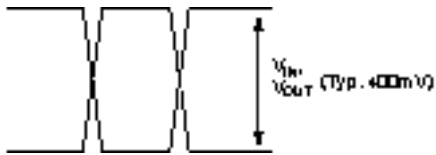


Figure 1a. Single-Ended Voltage Swing

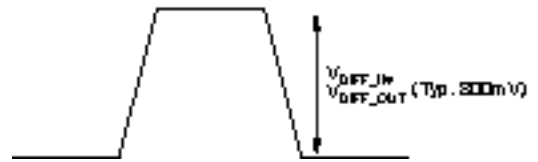
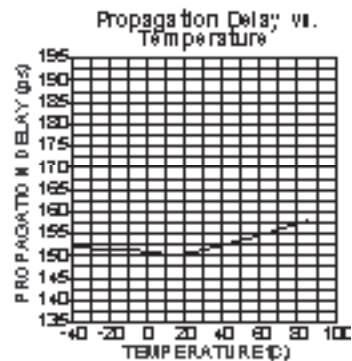
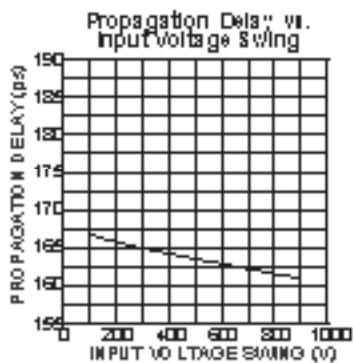
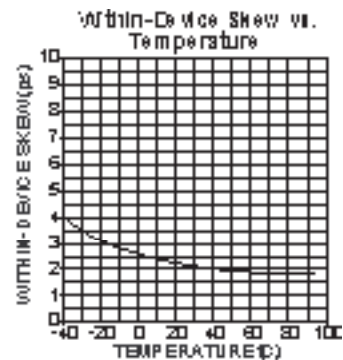
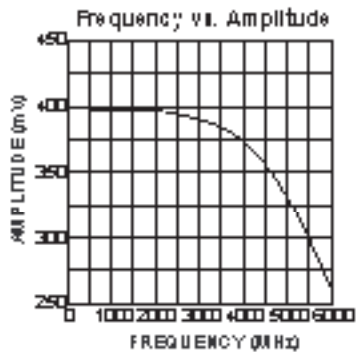


Figure 1b. Differential Voltage Swing

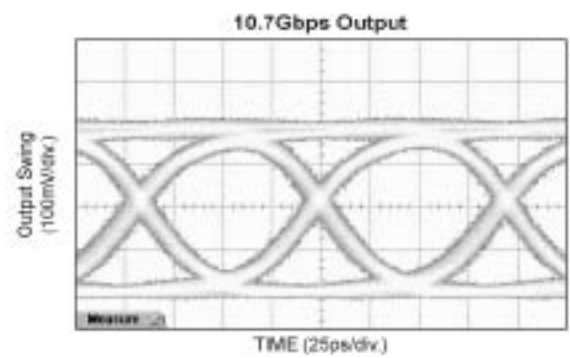
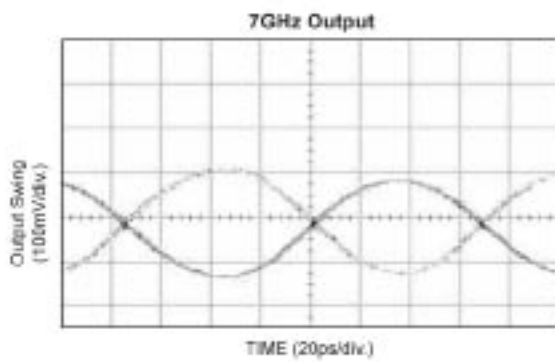
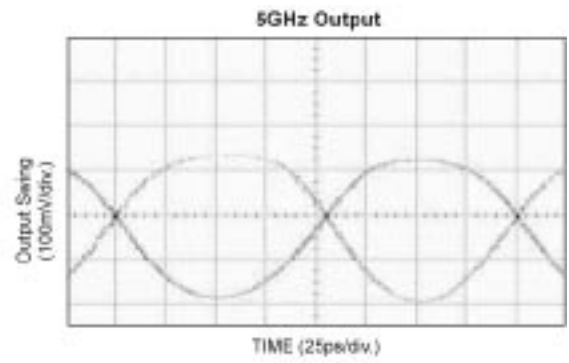
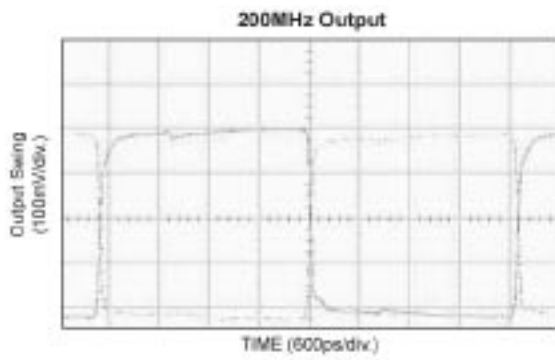
**TYPICAL OPERATING CHARACTERISTICS**

$V_{CC} = 3.3V$ ,  $GND = 0$ ,  $V_{IN} = 100mV$ ,  $T_A = 25^\circ C$ , unless otherwise stated.



# FUNCTIONAL CHARACTERISTICS

$V_{CC} = 3.3V$ ,  $V_{EE} = 0V$ ,  $V_{IN} = 100mV$ ,  $T_A = 25^{\circ}C$ , unless otherwise stated.



( $2^{23}-1$  PRBS Pattern)

**INPUT STAGE**

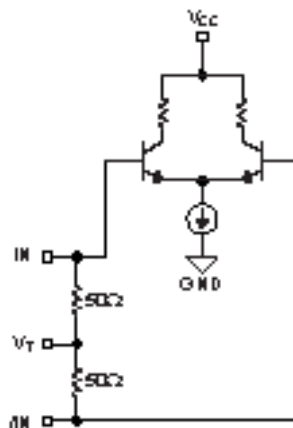


Figure 2. Simplified Differential Input Buffer

**INPUT INTERFACE APPLICATIONS**

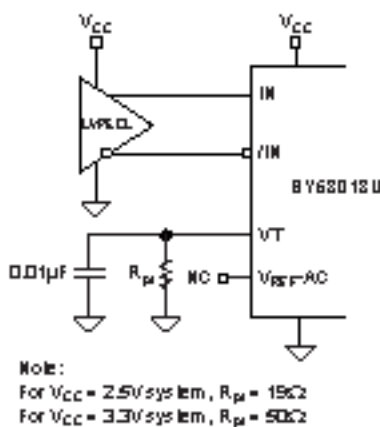


Figure 3a. DC-Coupled LVPECL Input Interface

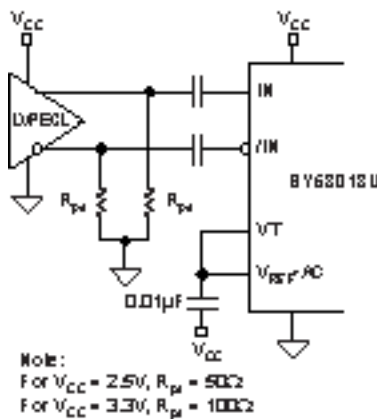


Figure 3b. AC-Coupled LVPECL Input Interface

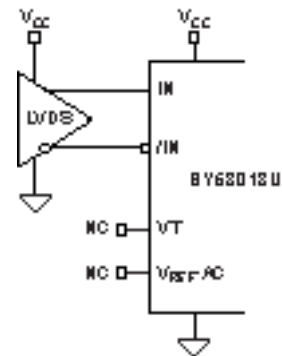


Figure 3c. LVDS Input Interface

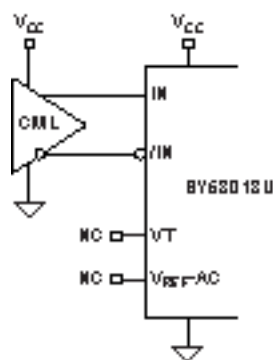


Figure 3d. DC-Coupled CML Input Interface  
(option: may connect  $V_T$  to  $V_{CC}$ )

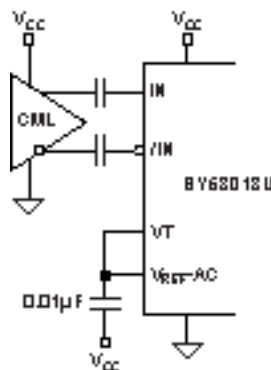
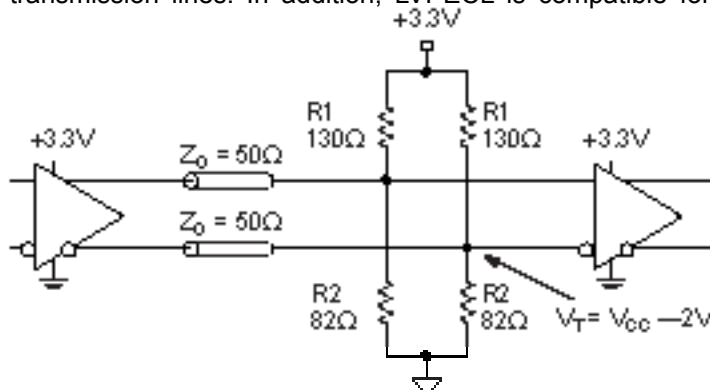


Figure 3e. AC-Coupled CML Input Interface



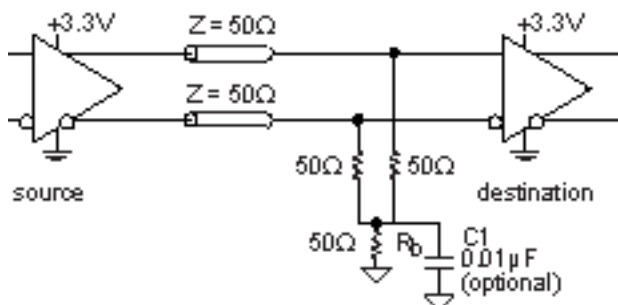
## OUTPUT TERMINATION RECOMMENDATIONS

LVPECL outputs have very low output impedance (open emitter), and small signal swing which results in low EMI (electro-magnetic interference). The LVPECL is ideal for driving 50 ohms and 100 ohms controlled impedance transmission lines. In addition, LVPECL is compatible for



**Figure 4. Parallel Termination-Thevenin Equivalent**

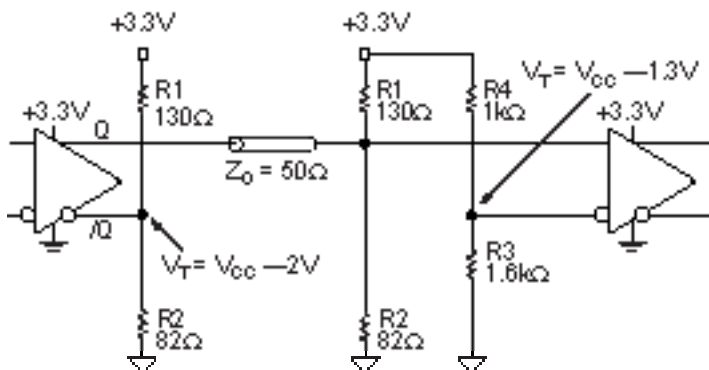
- Note 1.** For +2.5V systems: R1 = 250 ohms, R2 = 62.5 ohms
- Note 2.** For +3.3V systems: R1 = 130 ohms, R2 = 82 ohms



**Figure 5. Three-Resistor "Y-Termination"**

- Note 1.** Power-saving alternative to Thevenin termination.
- Note 2.** Place termination resistors as close to destination inputs as possible.
- Note 3.**  $R_b$  resistor sets the DC bias voltage, equal to  $V_T$ .  
For +2.5V systems  $R_b = 39$  ohms.  
For +3.3V systems  $R_b = 46$  ohms to 50 ohms.
- Note 4.** C1 is an optional bypass capacitor intended to compensate for any  $t_r/t_f$  mismatches.

driving standard PECL inputs since PECL inputs require only 100mV input swing. Further, there are several techniques in terminating the LVPECL outputs, as shown in Figure 4 through 6.



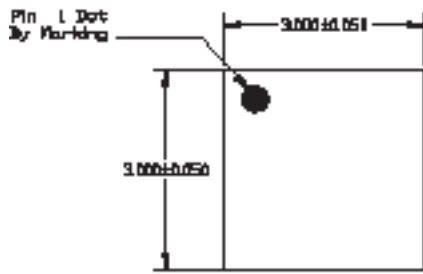
**Figure 6. Terminating Unused I/O**

- Note 1.** Unused output (/Q) must be terminated to balance the output.
- Note 2.** For +2.5V systems: R1=250ohms, R2=62.5ohms, R3=1.25kohms, R4 = 1.2k ohms.  
For +3.3V systems: R1 = 130 ohms, R2 = 82 ohms, R3 = 1k ohms, R4 = 1.6k ohms.
- Note 3.** Unused output pairs (Q and /Q) may be left floating.

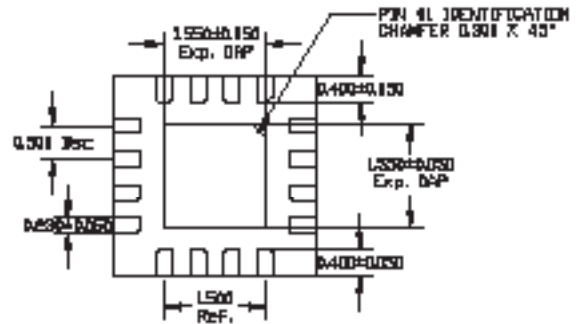
## RELATED MICREL PRODUCTS AND SUPPORT DOCUMENTATION

Part Number	Function	Data Sheet Link
SY58011U	7GHz, 1:2 CML Fanout Buffer/Translator With Internal I/O Termination	<a href="http://www.micrel.com/product-info/prod/ucts/sy58011u.shtml">http://www.micrel.com/product-info/prod/ucts/sy58011u.shtml</a>
SY58012U	5GHz, 1:2 LVPECL Fanout Buffer/Translator With Internal Input Termination	<a href="http://www.micrel.com/product-info/products/sy58012u.shtml">http://www.micrel.com/product-info/products/sy58012u.shtml</a>
SY58013U	6GHz, 1:2 Fanout Buffer/Translator w/400mV LVPECL Outputs and Internal Input Termination	<a href="http://www.micrel.com/product-info/products/sy58013u.shtml">http://www.micrel.com/product-info/products/sy58013u.shtml</a>
	16-MLF® Manufacturing Guidelines Exposed Pad Application Note	<a href="http://www.amkor.com/products/notes_papers/mlf_AppNote_0902.pdf">www.amkor.com/products/notes_papers/mlf_AppNote_0902.pdf</a>
M-0317	HBW Solutions	<a href="http://www.micrel.com/product-info/as/solutions.shtml">http://www.micrel.com/product-info/as/solutions.shtml</a>

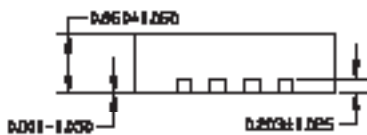
**16-PIN QFN (QFN-16)**



TOP VIEW

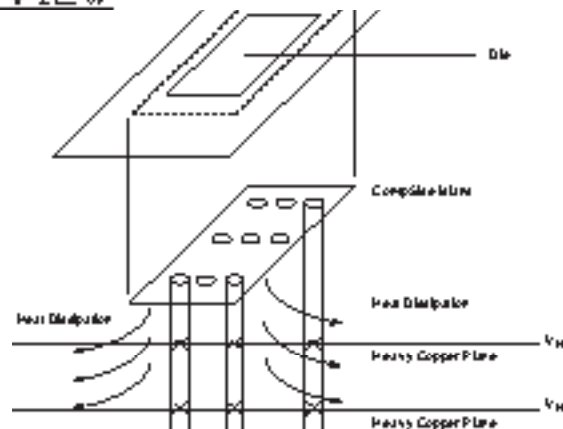


BOTTOM VIEW



SIDE VIEW

- NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
  2. MAX. PACKAGE WARPAGE IS 0.05 mm.
  3. MAXIMUM ALLOWABLE BURR IS 0.075 mm IN ALL DIRECTIONS.
  4. PIN #1 IS ON TOP WILL BE LASER/INK MARKED.



**PCB Thermal Consideration for 16-Pin QFN Package**  
(Always solder, or equivalent, the exposed pad to the PCB)

**Package Notes:**

- Note 1. Package meets Level 2 qualification.
- Note 2. All parts are dry-packaged before shipment.
- Note 3. Exposed pads must be soldered to a ground for proper thermal management.

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