



**ULTRA-PRECISION 1:8 FANOUT  
BUFFER WITH 400mV LVPECL OUTPUTS** Precision Edge®  
**AND INTERNAL TERMININATION** SY58033U

**FEATURES**

- Precision 1:8, 400mV LVPECL fanout buffer
- Low-jitter performance:
  - 76fs<sub>RMS</sub> phase jitter (typ)
- Guaranteed AC performance over temperature and voltage:
  - Clock frequency range: DC to 5.5GHz
  - <80ps t<sub>r</sub>/t<sub>f</sub> times
  - <280ps t<sub>pd</sub>
  - <20ps skew
- 100k LVPECL compatible outputs
- Fully differential inputs/outputs
- Accepts an input signal as low as 100mV
- Unique input termination and V<sub>T</sub> pin accepts DC-coupled and AC-coupled differential inputs: (LVPECL, LVDS, and CML)
- Power supply 2.5V ±5% or 3.3V ±10%
- Industrial temperature range: -40°C to +85°C
- Available in 32-pin (5mm x 5mm) QFN Package



Precision Edge®

**DESCRIPTION**

The SY58033U is a 2.5V/3.3V precision, high-speed, fully differential 400mV LVPECL 1:8 fanout buffer. The SY58033U is optimized to provide eight identical output copies with less than 20ps of skew and only 76fs<sub>RMS</sub> phase jitter. It can process clock signals as fast as 5.5GHz.

The differential input includes Micrel's unique, 3-pin input termination architecture that allows the SY58033U to directly interface to LVPECL, CML, and LVDS differential signal (AC- or DC-coupled) without any level-shifting or termination resistor networks in the signal path. The result is a clean, stub-free, low-jitter solution. The LVPECL (100k temperature compensated) outputs feature a 400mV typical swing into 50 ohms loads, and provide an extremely fast rise/fall time guaranteed to be less than 80ps.

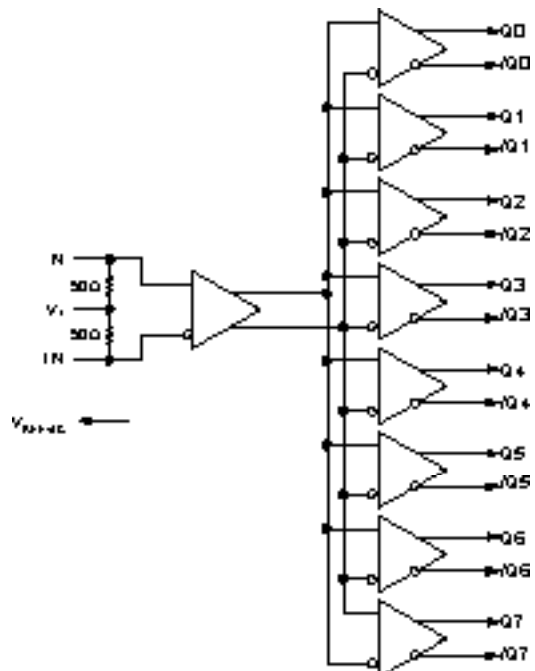
The SY58033U operates from a 2.5V ±5% supply or 3.3V ±10% supply and is guaranteed over the full industrial temperature range (-40°C to +85°C). Other high-speed 1:8 fanout buffers include the CML SY58031U and the 800mV LVPECL SY58032U. The SY58033U is part of Micrel's high-speed, Precision Edge® product line.

All support documentation can be found on Micrel's web site at [www.micrel.com](http://www.micrel.com).

**APPLICATIONS**

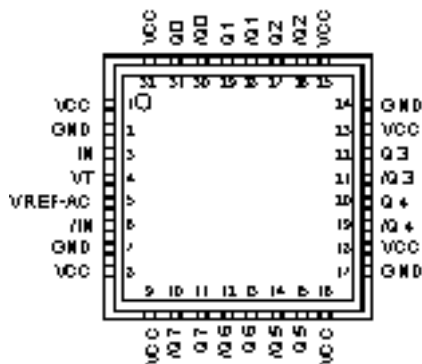
- All SONET and all GigE clock distribution
- All Fibre Channel clock and data distribution
- Network routing engine timing distribution
- High-end, low-skew multiprocessor synchronous clock distribution

**FUNCTIONAL BLOCK DIAGRAM**



United States Patent No. RE44,134  
Precision Edge is a registered trademark of Micrel, Inc.

**PACKAGE/ORDERING INFORMATION**



32-Pin QFN (QFN-32)

**Ordering Information<sup>(1)</sup>**

Part Number	Package Type	Operating Range	Package Marking
SY58033UMG <sup>(3)</sup>	QFN-32 Pb-Free	Industrial	SY58033U with Pb-Free bar-line indicator
SY58033UMGTR <sup>(2, 3)</sup>	QFN-32 Pb-Free	Industrial	SY58033U with Pb-Free bar-line indicator

**Notes:**

- Contact factory for die availability. Dice are guaranteed at T<sub>A</sub> = 25°C, DC electricals only. All devices are Pb-Free.
- Tape and Reel.
- Pb-Free package recommended for new designs.

**PIN DESCRIPTION**

Pin Number	Pin Name	Pin Function
3, 6	IN, /IN	Differential Signal Input: Each pin of this pair internally terminates with 50Ω to the V <sub>T</sub> pin. Note that this input will default to an indeterminate state if left open. See "Input Interface Applications" section.
4	VT	Input Termination Center-Tap: Each input terminates to this pin. The V <sub>T</sub> pin provides a center-tap for each input (IN, /IN) to the termination network for maximum interface flexibility. See "Input Interface Applications" section.
2, 7, 17, 24	GND, Exposed Pad	Ground. Exposed pad must be connected to a ground plane that is the same potential as the ground pin.
1, 8, 9, 16, 18, 23, 25, 32	VCC	Positive Power Supply: Bypass with 0.1μF  0.01μF low ESR capacitors as close to the pins as possible.
31, 30, 29, 28, 27, 26, 22, 21, 20, 19, 15, 14, 13, 12, 11, 10	Q0, /Q0, Q1, /Q1, Q2, /Q2, Q3, /Q3 Q4, /Q4, Q5, /Q5, Q6, /Q6, Q7, /Q7	400mV LVPECL Differential Output Pairs: Differential buffered output copy of the input signal. The LVPECL output swing is typically 400mV into 50Ω. Unused output pairs may be left floating with no impact on jitter. See "LVPECL Output" section.
5	VREF-AC	Bias Reference Voltage: Equal to V <sub>CC</sub> -1.2V (approx.), and used for AC-coupled applications. See "Input Interface Applications" section. When using V <sub>REF-AC</sub> , bypass with 0.01μF capacitor to V <sub>CC</sub> . Maximum sink/source current is 0.5mA.

### Absolute Maximum Ratings<sup>(1)</sup>

Power Supply Voltage ( $V_{CC}$ ) ..... -0.5V to +4.0V  
 Input Voltage ( $V_{IN}$ )..... -0.5V to  $V_{CC}$   
 Current ( $V_T$ )  
 Source or sink current on  $V_T$  pin.....  $\pm 100$ mA  
 Input Current ( $V_T$ )  
 Source or sink current on IN, /IN .....  $\pm 50$ mA  
 Current ( $V_{REF}$ )  
 Source or sink current on  $V_{REF-AC}$ <sup>(3)</sup>.....  $\pm 1.5$ mA  
 Lead Temperature Soldering (20 sec.) ..... 260°C  
 Storage Temperature Range ( $T_S$ ) ..... -65°C to +150°C

### Operating Ratings<sup>(2)</sup>

Power Supply Voltage ( $V_{CC}$ ) ..... +2.375V to +3.60V  
 Ambient Temperature Range ( $T_A$ ) ..... -40°C to +85°C  
 Package Thermal Resistance<sup>(4)</sup>  
 QFN ( $\theta_{JA}$ )  
 Still-Air ..... 35°C/W  
 QFN ( $\psi_{JB}$ )  
 Junction-to-Board ..... 20°C/W

## DC ELECTRICAL CHARACTERISTICS<sup>(5)</sup>

$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{CC}$	Power Supply Voltage	2.5V nominal	2.375	2.5	2.625	V
		3.3V nominal	3.0	3.3	3.6	V
$I_{CC}$	Power Supply Current	$V_{CC} = \text{max}$ . No. load includes current through 50 $\Omega$ pull-ups.		180	250	mA
$V_{IH}$	Input HIGH Voltage	IN, /IN, Note 6	$V_{CC}-1.6$		$V_{CC}$	V
$V_{IL}$	Input LOW Voltage	IN, /IN	0		$V_{IH}-0.1$	V
$V_{IN}$	Input Voltage Swing	IN, /IN, see Figure 1a.	0.1		1.7	V
$V_{DIFF\_IN}$	Differential Input Voltage Swing  IN0, /IN0 ,  IN1, /IN1	IN, /IN, see Figure 1b.	0.2			V
$R_{IN}$	In-to- $V_T$ Resistance		40	50	60	$\Omega$
$V_{T\_IN}$	Max. In-to- $V_T$ (IN, /IN)				1.28	V
$V_{REF-AC}$			$V_{CC}-1.3$	$V_{CC}-1.2$	$V_{CC}-1.1$	V

## LVPECL DC ELECTRICAL CHARACTERISTICS<sup>(5)</sup>

$V_{CC} = 2.5\text{V} \pm 5\%$  or  $3.3\text{V} \pm 10\%$ ;  $R_L = 50\Omega$  to  $V_{CC}-2\text{V}$ ;  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  unless otherwise stated

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{OH}$	Output HIGH Voltage		$V_{CC}-1.145$		$V_{CC}-0.895$	V
$V_{OL}$	Output LOW Voltage		$V_{CC}-1.545$		$V_{CC}-1.295$	V
$V_{OUT}$	Output Voltage Swing	see Figure 1a.	150	400		mV
$V_{DIFF\_OUT}$	Differential Voltage Swing	see Figure 1b.	300	800		mV

**Notes:**

1. Permanent device damage may occur if "Absolute Maximum Ratings" are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to "Absolute Maximum Ratings" conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Due to the limited drive capability, use for input of the same package only.
4. Thermal performance assumes exposed pad is soldered (or equivalent) to the device's most negative potential (GND) on the PCB.  $\psi_{JB}$  uses 4-layer  $\theta_{JA}$  in still-air number unless otherwise stated.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6.  $V_{IH}$  (min) not lowers than 1.2V.

## AC ELECTRICAL CHARACTERISTICS(7)

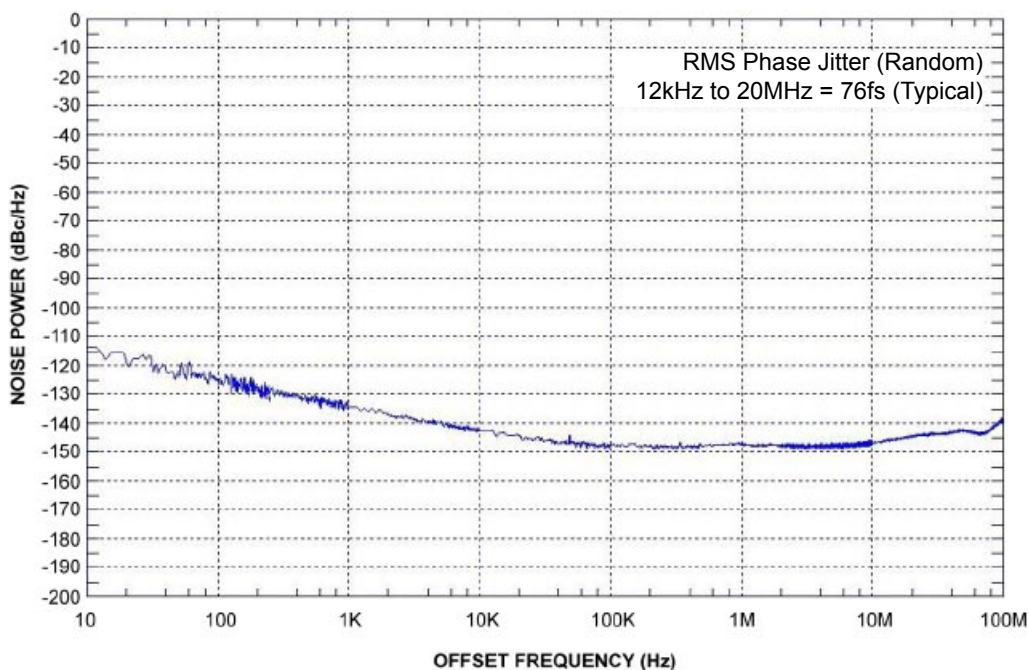
$V_{CC} = 2.5V \pm 5\%$  or  $3.3V \pm 10\%$ ;  $R_L = 50\Omega$  to  $V_{CC}-2V$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$f_{MAX}$	Maximum Operating Frequency	$V_{OUT} \geq 200mV$ Clock	5.5			GHz
$t_{pd}$	Propagation Delay (IN-to-Q)		130	200	280	ps
$t_{pd} \text{ tempco}$	Differential Propagation Delay Temperature Coefficient			35		fs/°C
$t_{SKEW}$	Output-to-Output Skew(within device)	<b>Note 8</b>		7	20	ps
	Part-to-Part Skew	<b>Note 9</b>			100	ps
$t_{JITTER}$	RMS Phase Jitter	Output = 622MHz Integration Range 12kHz - 20MHz		76		fs
$t_r, t_f$	Output Rise/Fall Time	20% to 80%, at full output swing.	20	50	80	ps

**Notes:**

7. High frequency AC electricals are guaranteed by design and characterization. All outputs loaded with  $50\Omega$  to  $V_{CC}-2V$ ,  $V_{IN} \geq 100mV$ .
8. Output-to-output skew is measured between outputs under identical conditions.
9. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs. Part-to-part skew includes variation in  $t_{pd}$ .

## PHASE NOISE



**Phase Noise Plot: 622MHz @ 3.3V**

### SINGLE-ENDED AND DIFFERENTIAL SWINGS

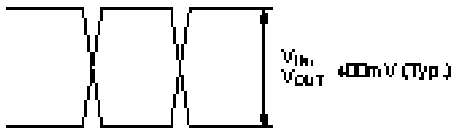


Figure 1a. Single-Ended Voltage Swing

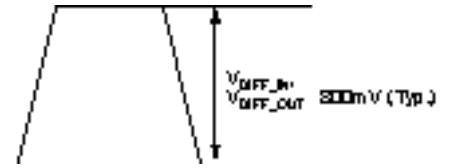
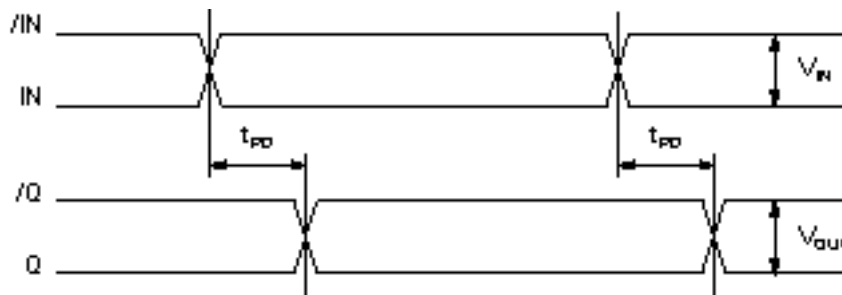


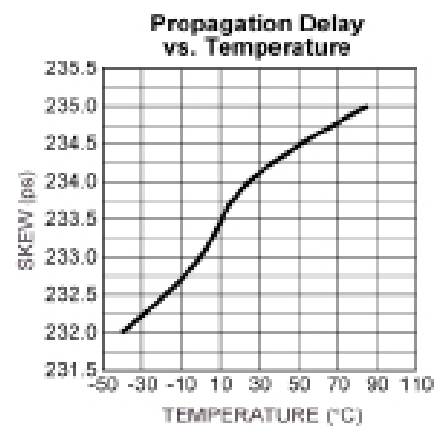
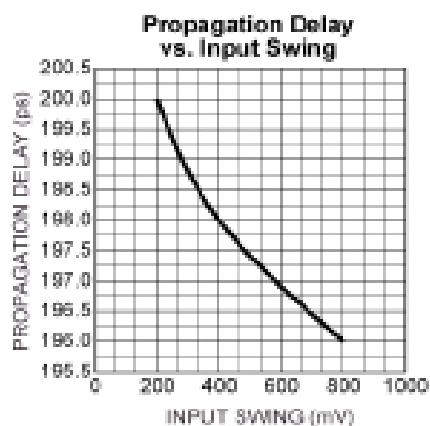
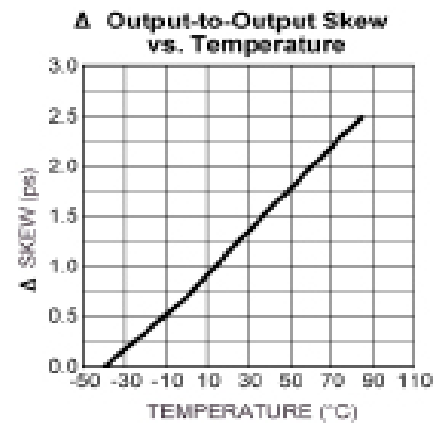
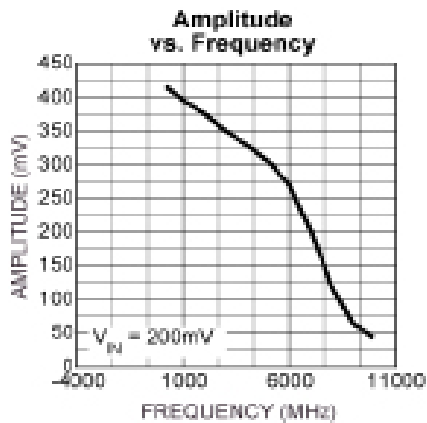
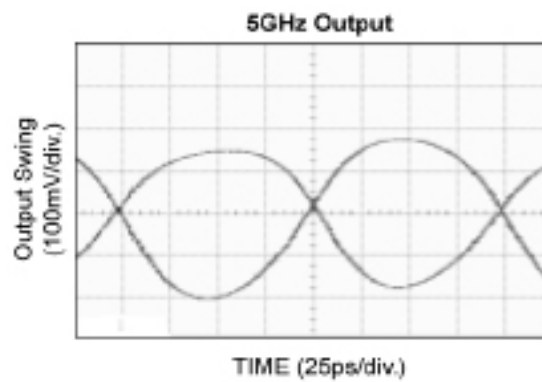
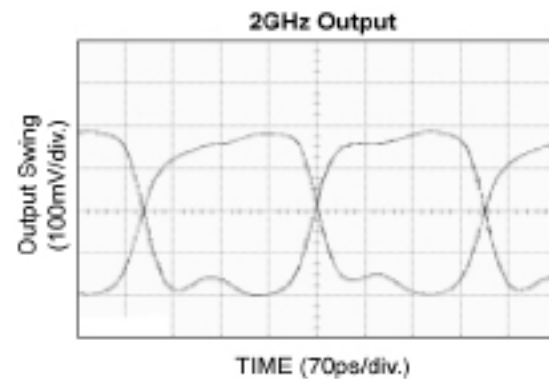
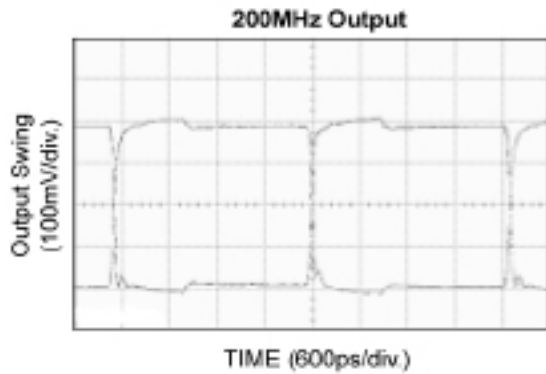
Figure 1b. Differential Voltage Swing

### TIMING DIAGRAM



**TYPICAL OPERATING CHARACTERISTICS**

$V_{CC} = 2.5V$ ,  $GND = 0$ ,  $V_{IN} = 100mV$ ,  $T_A = 25^\circ C$ , unless otherwise stated.



**INPUT BUFFER**

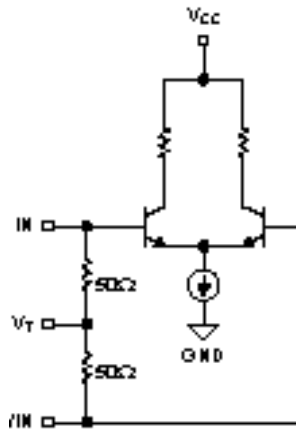


Figure 2. Simplified Differential Input Buffer

**INPUT INTERFACE APPLICATIONS**

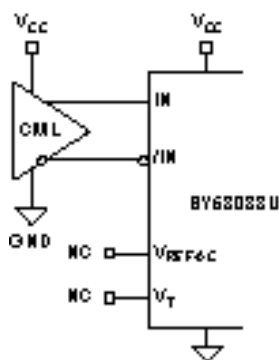


Figure 3a. DC-Coupled CML Input Interface

Option: May connect  $V_T$  to  $V_{CC}$ .

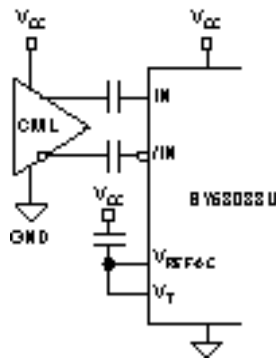
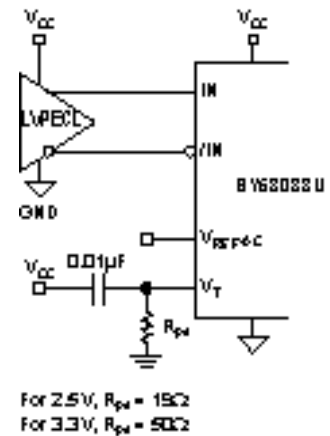
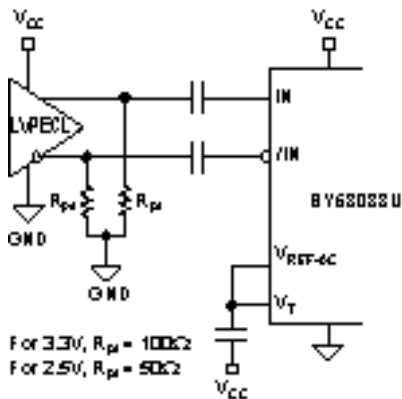


Figure 3b. AC-Coupled CML Input Interface



For 2.5V,  $R_{Pd} = 15\Omega$   
For 3.3V,  $R_{Pd} = 50\Omega$

Figure 3c. LVPECL Input Interface



For 3.3V,  $R_{Pd} = 100\Omega$   
For 2.5V,  $R_{Pd} = 50\Omega$

Figure 3d. AC-Coupled LVPECL Input Interface

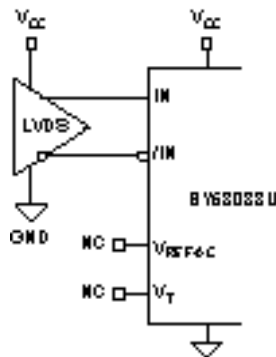


Figure 3e. LVDS Input Interface

## LVPECL OUTPUT

LVPECL has high input impedance, and very low output impedance (open emitter), and small signal swing which results in low electromagnetic interference (EMI). LVPECL is ideal for driving 50Ω and 100Ω controlled impedance transmission lines. There are several techniques in

terminating the LVPECL output, which are the Parallel Termination-Thevenin Equivalent, the Parallel Termination (3-Resistor), and the AC-Coupled Termination. Unused output pairs may be left floating. However, single-ended outputs must be terminated, or balanced.

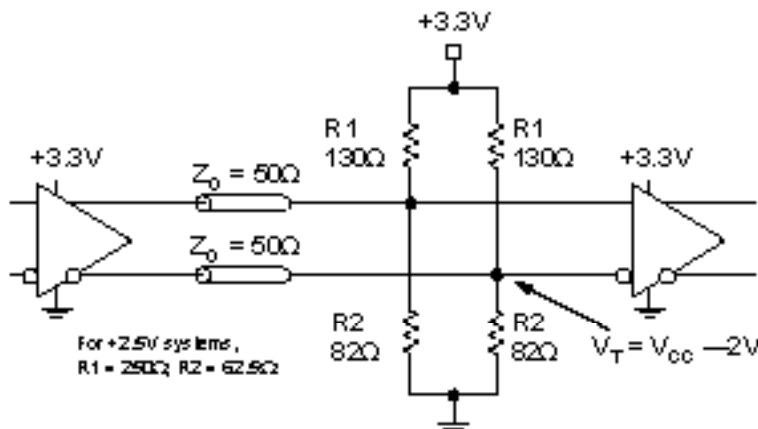
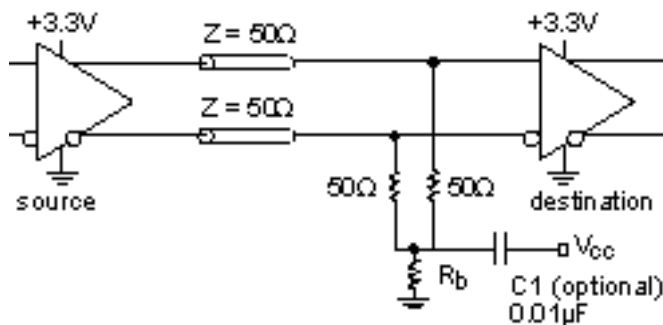


Figure 4. Parallel Termination-Thevenin Equivalent



1. Power saving alternative to Thevenin termination.
2. Place termination resistors as close to destination inputs as possible.
3.  $R_b$  sets the DC bias voltage, equal to  $V_T$ .
4. For 2.5V systems,  $R_b = 150\Omega$ . For 3.3V systems,  $R_b = 50\Omega$ .

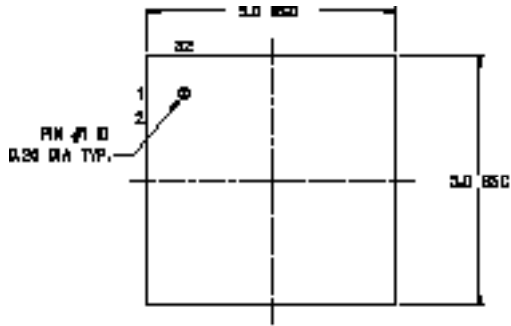
Figure 5. Parallel Termination (3-Resistor)

## RELATED MICREL PRODUCTS AND SUPPORT DOCUMENTATION

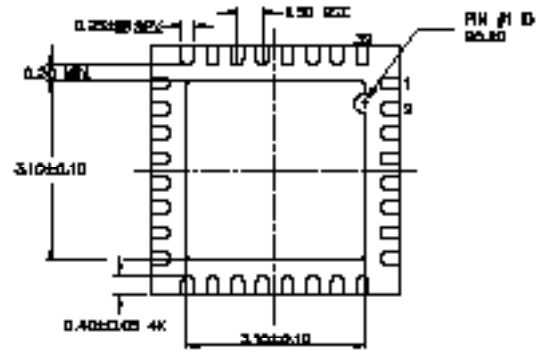
Part Number	Function	Data Sheet Link
SY58031U	Ultra-Precision 1:8 Fanout Buffer with 400mV CML Outputs and Internal I/O Termination	<a href="http://www.micrel.com/product-info/products/sy58031u.shtml">http://www.micrel.com/product-info/products/sy58031u.shtml</a>
SY58032U	Ultra-Precision 1:8 Fanout Buffer with LVPECL Outputs and Internal Termination	<a href="http://www.micrel.com/product-info/products/sy58032u.shtml">http://www.micrel.com/product-info/products/sy58032u.shtml</a>
SY58033U	Ultra-Precision 1:8 Fanout Buffer with 400mV LVPECL Outputs and Internal Termination	<a href="http://www.micrel.com/product-info/products/sy58033u.shtml">http://www.micrel.com/product-info/products/sy58033u.shtml</a>
	32-MLF® Manufacturing Guidelines Exposed Pad Application Note	<a href="http://www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf">www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf</a>
	HBW Solutions	<a href="http://www.micrel.com/product-info/as/solutions.shtml">http://www.micrel.com/product-info/as/solutions.shtml</a>



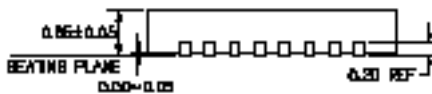
**32-PIN QFN (QFN-32)**



TOP VIEW

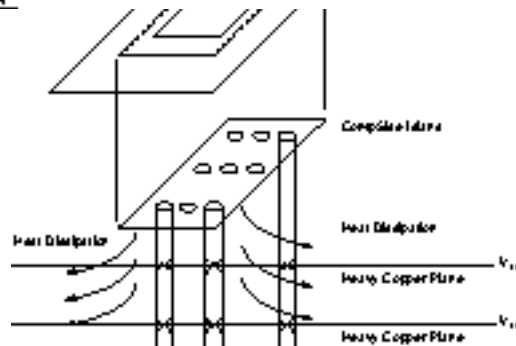


BOTTOM VIEW



SIDE VIEW

NOTE:  
 1. ALL DIMENSIONS ARE IN MILLIMETERS.  
 2. MAX PACKAGE WARPAGE IS 0.03 mm.  
 3. MAXIMUM ALLOWABLE BURESS IS 0.076 mm IN ALL DIRECTIONS.  
 4. PIN #1 ID ON TOP WILL BE LASER/DINK MARKED.



**PCB Thermal Consideration for 32-Pin QFN Package**  
 (Always solder, or equivalent, the exposed pad to the PCB)

**Package Notes:**

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

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