SY58038U

Ultra-Precision, 8:1 MUX with Internal Termination and 1:2 LVPECL Fanout Buffer

Precision Edge®

General Description

The SY58038U is a low-jitter, low-skew, high-speed 8:1 multiplexer with a 1:2 differential fanout buffer optimized for precision telecom and enterprise server distribution applications. The SY58038U distributes clock frequencies from DC to 3.5GHz, and data rates to 4.5Gpbs guaranteed over temperature and voltage.

The SY58038U differential input includes Micrel's unique, 3-pin input termination architecture that directly interfaces to any differential signal (AC- or DC-coupled) as small as 100mV without any level shifting or termination resistor networks in the signal path. The outputs are 800mV, 100K compatible LVPECL with extremely fast rise/fall times guaranteed to be less than 100ps.

The SY58038U features a patented isolation design that significantly improves channel-to-channel crosstalk performance.

The SY58038U operates from a 2.5V ±5% or 3.3V ±10% supply and is guaranteed over the full industrial temperature range of –40°C to +85°C. The SY58038U is part of Micrel's high-speed, Precision Edge® product line.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

Precision Edge®

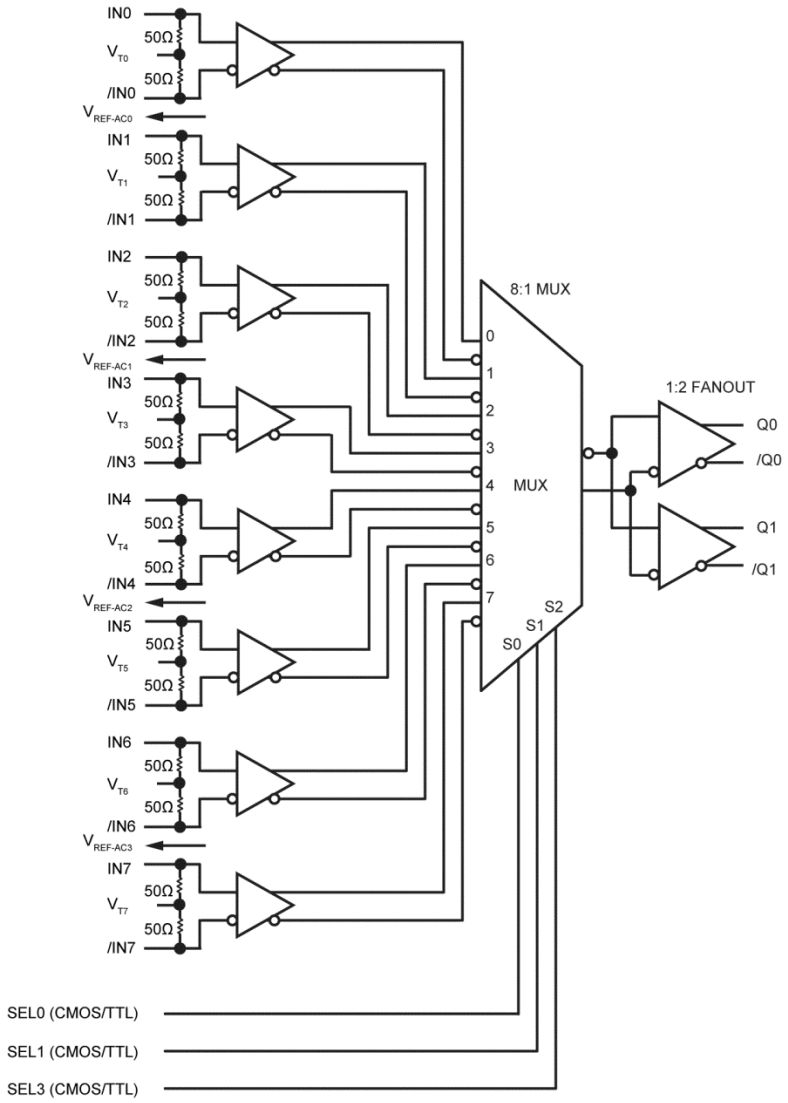
Features

- Selects between 1 of 8 inputs, and provides two precise, low-skew LVPECL output copies
- Ultra-low jitter design:
  - 72fs$_{rms}$ phase jitter (typical)
- Guaranteed AC performance over temperature and voltage:
  - DC to 4.5Gbps throughput
  - <500ps propagation delay IN-to-Q (V_{IN} > 100mV)
  - <100ps t_r / t_f time
  - <15ps skew (output-to-output)
- Unique, patented, channel-to-channel isolation design provides superior crosstalk performance
- Unique, patented, input termination and V_T pin accepts DC- and AC-coupled inputs (CML, PECL, LVDS)
- 800mV LVPECL output swing
- Power supply 2.5V ±5% or 3.3V ±10%
- –40°C to +85°C temperature range
- Available in 44-pin (7mm × 7mm) QFN package

Applications

- Data communication systems
- All SONET/SDH data/clock applications
- All Fibre Channel applications
- All Gigabit Ethernet applications

Functional Block Diagram



Truth Table

SEL2	SEL1	SEL0	Q	/Q
L	L	L	IN0	/IN0
L	L	H	IN1	/IN1
L	H	L	IN2	/IN2
L	H	H	IN3	/IN3
H	L	L	IN4	/IN4
H	L	H	IN5	/IN5
H	H	L	IN6	/IN6
H	H	H	IN7	/IN7

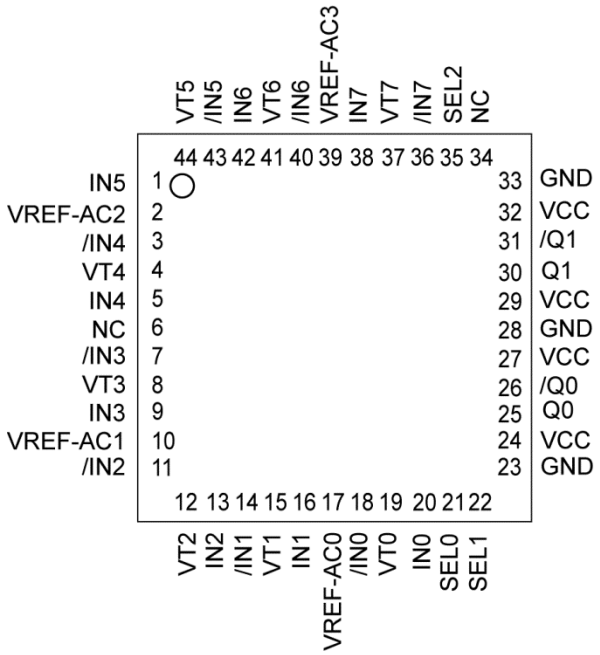
Ordering Information[1]

Part Number	Marking	Operating Range	Package
SY58038UMY	SY58038U	–40°C to +85°C	44-pin (7mm × 7mm) QFN
SY58038UMY TR[2]	SY58038U	–40°C to +85°C	44-pin (7mm × 7mm) QFN

Notes:

1. Contact factory for die availability. Die are guaranteed at T_A = +25°C, DC electricals only.
2. Tape and reel.

Pin Configuration



44-Pin (7mm × 7mm) QFN (QFN-44)
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
20, 18 16, 14 13, 11 9, 7 5, 3 1, 43 42, 40 38, 36	IN0, /IN0 IN1, /IN1 IN2, /IN2 IN3, /IN3 IN4, /IN4 IN5,/IN5 IN6, /IN6 IN7, /IN7	Differential Inputs: These input pairs are the differential signal inputs to the device. Inputs accept AC or DC-coupled signals as small as 100mV. Each pin of a pair internally terminates to a VT pin through 50Ω. Note that these inputs will default to an indeterminate state if left open. Refer to the *Input Interface Applications* section for more details.
19,15 12, 8 4, 44 41, 37	VT0, VT1 VT2, VT3 VT4, VT5 VT6, VT7	Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin. The VT pins provide a center-tap to a termination network for maximum interface flexibility. Refer to the *Input Interface Applications* section for more details
17 10 2 39	VREF-AC0 VREF-AC1 VREF-AC2 VREF-AC3	Reference Voltage: This output biases to V_{CC} – 1.2V. It is used when AC coupling the inputs (IN, /IN). For AC-coupled applications, connect VREF-AC to the VT pin and bypass with a 0.01µF low-ESR capacitor to V_{CC} or GND, depending on input type. Refer to the *Input Interface Applications* section for more details.
21 22 35	SEL0 SEL1 SEL2	The single-ended TTL/CMOS-compatible inputs select the inputs to the multiplexer. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open.
24, 27, 29, 32	VCC	Positive Power Supply. Bypass with 0.1µF//0.01µF low-ESR capacitors as close to each VCC pin.
25, 26 30, 31	Q0,/Q0 Q1,/Q1	Differential Outputs: These LVPECL output pairs are the outputs of the device. Unused output pairs may be left open. Each output is designed to drive 800mV into 50Ω terminated to V_{CC} – 2V (or V_{CC} – 1.2V, if AC-coupled).
23, 28, 33	GND, ePad	Ground. GND and exposed pad (ePad) must both be connected to the most negative potential of chip ground.

hbwhelp@micrel.com or (408) 955-1690

Absolute Maximum Ratings[3]

Power Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
LVPECL Output Current (I_{OUT})
  Continuous 50mA
  Surge 100mA
Termination Current[6]
  Source or Sink Current (on VT pin) ..... ±100mA
Lead Temperature (soldering, 10s) ..... +260°C
Storage Temperature Range (T_S) ..... –65°C to +150°C

Operating Ratings[4]

Power Supply
  Voltage (V_{CC}) ..... +2.375V to +2.625V or +3.0V to 3.6V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance[5]
  QFN (θ_{JA})
    Still Air ..... 24°C/W
  QFN (ψ_{JB})
    Junction-to-Board ..... 12°C/W

DC Electrical Characteristics[7]

T_A = –40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power Supply Voltage	V_{CC} = 2.5V	2.375	2.5	2.625	V
		V_{CC} = 3.3V	3.0	3.3	3.6	
I_{CC}	Power Supply Current	No load, maximum V_{CC}		120	170	mA
R_{IN}	Input Resistance (IN-to-V_T)		40	50	60	Ω
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		80	100	120	Ω
V_{IH}	Input HIGH Voltage (IN-to-/IN)	Note 8	V_{CC} – 1.6		V_{CC}	V
V_{IL}	Input LOW Voltage (IN-to-/IN)		0		V_{IN} – 0.1	V
V_{IN}	Input Voltage Swing (IN-to-/IN)	See Figure 1	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage Swing (IN-to-/IN)	See Figure 2	0.2			V
V_{T_IN}	IN-to-V_T (IN-to-/IN)				1.28	V
V_{REF-AC}	Output Reference Voltage		V_{CC} – 1.3	V_{CC} – 1.2	V_{CC} – 1.1	V

Notes:

3. Permanent device damage may occur if ratings in the *Absolute Maximum Ratings* section are exceeded. This is a stress rating only and functional operation is not implied for conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
4. The datasheet limits are not guaranteed if the device is operated beyond the operating ratings.
5. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. ψ_{JB} uses 4-layer θ_{JA} in still-air number unless otherwise stated.
6. Due to the limited drive capability, use for input of the same package only.
7. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
8. V_{IH} (minimum), not lower than 1.2V.

LVPECL Output DC Electrical Characteristics[9]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A = –40°C ≤ to +85°C, R_L = 50Ω to V_{CC} – 2V, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OH}	Output HIGH Voltage (Q, /Q)		V_{CC} – 1.145		V_{CC} – 0.895	V
V_{OL}	Output LOW Voltage (Q, /Q)		V_{CC} – 1.945		V_{CC} – 1.695	V
V_{OUT}	Output Differential Swing (Q, /Q)	See Figure 1	550	800		mV
V_{DIFF_OUT}	Differential Output Voltage Swing (Q, /Q)	See Figure 2	1100	1600		mV

LVTTL/CMOS DC Electrical Characteristics[9]

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A = –40°C ≤ to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current		–125		30	µA
I_{IL}	Input LOW Current		–300			µA

AC Electrical Characteristics[10]

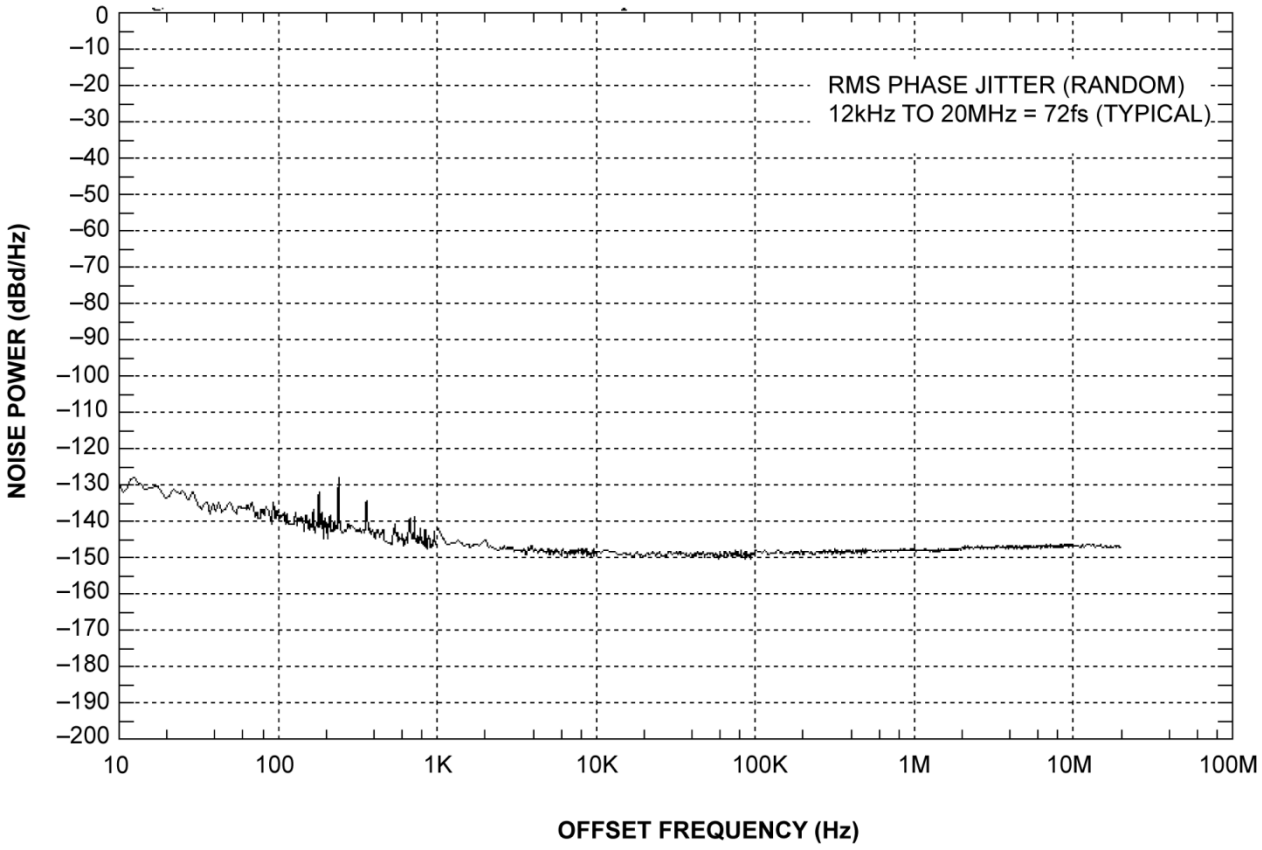
V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A = –40°C ≤ to +85°C, R_L = 50Ω to V_{CC} – 2V, unless otherwise noted.

Symbol	Parameter		Condition	Min.	Typ.	Max.	Units
f_{MAX}	Maximum Operating Frequency		NRZ Data	4.5			Gbps
			V_{OUT} ≥ 400mV Clock	3.5	5		GHz
t_{pd}	Differential Propagation Delay	IN-to-Q	V_{IN} ≥ 100mV	280	390	500	ps
		SEL-to-Q		150		600	ps
Δt_{pd} Temp Coefficient	Differential Propagation Delay Temperature Coefficient				220		fs/°C
t_{SKEW}	Output-to-Output Skew		Note 11			15	ps
	Part-to-Part Skew		Note 12			150	ps
t_{JITTER}	RMS Phase Jitter		Carrier = 622MHz Integration Range: 12kHz – 20MHz		72		fs_{rms}
t_r, t_f	Output Rise/Fall Time		At full output swing, 20% to 80%	35	65	100	ps

Note:

9. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
10. High-frequency AC-parameters are guaranteed by design and characterization.
11. Output-to-output skew is measured between two different outputs under identical input transitions.
12. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.

Phase Noise Plot



Single-Ended and Differential Swings

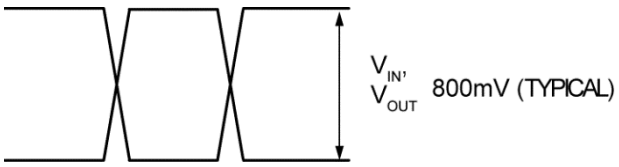


Figure 1. Single-Ended Voltage Swing

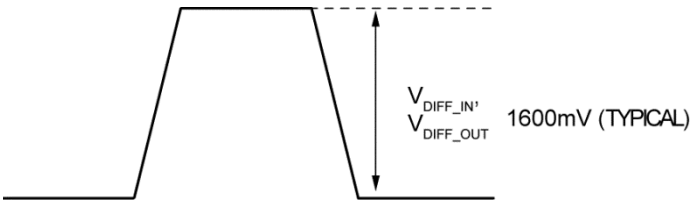
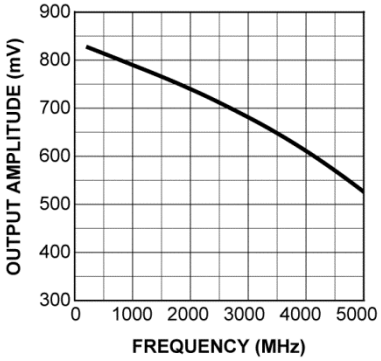


Figure 2. Differential Voltage Swing

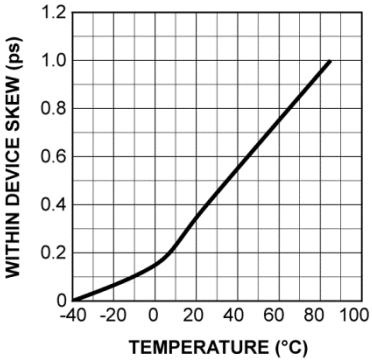
Typical Operating Characteristics

V_{CC} = 3.3V, GND = 0, V_{IN} = 100mV, T_A = +25°C, unless otherwise stated

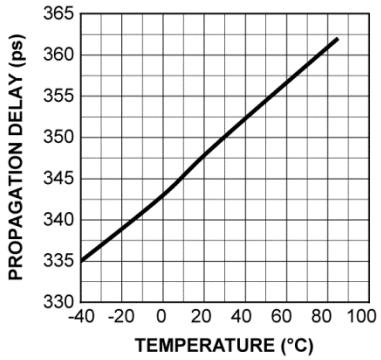
Output Amplitude vs. Frequency



Within Device Skew vs. Temperature



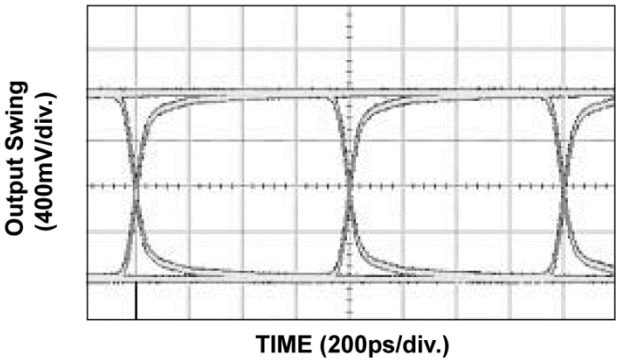
Propagation Delay vs. Temperature



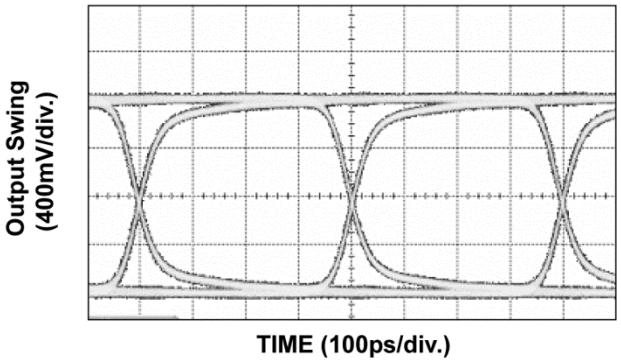
Functional Characteristics

V_{CC} = 3.3V, GND = 0, V_{IN} = 100mV, T_A = +25°C, unless otherwise stated.

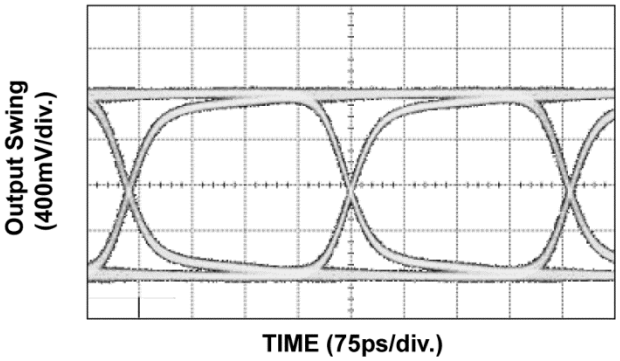
1.25Gbps Output (Q – /Q)



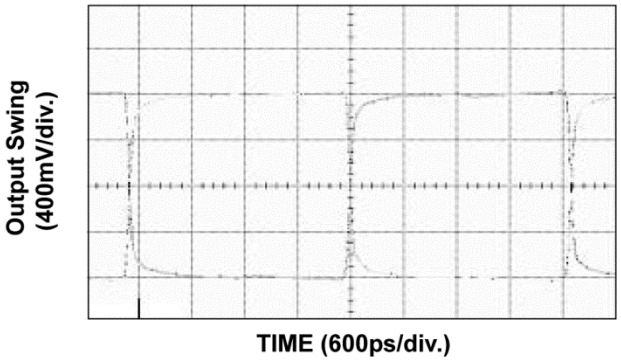
2.5Gbps Output (Q – /Q)



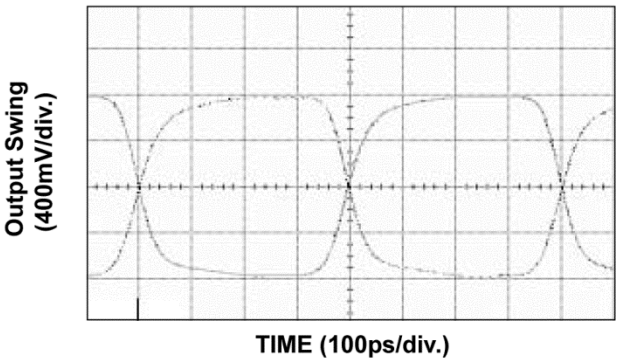
3.2Gbps Output (Q – /Q)



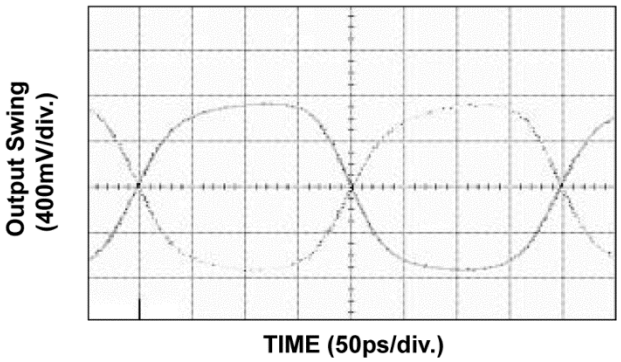
200MHz Output (Q – /Q)



1.25GHz Output (Q – /Q)



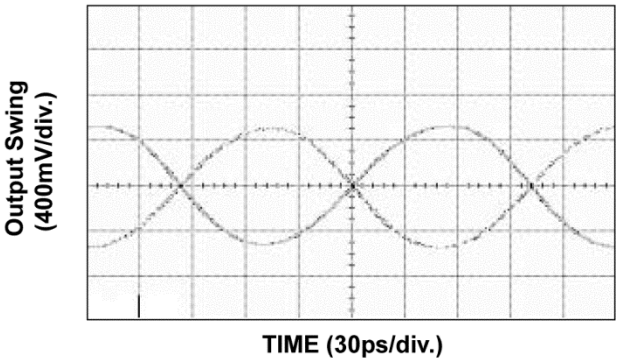
2.5GHz Output (Q – /Q)



Functional Characteristics (Continued)

V_{CC} = 3.3V, GND = 0, V_{IN} = 100mV, T_A = +25°C, unless otherwise stated.

5GHz Output (Q – /Q)



Input and Output Stages

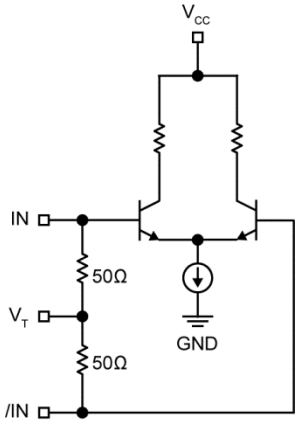


Figure 3. Simplified Differential Input Stage

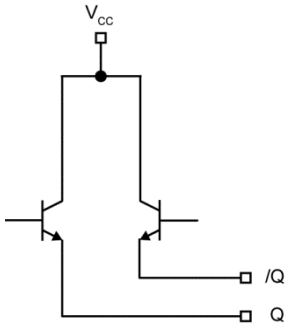


Figure 4. Simplified LVPECL Output Stage

Input Interface Applications

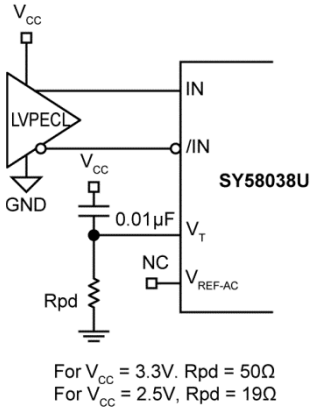


Figure 5. LVPECL Interface (DC-Coupled)

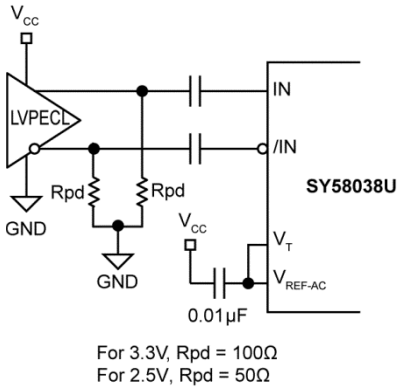


Figure 6. LVPECL Interface (AC-Coupled)

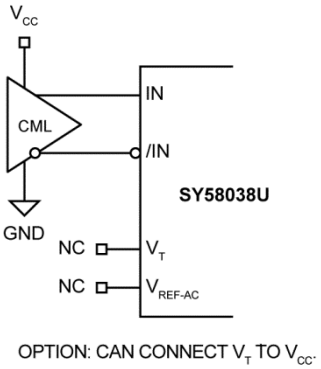


Figure 7. CML Interface (DC-Coupled)

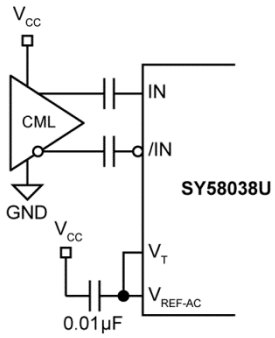


Figure 8. CML Interface (AC-Coupled)

Input Interface Applications (Continued)

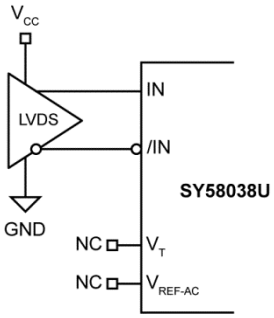


Figure 9. LVDS Interface (DC Coupled)

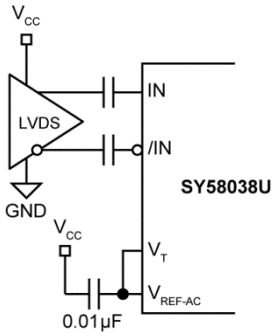
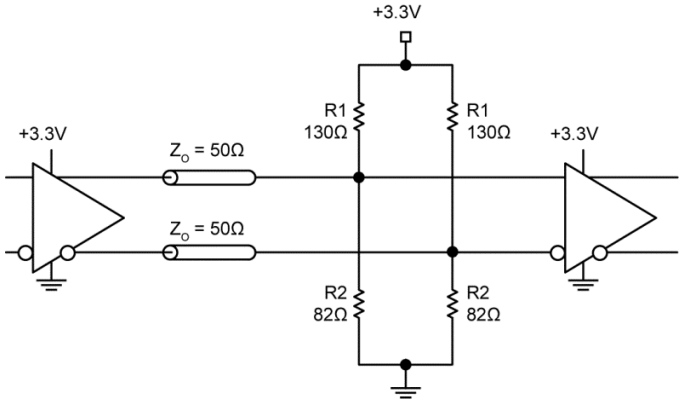


Figure 10. LVDS Interface (AC Coupled)

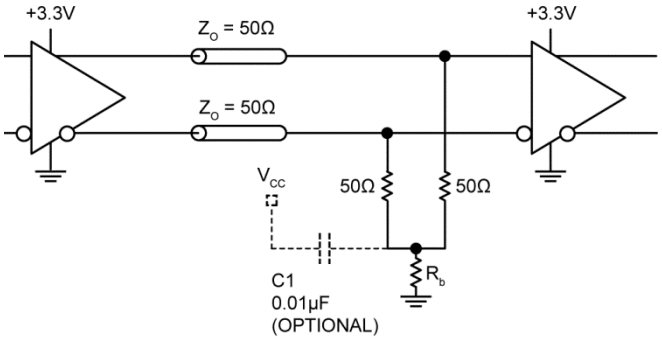
Output Interface Applications



Note:

For +2.5V system, R1 = 250Ω, R2 = 62.5Ω

Figure 11. Parallel Thevenin-Equivalent Termination

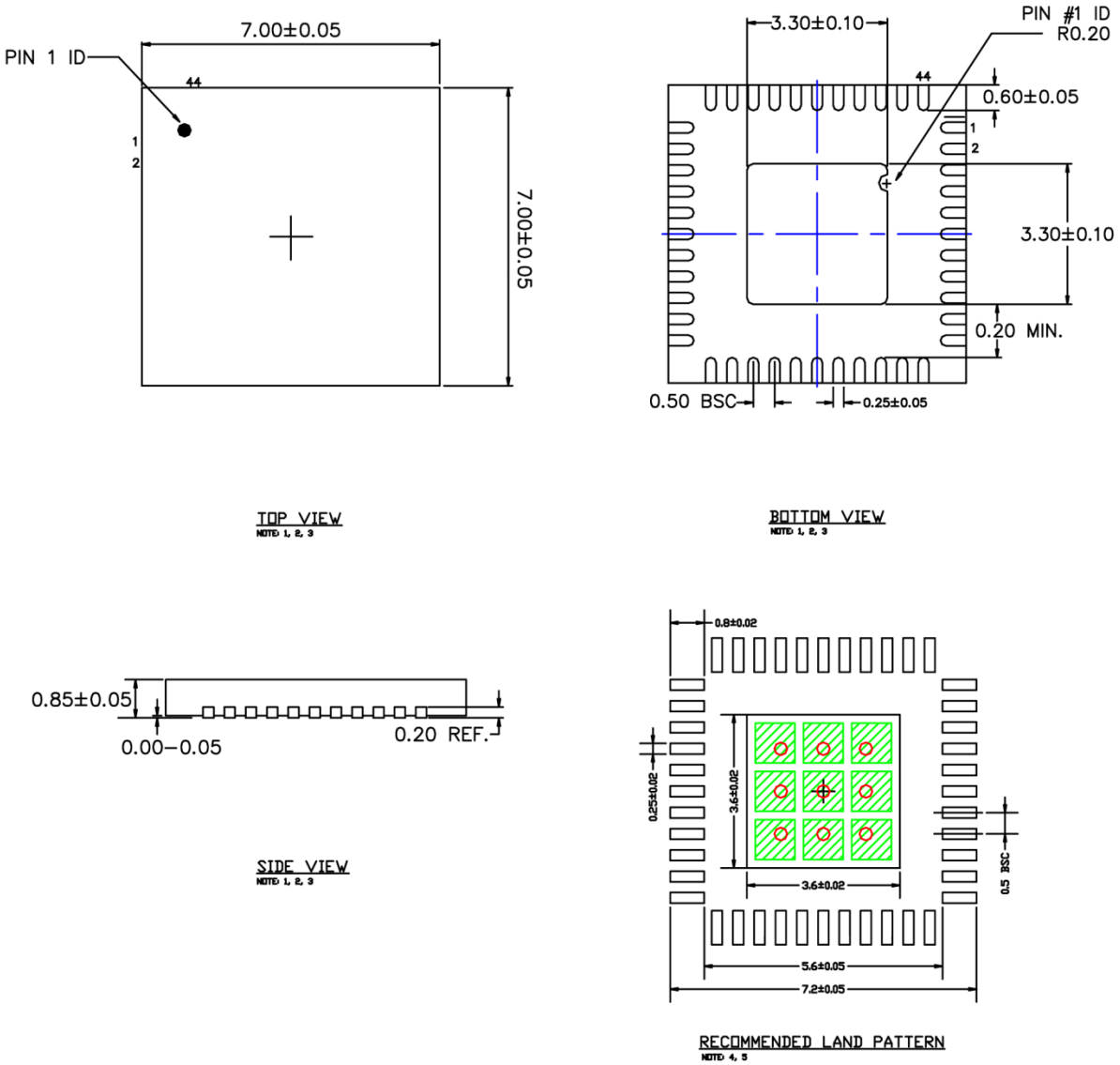


Note:

For +2.5V system, R_b = 19Ω
For +3.3V system, R_b = 50Ω

Figure 12. Parallel Termination (3-Resistor)

Package Information and Recommended Landing Pattern[13]



NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30–0.35MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE. 1.0MM PITCH
5. GREEN RECTANGLES (SHADED AREA) REPRESENT SOLDER STENCIL OPENING ON EXPOSED PAD AREA. RECOMMENDED SIZE IS 0.93x0.93MM, SPACING IS 0.2MM

44-Pin 7mm × 7mm QFN (MM)

Note:

13. Package meets Level 2 qualification. All parts are dry-packaged before shipment. Exposed pads must be soldered to a ground for proper thermal management. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com

Micrel, Inc. is a leading global manufacturer of IC solutions for the worldwide high-performance linear and power, LAN, and timing & communications markets. The Company's products include advanced mixed-signal, analog & power semiconductors; high-performance communication, clock management, MEMs-based clock oscillators & crystal-less clock generators, Ethernet switches, and physical layer transceiver ICs. Company customers include leading manufacturers of enterprise, consumer, industrial, mobile, telecommunications, automotive, and computer products. Corporation headquarters and state-of-the-art wafer fabrication facilities are located in San Jose, CA, with regional sales and support offices and advanced technology design centers situated throughout the Americas, Europe, and Asia. Additionally, the Company maintains an extensive network of distributors and reps worldwide.