Applications Note: SY5830

Single Stage Flyback And PFC Controller With Primary Side Control For LED Lighting

Preliminary datasheet

General Description

The SY5830 is a single stage Flyback and PFC controller targeting at LED lighting applications. It is a primary side controller without applying any secondary feedback circuit for low cost, and drives the Flyback converter in the quasi-resonant mode to achieve higher efficiency. It keeps the Flyback converter in constant on time operation to achieve high power factor. It adopts special design to achieve quick start up and reliable protection for safety requirement.

Ordering Information

SY5830 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY5830ABC	SOT23-6	----

Features

- Primary side control eliminates the opto-coupler.
- Valley turn-on of the primary MOSFET to achieve low switching losses
- Power factor >0.90 with single-stage conversion.
- Reliable short LED and Open LED protection
- Quick start up <500ms
- Low start up current:15μA typical
- Package: SOT23-6

Applications

- LED lighting

Typical Applications

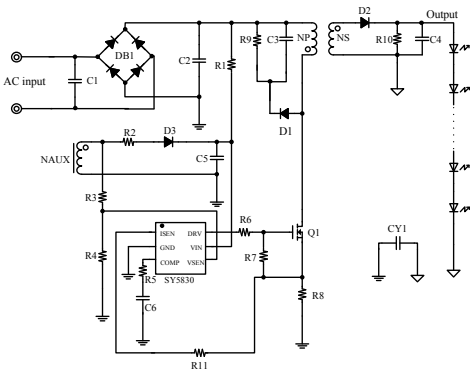


Figure 1. Schematic Diagram SOT23-6

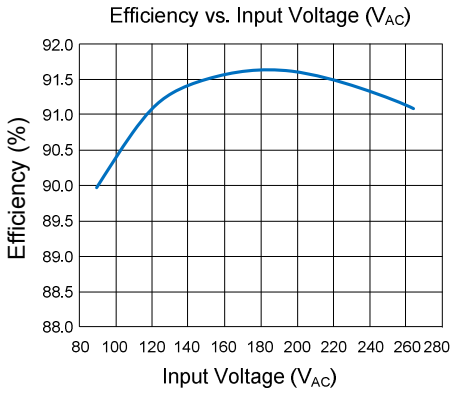
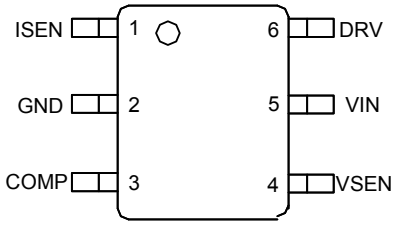


Figure 2. Efficiency vs Input Voltage

Pinout (top view)



(SOT23-6)

Top Mark: XO*xyz* (device code: XO, ***x=year code, y=week code, z= lot number code***)

Pin Name	SOT23-6	Pin Description
ISEN	1	Current sense pin. Connect this pin to the source of the primary switch. Connect the sense resistor across the source of the primary switch and the GND pin. (current sense resister R_S: $R_S=k\frac{V_{REF}\times N_{PS}}{I_{OUT}}$, k=0.167) Also this pin used to detect transformer and secondary is short or not.
GND	2	Ground pin
COMP	3	Loop compensation pin. Connect a RC network across this pin and ground to stabilize the control loop.
VSEN	4	Inductor current zero-crossing detection pin. This pin receives the auxiliary winding voltage by a resister divider and detects the inductor current zero crossing point. This pin also provides over voltage protection and line regulation modification function simultaneously. If the voltage on this pin is above $V_{VSEN,OVP}$, the IC would enter over voltage protection mode. Good line regulation can be achieved by adjusting the upper resistor of the divider.
VIN	5	Power supply pin. This pin also provides output over voltage protection along with VSEN pin.
DRV	6	Gate driver pin. Connect this pin to the gate of primary MOSFET.

Absolute Maximum Ratings (Note 1)

VIN, DRV ---------- -0.3V~33V
Supply Current I_{VIN} ---------- 15mA
VSEN---------- -0.3V ~V_{IN}+0.3V
ISEN, COMP ---------- -0.3~3.6V
Power Dissipation, @ T_A = 25°C SOT23-6 ----------0.6W
Package Thermal Resistance (Note 2)
SOT23-6, θJA ----------170°C/W
SOT23-6, θJC ----------130°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

VIN, DRV ---------- 9.5V~27V
Junction Temperature Range ---------- -40°C to 125°C

Block Diagram

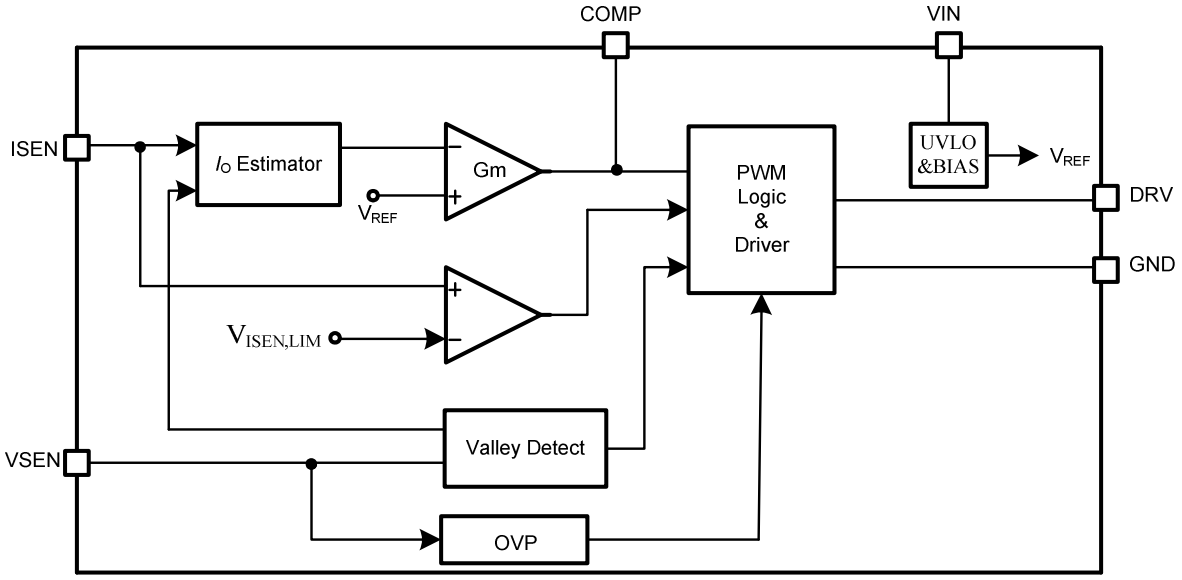


Figure3. Block Diagram

Electrical Characteristics

(V_{IN} = 12V (Note 3), T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
VIN turn-on threshold	$V_{VIN,ON}$			25.3		V
VIN turn-off threshold	$V_{VIN,OFF}$			8.5		V
VIN OVP voltage	$V_{VIN,OVP}$			30.0		V
Start up Current	I_{ST}	$V_{VIN}<V_{VIN,OFF}$		15		μA
Shunt current in OVP mode	$I_{VIN,OVP}$	$V_{VIN}>V_{VIN,OVP}$		4.7		mA
Error Amplifier Section						
Internal reference voltage	V_{REF}			0.3		V
Current Sense Section						
Current limit voltage	$V_{ISEN,LIMIT}$			0.44		V
Protection limit for TR short	$V_{ISEN,EX}$			0.9		V
CC Feedforward coefficient	K_2			0.1		
CC Feedforward resistor	R_{K2}			340		Ω
COMP section						
Pre-charge value	$V_{COMP,LIM}$			1.4		V
VSEN pin Section						
VSEN pin OVP voltage threshold	$V_{VSEN,OVP}$			1.5		V
Fast start up theshold	$V_{VSEN,ST}$			0.55		V
Gate Driver Section						
Gate driver voltage	V_{Gate}			11.7		V
Maximum source current	I_{SOURCE}			0.06		A
Minimum sink current	I_{SINK}			0.25		A
Max ON Time	$T_{ON,MAX}$	V_{COMP}=1.5V		10		μs
Max OFF Time	$T_{OFF,MAX}$			150		μs
Blanking time for ON time	$T_{ON,BLK}$			350		ns
Blanking time for OFF time	$T_{OFF,BLK}$			2		μs
Maximum switching frequency	f_{MAX}			113		kHz
Thermal Section						
Thermal Shutdown Temperature	T_{SD}			150		C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: Increase VIN pin voltage gradually higher than $V_{VIN,ON}$ voltage then turn down to 12V.

Operation

SY5830 is a constant current Flyback controller with primary side control and PFC function that targets at LED lighting applications.

The device provides primary side control to eliminate the opto-couplers or the secondary feedback circuits, which would cut down the cost of the system.

High power factor is achieved by constant on operation mode, with which the control scheme and the circuit structure are both simple.

Start up process is optimized inside SY5830, and quick start up (less than 500ms) is achieved without any additional circuit

In order to reduce the switching losses and improve EMI performance, Quasi-Resonant switching mode is applied, which means to turn on the power MOSFET at voltage valley; the start up current of SY5830 is rather small (15μA typically) to reduce the standby power loss further; the maximum switching frequency is clamped to 125kHz to reduce switching losses and improve EMI performance when the converter is operated at light load condition.

SY5830 provides reliable protections such as Short Circuit Protection (SCP), Open LED Protection (OLP), Over Temperature Protection (OTP), transformer shorted protection and power diode shorted protection, etc.

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SY5830 is available with SOT23-6

Applications Information

Start up

After AC supply or DC BUS is powered on, the capacitor C_{VIN} across VIN and GND pin is charged up by BUS voltage through a start up resistor R_{ST}. Once V_{VIN} rises up to V_{VIN-ON}, the internal blocks start to work and PWM output is enabled.
The output voltage is feedback by VSEN pin, which is taken as V_{FB}. If V_{FBV} is lower than certain threshold $V_{VSEN,ST}$, which means the output voltage is not built up, V_{COMP} is pulled up to high clamped; if V_{FBV} is higher than $V_{VSEN,ST}$, V_{COMP} is under charge of the internal gain modulator.

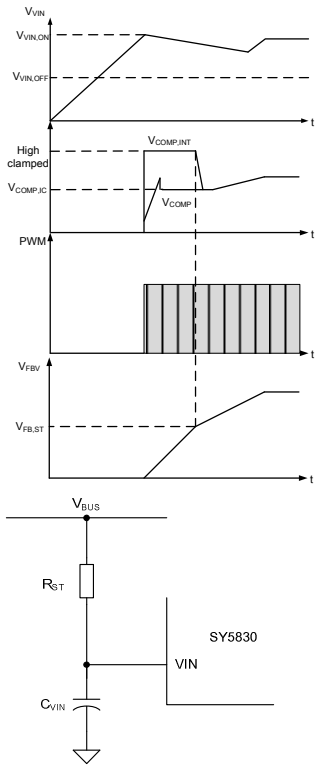


Fig. Start up

This operation is aimed to build up enough output voltage for auxiliary winding bias supply as quickly as possible. It is enabled only one time just when V_{VIN} is over $V_{VIN,ON}$.

V_{COMP} is pre-charged by internal current source to $V_{COMP,IC}$ and hold at this level until fast start up process is finished.

The start up resistor R_{ST} and C_{VIN} are designed by rules below:

(a) Preset start-up resistor R_{ST}, make sure that the current through R_{ST} is larger than I_{ST} and smaller than I_{VIN_OVP}

$$\frac{V_{BUS}}{I_{VIN\_OVP}} < R_{ST} < \frac{V_{BUS}}{I_{ST}}$$

Where V_{BUS} is the BUS line voltage.

(b) Select C_{VIN} to obtain an ideal start up time $t_{ST,}$ and ensure the output voltage is built up at one time.

$$C_{VIN}=\frac{(\frac{V_{BUS}}{R_{ST}}-I_{ST})\times t_{ST}}{V_{VIN\_ON}}$$

(d) If the C_{VIN} is not big enough to build up the output voltage at one time. Increase C_{VIN} and decrease R_{ST}, go back to step (a) and redo such design flow until the ideal start up procedure is obtained.

Shut down

After AC supply or DC BUS is powered off, the energy stored in the BUS capacitor will be discharged. When the auxiliary winding of Flyback transformer can not supply enough energy to VIN pin, V_{VIN} will drop down. Once V_{VIN} is below $V_{VIN-OFF}$, the IC will stop working and V_{COMP} will be discharged to zero.

Primary-side constant-current control

Primary side control is applied to eliminate secondary feedback circuit or opto-coupler, which reduces the circuit cost. The switching waveforms are shown in blow.

The output current I_{OUT} can be represented by,

$$I_{OUT}=\frac{I_{SP}}{2}\times\frac{t_{DIS}}{t_S}$$

Where I_{SP} is the peak current of the secondary side; t_{DIS} is the discharge time of Flyback transformer; t_S is the switching period.

The secondary peak current is related with primary peak current, if the effect of the leakage inductor is neglected.

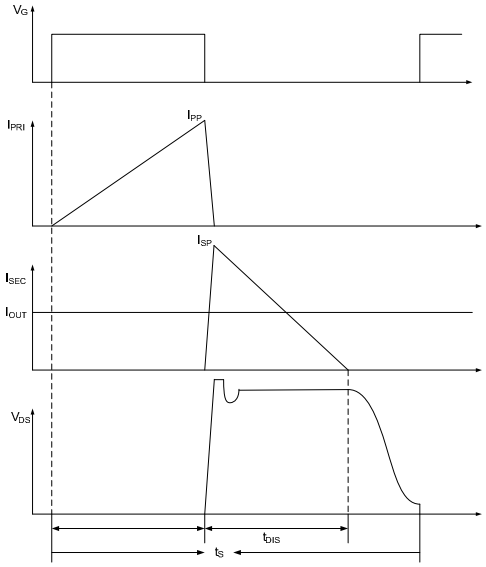


Fig. switching waveforms

$$I_{SP}=N_{PS}\times I_{PP} \quad (4)$$

Where N_{PS} is the turns ratio of primary to secondary of the Flyback transformer.

Thus, I_{OUT} can be represented by

$$I_{OUT}=\frac{N_{PS}\times I_{PP}}{2}\times\frac{t_{DIS}}{t_S}$$

The primary peak current I_{PP} and inductor current discharge time t_{DIS} can be detected by Source and VSEN pin, which is shown in blow. These singals are processed and applied to the negative input of the gain modulator. In static state, the positive and negative inputs are equal

$$V_{REF}=I_{PP}\times R_S\times\frac{t_{DIS}}{t_S}\times k_1$$

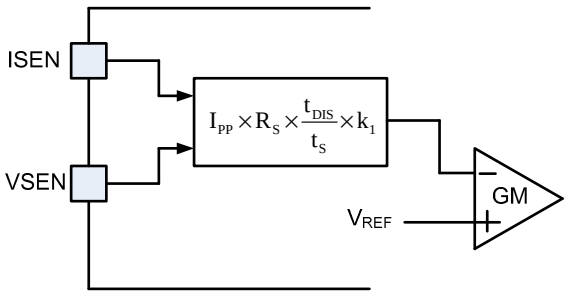


Fig. Output current detection diagram

Finally, the output current I_{OUT} can represented by

$$I_{OUT}=\frac{V_{REF}\times N_{PS}}{R_S\times 2\times k_1}$$

Where k_1 is the output current weight coefficient; V_{REF} is the internal reference voltage; R_S is the current sense resistor.

k_1, and V_{REF} are all internal constant parameters, I_{OUT} can be programmed by N_{PS} and R_S.

$$R_S=\frac{V_{REF}\times N_{PS}}{I_{OUT}\times 2\times k_1}$$

then

$$R_S=\frac{k\times V_{REF}\times N_{PS}}{I_{OUT}},\ k=\frac{1}{2k_1}$$

Quasi-Resonant Operation

QR mode operation provides low turn-on switching losses for Flyback converter.

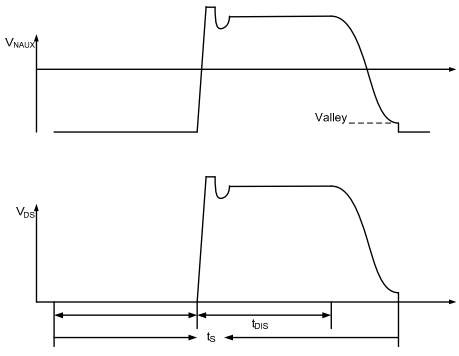


Fig. QR mode operation

The voltage across drain and source of the primary MOSFET is reflected by the auxiliary winding of the Flyback transformer. VSEN pin detects the voltage across the auxiliary winding by a resistor divider. When the voltage across drain and source of the primary MOSFET is at voltage valley, the MOSFET would be turned on.

Over Voltage Protection (OVP) & Open LED Protection (OLP)

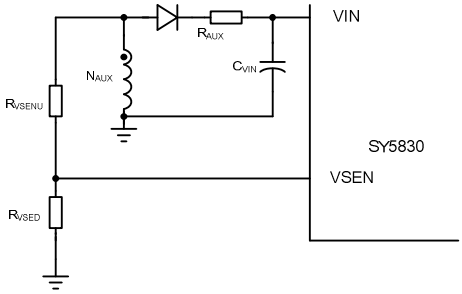


Fig. OVP&OLP

The output voltage is reflected by the auxiliary winding voltage of the Flyback transformer, and both VSEN pin and VIN pin provide over voltage protection function. When the load is null or large transient happens, the output voltage will exceed the rated value. When V_{VIN} exceeds $V_{VIN,OVP}$ or V_{VSEN} exceeds $V_{VSEN,OVP}$, the over voltage protection is triggered and the IC will discharge V_{VIN} by an internal current source $I_{VIN,OVP}$. Once V_{VIN} is below $V_{VIN,OFF}$, the IC will shut down and be charged again by BUS voltage through start up resistor. If the over voltage condition still exists, the system will operate in hiccup mode.

Thus, the turns of the auxiliary winding N_{AUX} and the resistor divider is related with the OVP function.

$$\frac{V_{SEN\_OVP}}{V_{OVP}}=\frac{R_{VSEND}}{R_{VSENU}+R_{VSEND}}$$

$$\frac{V_{VIN\_OVP}}{V_{OVP}}\geq\frac{N_{AUX}}{N_S}$$

Where V_{OVP} is the output over voltage specification; R_{VSENU} and R_{VSEND} compose the resistor divider. The turns ratio of N_S to N_{AUX} and the ratio of R_{VSENU} to R_{VSEND} could be induced from equation above.

Short Circuit Protection (SCP)

When the output is shorted to ground, the output voltage is clamped to zero. The voltage of the auxiliary winding is proportional to the output winding, so valley signal cannot be detected by VSEN. Without valley detection, MOSFET cannot be turned ON until maximum off time $t_{OFF,MAX}$ is matched. If MOSFET is turned ON by $t_{OFF,MAX}$ 64

times continuously, IC will be shut down and enter into hiccup mode.

If the output voltage is not low enough to disable valley detection in short condition, V_{VIN} will drop down without auxiliary winding supply. Once V_{VIN} is below $V_{VIN,OFF}$, the IC will shut down and be charged again by the BUS voltage through the start up resistor. If the short circuit condition still exists, the system will operate in hiccup mode.

Line regulation modification

The IC provides line regulation modification function to improve line regulation performance.

Due to the sample delay of ISEN pin and other internal delay, the output current increases with increasing input BUS line voltage. A small compensation voltage $\Delta V_{ISEN,C}$ is added to ISEN pin during ON time to improve such performance. This ΔV_{ISEN-C} is adjusted by the upper resistor of the divider connected to VSEN pin and external resistor $R_{ISEN,C}$ on ISEN pin.

$$\Delta V_{ISEN,C} = V_{BUS} \times \frac{N_{AUX}}{N_P} \times \frac{1}{R_{VSENU}} \times k_2 \times (R_{k2} + R_{ISEN,C})$$

Where R_{VSENU} is the upper resistor of the divider; k_2 is an internal constant as the modification coefficient; R_{k2} is an internal feed-forward resistor; auxiliary resistor $R_{ISEN,C}$ can be added to enhance feed-forward effects.

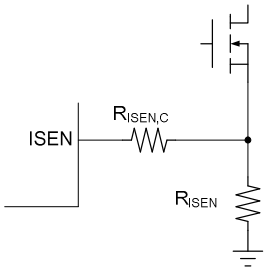


Fig. feed-forward resistor

Single fault design

If VSEN pin is shorted to GND pin or floating, valley detection is failed, which is similar to SLP, the system will operate in hiccup mode.

If the transformer is shorted, V_{ISEN} will exceeds $V_{ISEN,EX}$, which will trigger IC latch operation. In latch mode, IC won't work unless AC source restarts.

The protection above is also suitable for secondary diode short.

Power Device Design

MOSFET and Diode

When the operation condition is with maximum input voltage and full load, the voltage stress of MOSFET and secondary power diode is maximized;

$$V_{MOS\_DS\_MAX} = \sqrt{2}V_{AC\_MAX} + N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S$$

$$V_{D\_R\_MAX} = \frac{\sqrt{2}V_{AC\_MAX}}{N_{PS}} + V_{OUT}$$

Where $V_{AC,MAX}$ is maximum input AC RMS voltage; N_{PS} is the turns ratio of the Flyback transformer; V_{OUT} is the rated output voltage; $V_{D,F}$ is the forward voltage of secondary power diode; ΔV_S is the overshoot voltage clamped by RCD snubber during OFF time.

When the operation condition is with minimum input voltage and full load, the current stress of MOSFET and power diode is maximized.

$$I_{MOS\_PK\_MAX} = I_{P\_PK\_MAX}$$
$$I_{MOS\_RMS\_MAX} = I_{P\_RMS\_MAX}$$
$$I_{D\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX}$$
$$I_{D\_AVG} = I_{OUT}$$

Where $I_{P\text{-}PK\text{-}MAX}$ and $I_{P\text{-}RMS\text{-}MAX}$ are maximum primary peak current and RMS current, which will be introduced later.

Transformer (N_{PS} and L_M)

N_{PS} is limited by the electrical stress of the power MOSFET:

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - \sqrt{2}V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}}$$

Where $V_{MOS,(BR)DS}$ is the breakdown voltage of the power MOSFET.

In Quasi-Resonant mode, each switching period cycle t_S consists of three parts: current rising time t_1, current falling time t_2 and quasi-resonant time t_3 shown in blow.

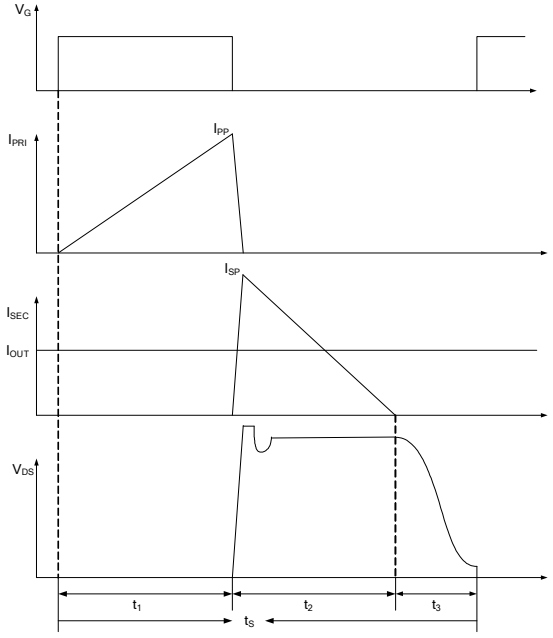


Fig. switching waveforms

The system operates in the constant on time mode to achieve high power factor. The ON time increases with the input AC RMS voltage decreasing and the load increasing. When the operation condition is with minimum input AC RMS voltage and full load, the ON time is maximized. On the other hand, when the input voltage is at the peak value, the OFF time is maximized. Thus, the minimum switching frequency $f_{S\text{-}MIN}$ happens at the peak value of input voltage with minimum input AC RMS voltage and maximum load condition; Meanwhile, the maximum peak current through MOSFET and the transformer happens.

Once the minimum frequency $f_{S\text{-}MIN}$ is set, the inductance of the transformer could be induced. The design flow is shown as below:

(a) Select N_{PS}

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - \sqrt{2}V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}}$$

(b) Preset minimum frequency $f_{S\text{-}MIN}$

(c) Compute relative t_S, t_1 (t_3 is omitted to simplify the design here)

$$t_S = \frac{1}{f_{S\_MIN}}$$

$$t_1 = \frac{t_S \times N_{PS} \times (V_{OUT} + V_{D\_F})}{\sqrt{2}V_{AC\_MIN} + N_{PS} \times (V_{OUT} + V_{D\_F})}$$

(d) Design inductance L_M

$$L_M = \frac{V_{AC\_MIN}^2 \times t_1^2 \times \eta}{2P_{OUT} \times t_S}$$

(e) Compute t_3

$$t_3 = \pi \times \sqrt{L_M \times C_{Drain}}$$

Where C_{Drain} is the parasitic capacitance at drain of MOSFET.

(f) Compute primary maximum peak current $I_{P\text{-}PK\text{-}MAX}$ and RMS current $I_{P\text{-}RMS\text{-}MAX}$ for the transformer fabrication.

$$I_{P\_PK\_MAX} = \frac{2P_{OUT} \times [\frac{L_M}{\sqrt{2}V_{AC\_MIN}} + \frac{L_M}{N_{PS} \times (V_{OUT} + V_{D\_F})}]}{L_M \times \eta} + \frac{\sqrt{4P_{OUT}^2 \times [\frac{L_M}{\sqrt{2}V_{AC\_MIN}} + \frac{L_M}{N_{PS} \times (V_{OUT} + V_{D\_F})}]^2 + 4L_M \times \eta \times P_{OUT} \times t_3}}{L_M \times \eta}$$

Where η is the efficiency; P_{OUT} is rated full load power

Adjust t_1 and t_S to t_1' and t_S' considering the effect of t_3

$$t_S' = \frac{\eta \times L_M \times I_{P\_PK\_MAX}^2}{4P_{OUT}}$$

$$t_1' = \frac{L_M \times I_{P\_PK\_MAX}}{\sqrt{2}V_{AC\_MIN}}$$

$$I_{P\_RMS\_MAX} \approx \sqrt{\frac{t_1'}{6t_S'}} \times I_{P\_PK\_MAX}$$

(g) Compute secondary maximum peak current $I_{S\text{-}PK\text{-}MAX}$ and RMS current $I_{S\text{-}RMS\text{-}MAX}$ for the transformer fabrication.

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX}$$

$$t_2' = t_S' - t_1' - t_3$$

$$I_{S\_RMS\_MAX} \approx \sqrt{\frac{t_2'}{6t_S'}} \times I_{S\_PK\_MAX}$$

Transformer design (N_P,N_S,N_{AUX})

The design of the transformer is similar with ordinary Flyback transformer. the parameters below are necessary:

Necessary parameters	
Turns ratio	N_{PS}
Inductance	L_M
Primary maximum current	$I_{P\text{-}PK\text{-}MAX}$
Primary maximum RMS current	$I_{P\text{-}RMS\text{-}MAX}$
Secondary maximum RMS current	$I_{S\text{-}RMS\text{-}MAX}$

The design rules are as followed:

(a) Select the magnetic core style, identify the effective area A_e.

(b) Preset the maximum magnetic flux ΔB

ΔB=0.22~0.26T

(c) Compute primary turn N_P

$$N_p = \frac{L_M \times I_{P\_PK\_MAX}}{\Delta B \times A_e}$$

(d) Compute secondary turn N_S

$$N_S = \frac{N_P}{N_{PS}}$$

(e) compute auxiliary turn N_{AUX}

$$N_{AUX} = N_S \times \frac{V_{VIN}}{V_{OUT}}$$

Where V_{VIN} is the working voltage of VIN pin (10V~11V is recommended).

(f) Select an appropriate wire diameter

With $I_{P\text{-}RMS\text{-}MAX}$ and $I_{S\text{-}RMS\text{-}MAX}$, select appropriate wire to make sure the current density ranges from 4A/mm^2 to 10A/mm^2.

(g) If the winding area of the core and bobbin is not enough, reselect the core style, go to **(a)** and redesign the transformer until the ideal transformer is achieved.

Output capacitor C_{OUT}

Preset the output current ripple ΔI_{OUT}, C_{OUT} is induced by

$$C_{OUT} = \frac{\sqrt{(\frac{2I_{OUT}}{\Delta I_{OUT}})^2 - 1}}{4\pi f_{AC} R_{LED}}$$

Where I_{OUT} is the rated output current; ΔI_{OUT} is the demanded current ripple; f_{AC} is the input AC supply frequency; R_{LED} is the equivalent series resistor of the LED load.

RCD snubber for MOSFET

The power loss of the snubber P_{RCD} is evaluated first

$$P_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{\Delta V_S} \times \frac{L_K}{L_M} \times P_{OUT}$$

Where N_{PS} is the turns ratio of the Flyback transformer; V_{OUT} is the output voltage; $V_{D\text{-}F}$ is the forward voltage of the power diode; ΔV_S is the overshoot voltage clamped by RCD snubber; L_K is the leakage inductor; L_M is the inductance of the Flyback transformer; P_{OUT} is the output power.

The R_{RCD} is related with the power loss:

$$R_{RCD} = \frac{(N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S)^2}{P_{RCD}}$$

The C_{RCD} is related with the voltage ripple of the snubber $\Delta V_{C\text{-}RCD}$:

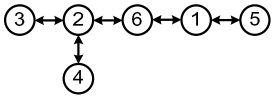
$$C_{RCD} = \frac{N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S}{R_{RCD} f_S \Delta V_{C\_RCD}}$$

Layout

(a) To achieve better EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to the BUS line capacitor first, then to the switching circuit.

(b) The circuit loop of all switching circuit should be kept small: primary power loop, secondary loop and auxiliary power loop.

(c) The connection of primary ground is recommended as:



Ground ①: ground of BUS line capacitor
Ground ②: ground of bias supply capacitor
Ground ③: ground node of auxiliary winding
Ground ④: ground of signal trace
Ground ⑤: primary ground node of Y capacitor
Ground ⑥: ground node of current sample resistor.

(d) bias supply trace should be connected to the bias supply capacitor first instead of GND pin. The bias supply capacitor should be put beside the IC.

(e) Loop of 'Source pin – current sample resistor – GND pin' should be kept as small as possible.

(f) The resistor divider connected to VSEN pin is recommended to be put beside the IC.

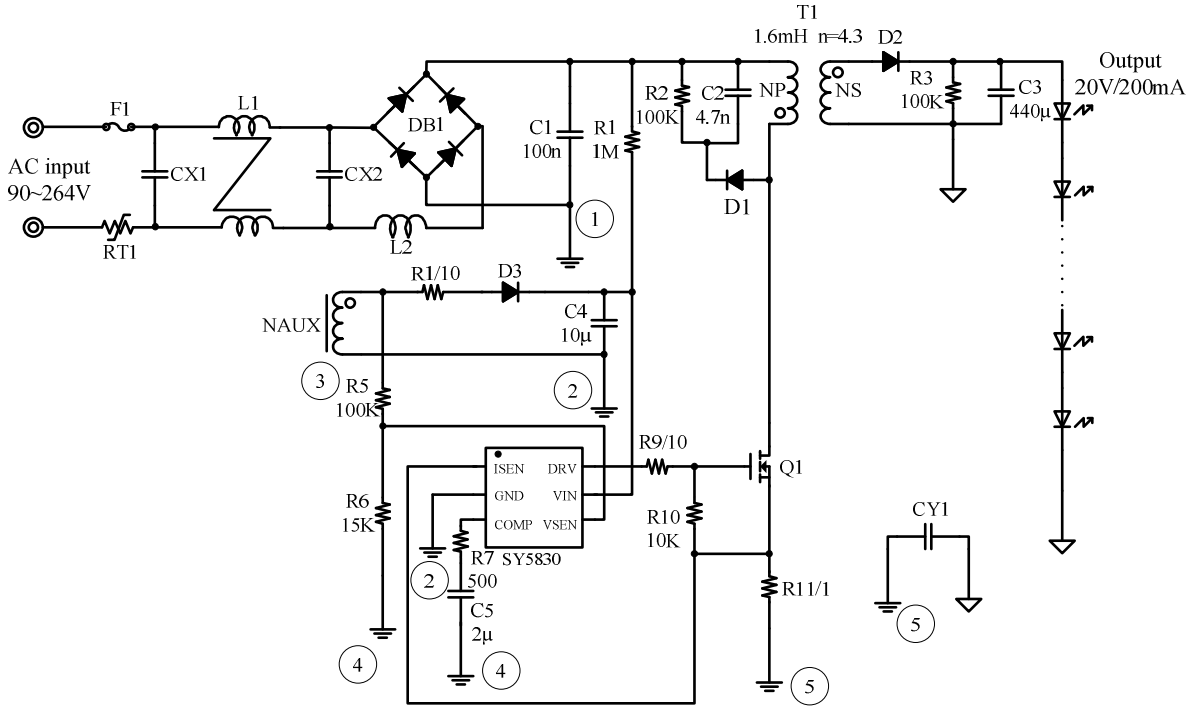
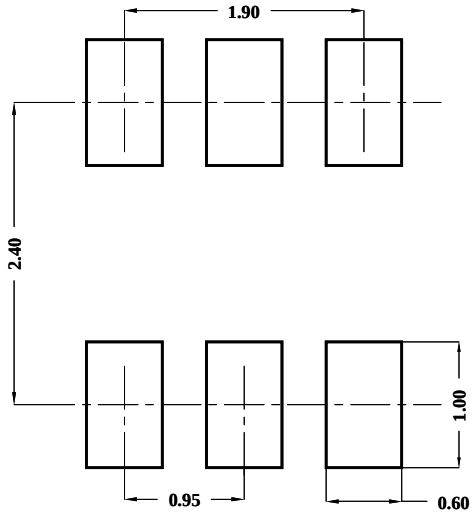
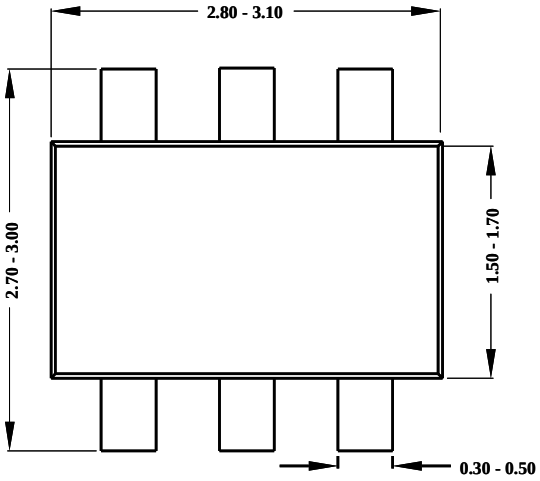


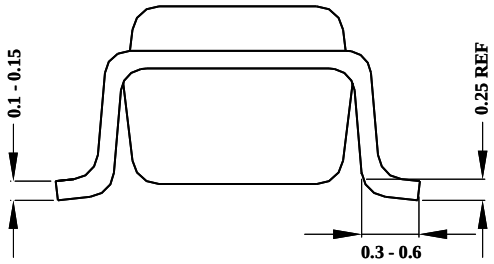
Fig. Ground connection recommended

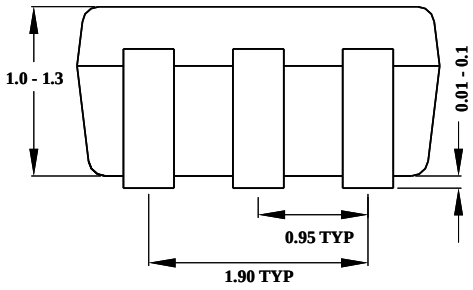
SOT23-6 Package outline & PCB layout design



Recommended Pad Layout







Notes: All dimensions are in millimeters.
All dimensions don't include mold flash & metal burr.