SY58627L

DC-to-6.4Gbps Backplane Receive Buffer with Four Stage Programmable Equalization and DC-Offset Control

Preliminary

General Description

The SY58627L high-speed, low jitter receive buffer is optimized for backplane and transmission line data-path management applications. The SY58627L is capable of receiving serial data up to 6.4Gbps across up to 36 inches of FR4.

The SY58627L differential input includes Micrel's unique, 3-pin input termination architecture that directly interfaces to any differential signal as small as $100mV_{pk}$ (AC- or DC-coupled) without any termination resistor networks in the signal path. The outputs are 50Ω source-terminated CML optimized to drive $400mV_{pk}$ into 50Ω (100Ω load across the output pair). The I/O termination is connected to a dedicated VTT pin for added bias flexibility.

The SY58627L receiver input provides four levels of equalization to compensate for degraded signals resulting from transmission losses. The equalization is programmed with a three-bit interface.

The SY58627L operates at 3.3V ±10% supply and is guaranteed over the full industrial temperature range of -40°C to +85°C. The SY58627L is part of Micrel's high-speed, Precision Edge® product line.

All data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Precision Edge®

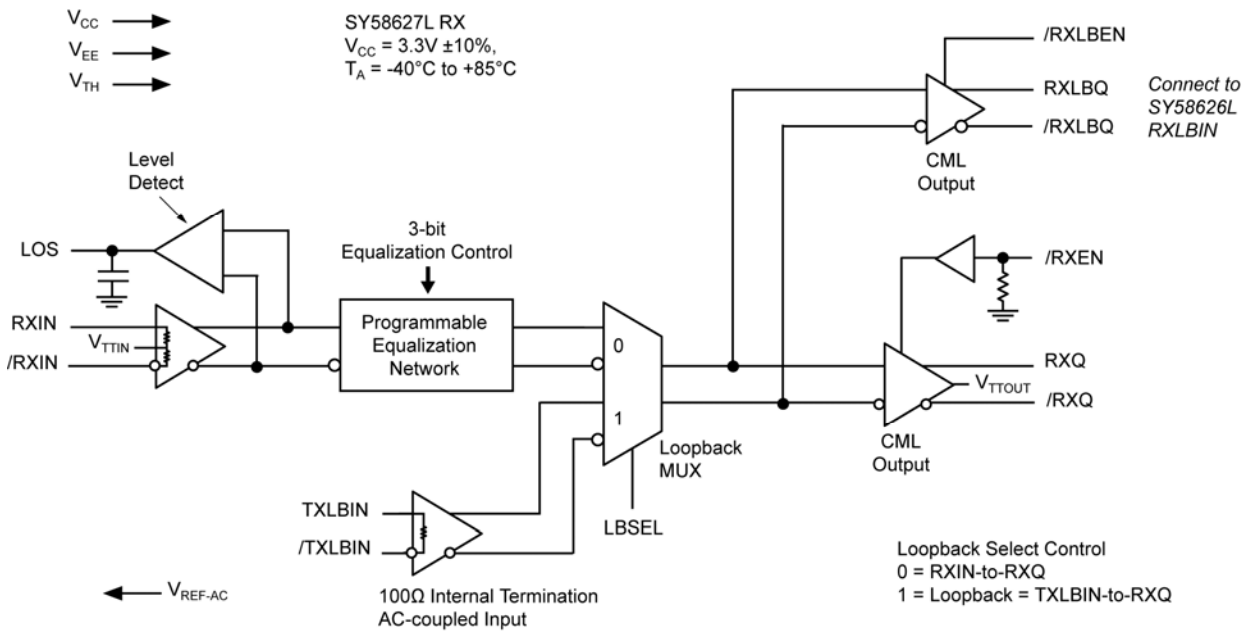
Features

- Selectable equalizing network to optimize incoming data eye pattern
- Four selectable equalization levels
- Receives up to 36" FR4 PCB trace, or longer combinations of FR4+cable+interconnect
- DC through 6.4Gbps data rate throughput
- Integrated loopback capability
- Unique, flexible I/O:
  - Patented, Internal termination to VTTIN pin interfaces to any differential AC- or DC-coupled signals
  - 50Ω source-terminated CML outputs minimize round-trip reflections
  - Wide input voltage range: 100mV to $1.3V_{PK}$
  - Output disable
  - DC-offset control with VTT I/O
- Input Loss-of-Signal
  - Hysteresis included
- 3.3V ±10% supply voltage
- -40°C to +85°C temperature range
- Available in 32-pin (5mm x 5mm) MLF™ package

Applications

- ATE, T&M backplane management
- Serial backplane management
- Combination FR4+cable+interconnect receiver
- Fibre Channel, GigE, SONET/SDH data transmission
- Electrical interface and interconnect applications that require DC-offset control

Functional Block Diagram



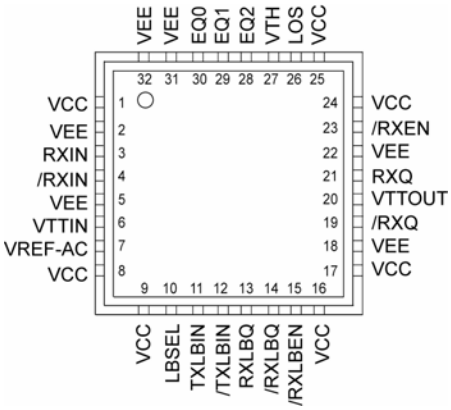
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY58627LMG	MLF-32	Industrial	SY58627L with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY58627LMGTR[2]	MLF-32	Industrial	SY58627L with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at TA = 25°C, DC Electricals only.
2. Tape and Reel.

Pin Configuration



32-Pin MLF™ (MLF-32)

Pin Description

Pin Number	Pin Name	Pin Function
3, 4	RXIN, /RXIN	Differential receiver input pair: This input pair is the differential signal input to the device. It accepts AC- or DC-coupled signals as small as 100mV (200mV$_{PP}$). The loss-of-signal (LOS Level) includes a small amount of hysteresis to prevent the loss-of-signal output from oscillating when no signal is present. RXIN and /RXIN internally terminate to the VTTIN pin through 50Ω. Please refer to the "Input Interface Applications" section for more details. RXIN, /RXIN differential inputs recommended be ≥ 90mV$_{PK}$ to ensure valid outputs. Consider disabling the outputs when the differential input is not present, or < 90mV$_{PK}$ (e.g.: Hot Swap Applications).
6	VTTIN	Input termination center-tap: RXIN and /RXIN terminate to VTTIN. The VTTIN pin provides a center-tap to the internal termination network for maximum interface flexibility, and DC-offset capability. Please refer to the "Input Interface Applications" section for more details.
7	VREF-AC	Reference voltage: This output biases to V_{CC}-0.84V. It is used for AC-coupling the input pair (RXIN, /RXIN). Connect VREF-AC directly to the VTTIN pin. Bypass with 0.01µF low ESR capacitor to VCC. Maximum sink/source current is ±1.5mA. Due to the limited drive capability, the VREF-AC pin is only intended to drive the VTTIN pin. Leave VREF-AC pin floating when not used. Please refer to the "Input Interface Applications" section for more details.
27	VTH	Input logic threshold control voltage for logic control threshold settings other than LVTTL/CMOS. This input control pin can be externally biased to set the proper threshold for all the logic control pins, /RXEN, LBSEL, 3-bit equalization control, and /RXLBEN. For standard LVTTL/CMOS control, simply leave the VTH pin floating and the threshold voltage defaults to V_{CC}/2 (When V_{EE} = 0V). For LVPECL thresholds, set VTH to V_{CC}-1.3V.
23	/RXEN	TTL/CMOS (or VTH controlled) compatible control input for the RXQ output pair. When pulled HIGH, the RXQ output pair is disabled. This input is internally connected to a 25kΩ pull-down resistor and will default to a logic LOW state (Enable) if left open. When disabled, the RXQ output goes LOW, and /RXQ output goes HIGH. Default threshold is V_{CC}/2 when VTH pin is floating.
15	/RXLBEN	TTL/CMOS (or VTH controlled) compatible control input for RXLBQ output pair. When pulled HIGH, the RXLBQ output pair is disabled. This input is internally connected to a 25kΩ pull-down resistor and will default to a logic LOW state (Enable) if left open. When disabled, the RXLBQ output goes LOW, and /RXLBQ output goes HIGH. Default threshold is V_{CC}/2 when VTH pin is floating. In normal operating mode, when the RXLBQ output pair is not needed, disable the RXLBQ output pair (/RXLBEN = HIGH) to minimize noise.
10	LBSEL	Loopback MUX select control: The TTL/CMOS (or VTH controlled) compatible input selects the input to the Loopback mode multiplexer. When LBSEL input is logic HIGH, Loopback mode is selected, and the TXLBIN input pair is selected to pass through the RXQ and RXLBQ output pairs. Note that the LBSEL pin is internally connected to a 25kΩ pull-down resistor and will default to a logic LOW state if left open (normal operation). The Loopback MUX includes internal input isolation to minimize crosstalk.
11, 12	TXLBIN, /TXLBIN	Loopback differential input pair: AC-coupled, CML-compatible input. This input pair includes internal termination connected to an internal VBB for an AC-coupled bias configuration. For local Loopback operation, the TXLBIN input pair receives a signal from the SY58626L transmitter TXLBQ output pair. The input signal from TXLBIN does not have any equalization. When the SY58627L Loopback mode is selected (LBSEL = HIGH), the signal at TXLBIN is directed to the RXQ and RXLBQ output pairs.

Pin Description (Continued)

Pin Number	Pin Name	Pin Function
13, 14	RXLBQ, /RXLBQ	Receiver loopback CML compatible output pair. When the SY58627L is in local Loopback mode (LBSEL = 1), RXLBQ output is directed from TXLBIN (no equalization). When the SY58627L is in normal mode (LBSEL = LOW) and the RXLBQ output is not required, disable the RXLBQ output (/RXLBEN = HIGH) to minimize switching noise. This differential output pair is optimized to drive 400mV$_{PK}$ swing into a 50Ω load (100Ω across the pair). The RXLBQ output pair includes 50Ω internal source termination resistors.
21, 19	RXQ, /RXQ	Receiver differential CML compatible output pair: This CML-compatible output pair is the equalized signal seen at the RXIN input pair and is optimized to drive 400mV$_{PK}$ swing into a 50Ω load (100Ω across the pair). The RXQ output pair includes 50Ω internal source termination resistors. When the SY58627L is in Loopback mode (LBSEL = HIGH), then the RXQ output signal is directed from the unequalized TXLBIN input.
26	LOS	Please contact factory Applications Engineers.
20	VTTOUT	Output termination center-tap: Each side of the RXQ differential output pair terminates to the VTTOUT pin through 50Ω. The VTTOUT pin provides a center-tap to the output termination network for maximum interface flexibility, and DC-offset capability. Please refer to the “CML Output Interface Applications” section for more details.
28 29 30	EQ2(MSB) EQ1 EQ0	TTL/CMOS (or VTH controlled) compatible, 3-bit control interface. There are four levels of equalization, as shown in the “Equalization Select Truth Table.” When the MSB is logic HIGH, the RXQ output pair will not include any equalization. 000 = lowest equalization setting 001 = medium equalization setting 010 = medium-high equalization setting 011 = highest equalization setting 1XX = equalization bypass
1, 8, 9, 16, 17, 24, 25	VCC	Positive Power Supply: Connect to +3.3V power supply. Bypass with 0.1µF//0.01µF low ESR capacitors as close to VCC pins as possible.
2, 5, 18, 22, 31, 32	VEE, Exposed Pad	Ground: Ground pins and exposed pad must be connected to the same ground plane.

Equalization Select Truth Table

Disable EQ (MSB = EQ2)	Equalization Select (EQ1)	Equalization Select (EQ0)	Typical FR4 Length	Equalization
0	0	0	9”	Low
0	0	1	18”	Medium Low
0	1	0	24”	Medium High
0	1	1	36”	High
1	X	X	NA	Disabled

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... -0.5V to +4.0V
Input Voltage (V_{IN}) ..... -0.5V to V_{CC}
Input Current (RXIN, /RXIN, ≤120mins) 67mA
CML Output Current (I_{OUT})
  Continuous (≤120mins) 67mA
  Surge 100mA
Termination Current
  V_T ..... ±100mA
V_{REF-AC} Current
  Source/sink current on V_{REF-AC} ..... ±2mA
Lead Temperature (soldering, 20 sec.) ..... +260°C
Storage Temperature (T_S) ..... -65°C to 150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... +3.0V to +3.6V
Ambient Temperature (T_A) ..... -40°C to +85°C
Package Thermal Resistance[3]
MLF™ (θ_{JA})
  Still-Air ..... 34°C/W
MLF™ (Ψ_{JB})
  Junction-to-Board ..... 20°C/W

DC Electrical Characteristics[4]

T_A = -40°C to +85°C; unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply		3.0	3.3	3.6	V
I_{EE}	Power Supply Current	Max V_{CC}, includes 50Ω internal source resistors, no external load current		210	260	mA
R_{IN}	Input Resistance (RXIN-to-VTTIN)		45	50	55	Ω
R_{DIFF_IN}	Differential Input Resistance (RXIN-to-/RXIN)		90	100	110	Ω
V_{IN_TRANS}	Transmission Line Input Voltage Swing (RXIN, /RXIN)	Input signal swing applied to transmission line input up to 36 in. (driver side of RXIN)	0.20			V_{PK}
V_{IN}	Input Voltage Swing (RXIN, /RXIN)	See Figure 4a.	0.1		1.3	V_{PK}
V_{DIFF_IN}	Differential Input Voltage Swing |RXIN-/RXIN|	See Figure 4b.	0.2			V_{PP}
V_{IH}	Input High Voltage (RXIN, /RXIN)		V_{EE}+1.6		V_{CC}	V
V_{IL}	Input LOW Voltage (RXIN, /RXIN)		V_{EE}+1.4		V_{IH}-0.1	V
V_{TTIN}	RXIN-to-VTTIN (RXIN, /RXIN)				1.5	V
V_{TTIN} Range	VTTIN Voltage Range	Voltage applied to VTTIN pin	V_{CC}-1.5		V_{CC}+1.5	V
V_{TTOUT} Range	VTTOUT Voltage Range	Voltage applied to VTTOUT pin	V_{CC}-0.4		V_{CC}	V
LOS	Loss-of-Signal Input Levels	LOS Assert		Note 5		mV_{PK}
		LOS De-assert		Note 5		
	Input Return Loss	100MHz to 3.5GHz		10		dB
V_{REF-AC}	Output Reference Voltage		V_{CC}-0.95	V_{CC}-0.84	V_{CC}-0.7	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. θ_{JA} and Ψ_{JB} values are determined for a 4-layer board in still air unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. $T_J \leq 125°C$.
5. Please contact factory Applications Engineers.

RXQ and RXLBQ Output DC Electrical Characteristics[6]

V_{CC} = 3.3V ±10%; V_{EE} = 0V; T_A = -40°C to + 85°C; R_L = 100Ω across output pair; unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	RXQ & RXLBQ Output High Voltage	R_L = 50Ω to Vcc	V_{CC}-0.040	V_{CC}-0.010	V_{CC}	V
V_{OUT}	Output Voltage Swing (RXQ, /RXQ) (RXLBQ, /RXLBQ)	See Figure 4a.	325	400		mV_{PK}
V_{DIFF_OUT}	RXQ & RXLBQ Differential Output Voltage Swing |RXQ-/RXQ| |RXLBQ-/RXLBQ|	See Figure 4b.	650	800		mV_{PP}
R_{OUT}	Output Impedance		45	50	55	Ω

Logic Control DC Electrical Characteristics[6]

V_{CC} = 3.3V ±10%; V_{EE} = 0V; T_A = -40°C to + 85°C; unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage	All control input pins	V_{TH}+0.2		V_{CC}	V
V_{IL}	Input LOW Voltage	All control input pins	V_{EE}		V_{TH}–0.2	V
I_{IH}	Input HIGH Current				300	µA
I_{IL}	Input LOW Current		-300			µA
V_{TH}	Threshold Input Voltage	Voltage applied to pin (V_{EE} = 0V)	1.4	V_{CC}/2	2.6	V

TXLBIN Input DC Electrical Characteristics[6]

V_{CC} = 3.3V ±10%; V_{EE} = 0V; T_A = -40°C to + 85°C; R_L = 100Ω across output pair; unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
R_{DIFF_IN}	Differential Input Resistance (TXLBIN-to-/TXLBIN)		90	100	110	Ω
V_{IN}	Input Voltage Swing (TXLBIN, /TXLBIN)	See Figure 4a.	0.1		1.3	V_{PK}
V_{DIFF_IN}	Differential Input Voltage Swing |TXLBIN-/TXLBIN|	See Figure 4b.	0.2			V_{PP}

Notes:

6. The circuit is designed to meet the DC specifications, shown in the above table, after thermal equilibrium has been established. 500lfpm Airflow. $T_J \leq 125°C$.

AC Electrical Characteristics[7]

V_{CC} = 3.3V ±10%; V_{EE} = 0V; T_A = -40°C to + 85°C; R_L = 100Ω across output pair; unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
Freq	Data Rate Throughput (RXQ & RXLBQ)	NRZ Data	DC		6.4	Gbps
t_{pd}	Differential Propagation Delay	RXIN-to-RXQ, no equalization	150	250	450	ps
		TXLBIN-to-RXQ		250		ps
t_{EN}	RXQ Enable/Disable Time	/RXEN		425	650	ps
t_{LB_EN}	RXLBQ Enable/Disable Time	/RXLBEN		425		ps
t_{LBSEL}	Loopback Select Time	LBSEL		350	600	ps
t_{PROG}	Programming Logic Control Time	3-bit equalization control update-to-valid RXQ		1		ns
t_{pd} Tempco	Differential Propagation Delay Temperature Coefficient			120		fs/°C
t_{SKEW}	Part-to-Part Skew	Note 8			200	ps
t_{JITTER}	Random Jitter (RJ)	Note 9			Note 11	ps_{RMS}
	Deterministic Jitter (DJ)	Note 10			Note 11	ps_{PP}
t_r, t_f	Output Rise/Fall Time (20% to 80%)	At full output swing	20	50	80	ps

Notes:

7. High-frequency AC-parameters are guaranteed by design and characterization.
8. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.
9. Random jitter is measured with a K28.7 pattern at: ≤6.4Gbps.
10. Deterministic jitter is measured with both K28.5 and 2^{23}-1 PRBS pattern, at 4.25Gbps/6.4Gbps.
11. Contact factory for updated random jitter and deterministic jitter limits.

Detailed Description

The SY58627L is a high speed, low jitter receive buffer with integrated loopback capability. This buffer also provides input signal detect and output disable. Four selectable levels of equalization are included with the receiver. Equalization allows for faster data rates and longer distances by reducing the effects of intersymbol interference (ISI) caused by long cable and trace lengths. Input equalization supports data rates up to 6.4Gbps.

DC-Offset Capability

The SY58627L transmitter includes the VTTIN and VTTOUT pin for maximum interface flexibility and DC-offset capability for the input and output, respectively. This feature allows for interfacing with different logic families without the use of AC-coupling. The output buffer has internal 50Ω source terminated CML outputs for minimizing round-trip reflections.

Transmitter Disable and Shutdown

The SY58627L disable function is initiated by pulling /RXEN to logic HIGH. In disable mode, RXQ goes to a LOW state and /RXQ goes to a HIGH state. The threshold for /RXEN is set with the VTH pin. When the VTH pin is floating, the VTH levels are TTL/CMOS-compatible with a threshold voltage at $V_{CC}/2$ (V_{EE} = 0V). For PECL compatible levels, apply a V_{CC}-1.3V voltage at the VTH pin. Please refer to, "Typical Operating Characteristics" for more details.

Loopback

The SY58627L features a loopback test mode, activated by setting LBSEL to logic HIGH. Using the SY58627L with the SY58626L enables local loopback and link side loopback, shown in Figures 2b and 2c. This mode enables an external loopback path, bypassing circuitry on both local and link side. Please refer to Table 1 and Figure 3 for Loopback Control information.

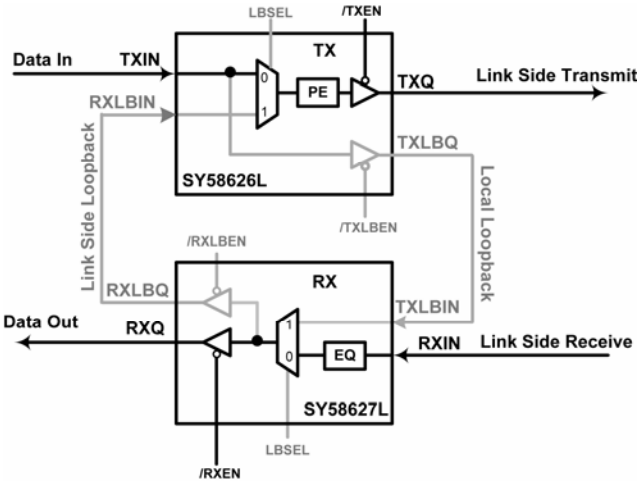


Figure 2a. Normal Operation

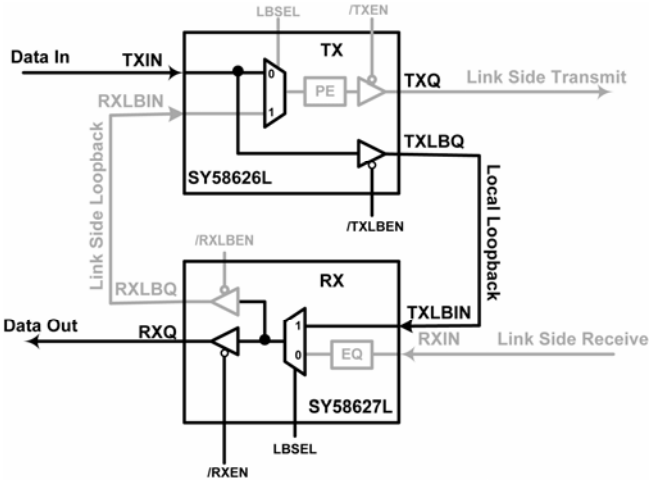


Figure 2b. Local Loopback Mode

hbwhelp@micrel.com or (408) 955-1690

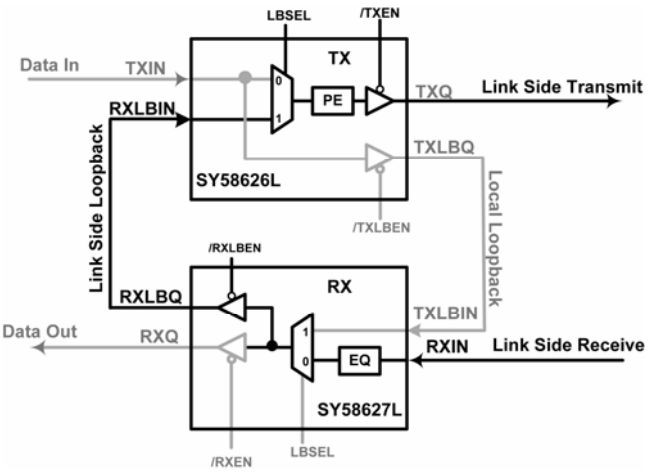


Figure 2c. Link Side Loopback Mode

	LBSEL	/RXLBEN	/RXEN	RXQ	RXLBQ
Normal Mode	0	0	0	RXIN	RXIN
	0	0	1	0	RXIN
	0	1	0	RXIN	0
	0	1	1	0	0
Link Side Loopback Mode	1	0	0	TXLBIN	TXLBIN
	1	0	1	0	TXLBIN
	1	1	0	TXLBIN	0
	1	1	1	0	0

Table 1. Transmit Loopback Control Signal

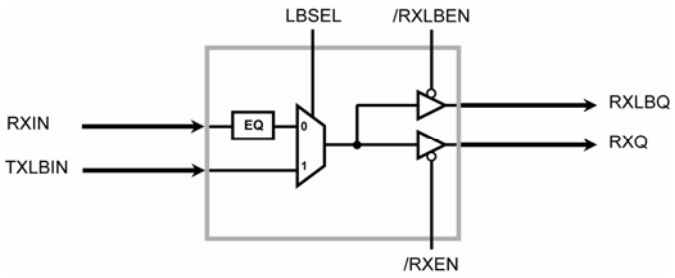


Figure 3. Loopback Control

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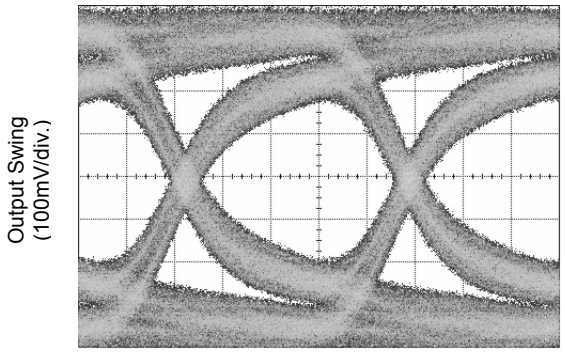
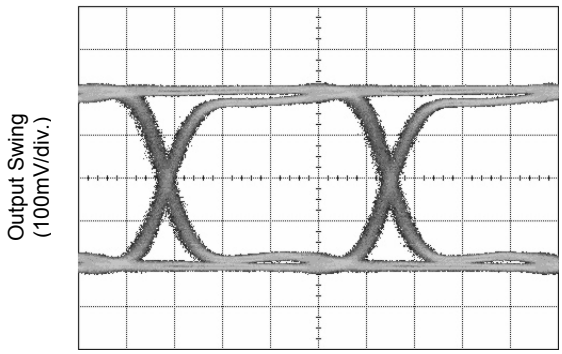
Typical Operating Characteristics

V_{CC} = 3.3V ±10%; V_{IN} > 400mV; T_A = 25°C, R_L = 100Ω across output pair; unless otherwise stated.

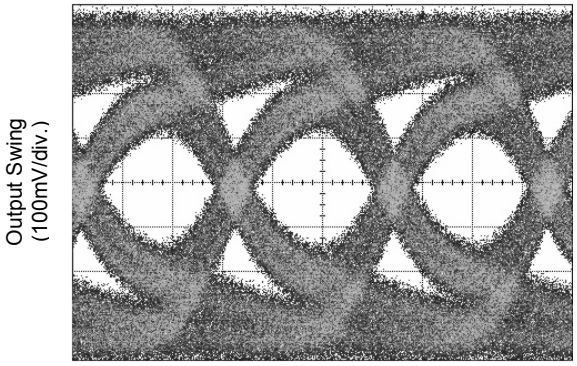
8in FR4 Output without SY58627L (4.25Gbps PRBS 2^{23})



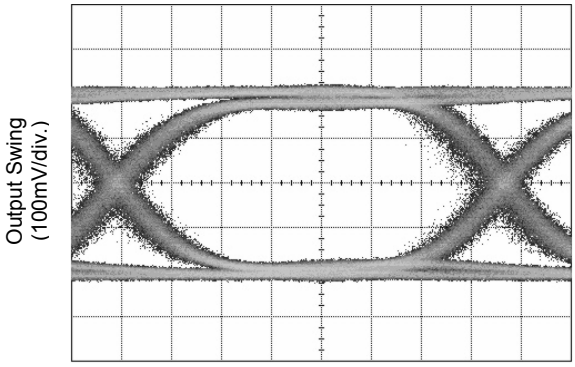
8in FR4 Output with SY58627L (4.25Gbps PRBS 2^{23})



8in FR4 Output without SY58627L (6.4Gbps PRBS 2^{23})



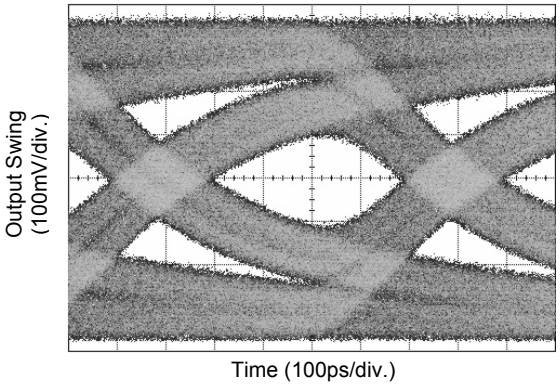
8in FR4 Output with SY58627L (6.4Gbps PRBS 2^{23})



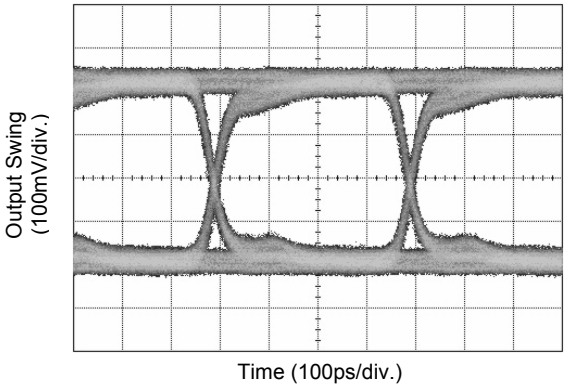
Typical Operating Characteristics (Continued)

V_{CC} = 3.3V ±10%; V_{IN} > 400mV; T_A = 25°C, R_L = 100Ω across output pair; unless otherwise stated.

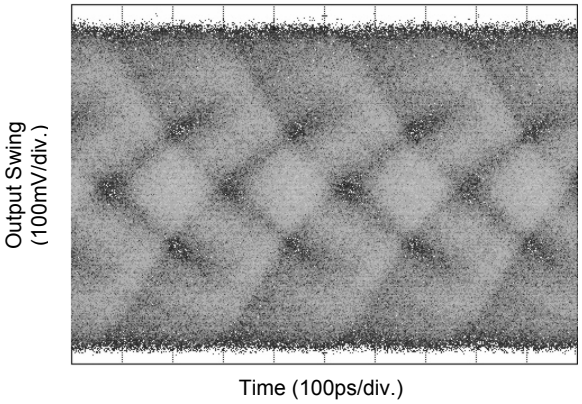
1m FR4 Output without SY58627L (2.5Gbps PRBS 2^{23})



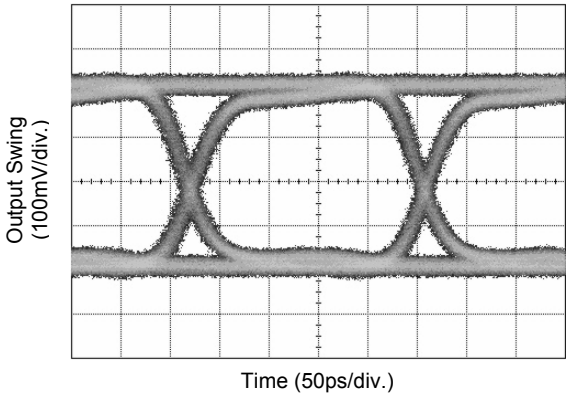
1m FR4 Output with SY58627L (2.5Gbps PRBS 2^{23})



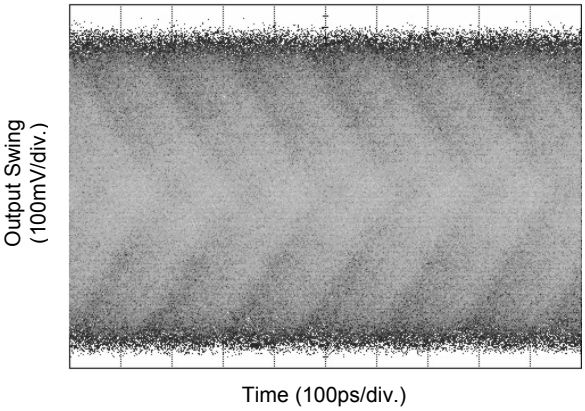
1m FR4 Output without SY58627L (4.25Gbps PRBS 2^{23})



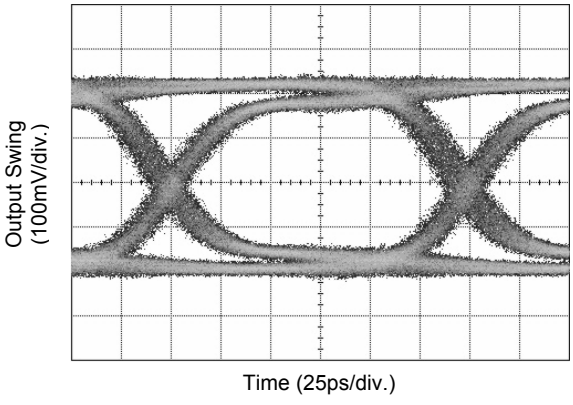
1m FR4 Output with SY58627L (4.25Gbps PRBS 2^{23})



1m FR4 Output without SY58627L (6.4Gbps PRBS 2^{23})



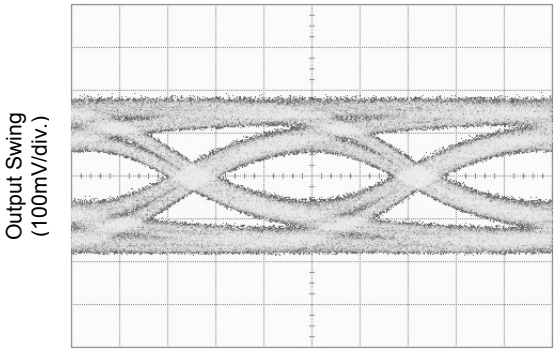
1m FR4 Output with SY58627L (6.4Gbps PRBS 2^{23})



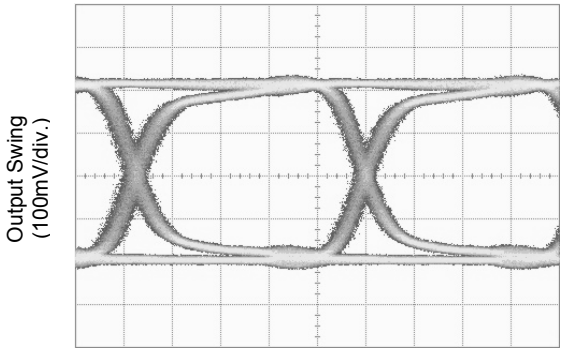
Typical Operating Characteristics (Continued)

V_{CC} = 3.3V ±10%; V_{IN} > 400mV; T_A = 25°C, R_L = 100Ω across output pair; unless otherwise stated.

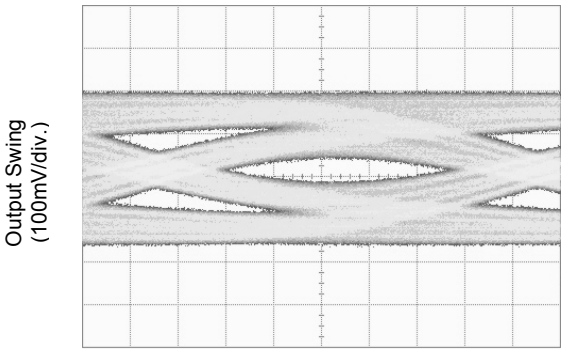
5m Cable(1) Output without SY58627L (4.25Gbps PRBS 2^{23})



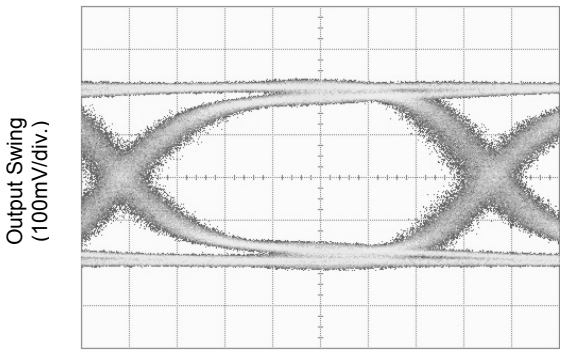
5m Cable(1) Output with SY58627L (4.25Gbps PRBS 2^{23})



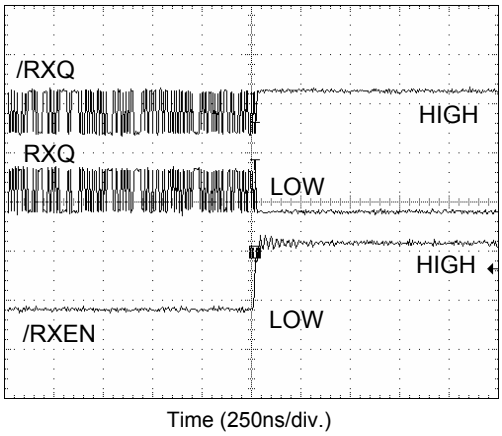
5m Cable(1) Output without SY58627L (6.4Gbps PRBS 2^{23})



5m Cable(1) Output with SY58627L (6.4Gbps PRBS 2^{23})



Output Disable



Note:

1. Measurements made with 26AWG Amphenol Skew Clear Eye Opener Plus cable.

Single-Ended and Differential Swings

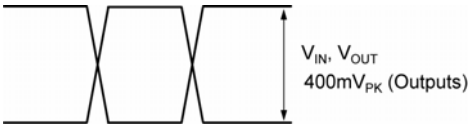


Figure 4a. Single-Ended Voltage Swing

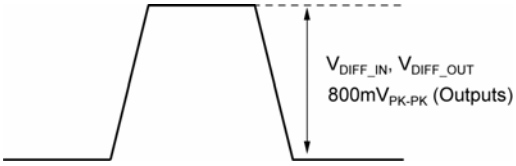


Figure 4b. Differential Voltage Swing

Input and Output Stages

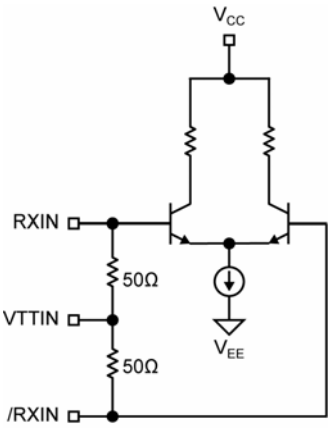


Figure 5a. Simplified RXIN Differential Input Stage

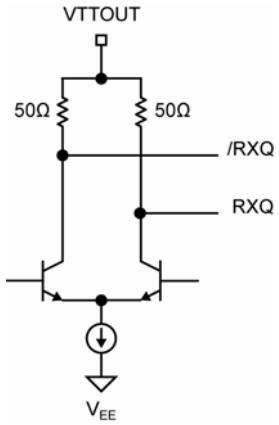


Figure 5b. Simplified RXQ Differential Output Stage

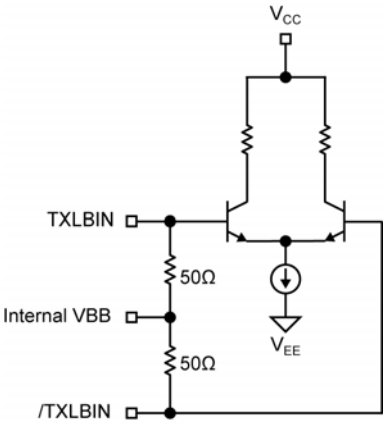


Figure 5c. Simplified TXLBIN Differential Input Stage

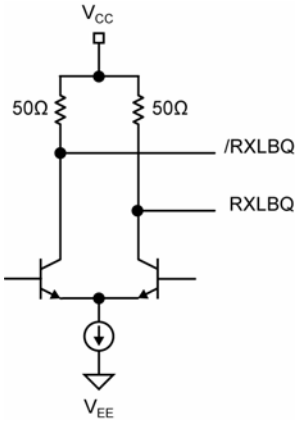


Figure 5d. Simplified RXLBQ Differential Output Stage

Input Interface Applications

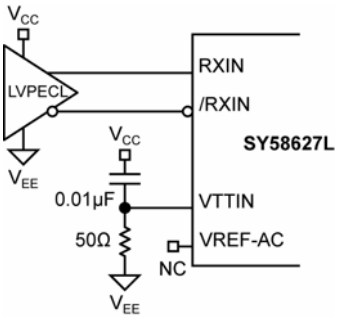


Figure 6a. LVPECL Interface (DC-Coupled)

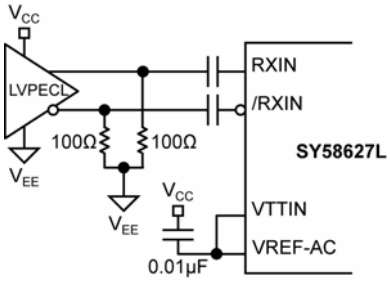
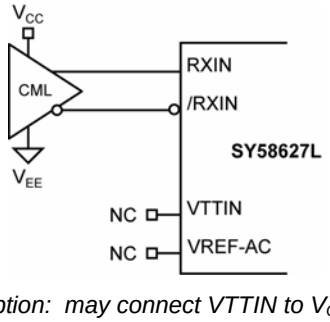


Figure 6b. LVPECL Interface (AC-Coupled)



option: may connect VTTIN to V_{CC}

Figure 6c. CML Interface (DC-Coupled)

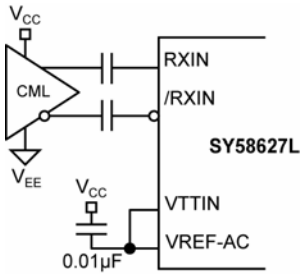


Figure 6d. CML Interface (AC-Coupled)

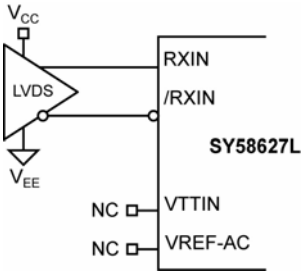


Figure 6e. LVDS Interface (DC-Coupled)

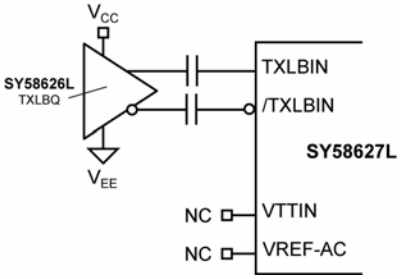


Figure 6f. TXLBIN Interface (AC-Coupled)

RXQ Output Interface Applications

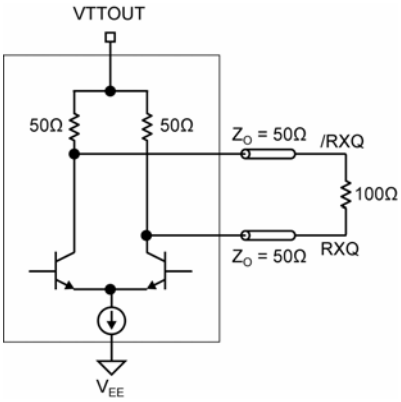


Figure 7a. CML DC-Coupled Termination

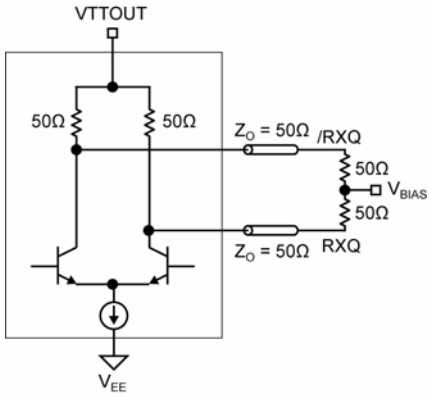


Figure 7b. CML DC-Coupled Termination

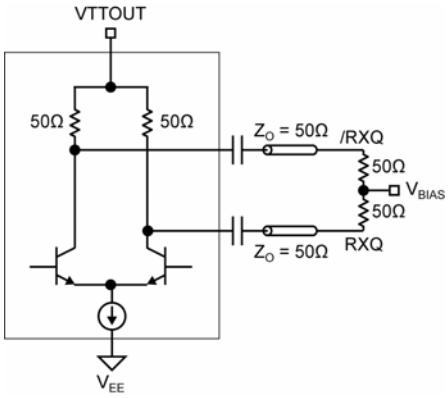


Figure 7c. CML AC-Coupled Termination

RXLBQ Output Interface Applications

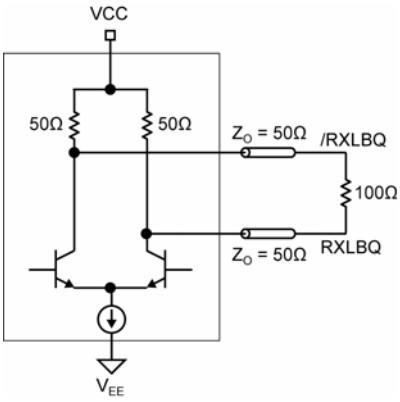


Figure 7d. CML DC-Coupled Termination

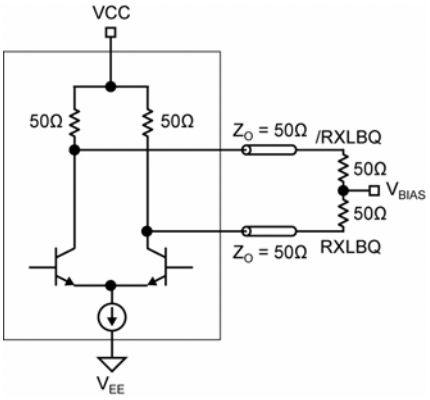


Figure 7e. CML DC-Coupled Termination

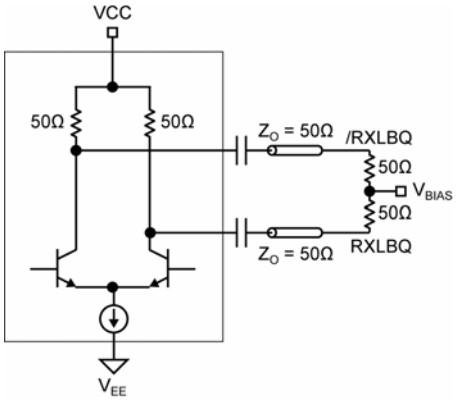
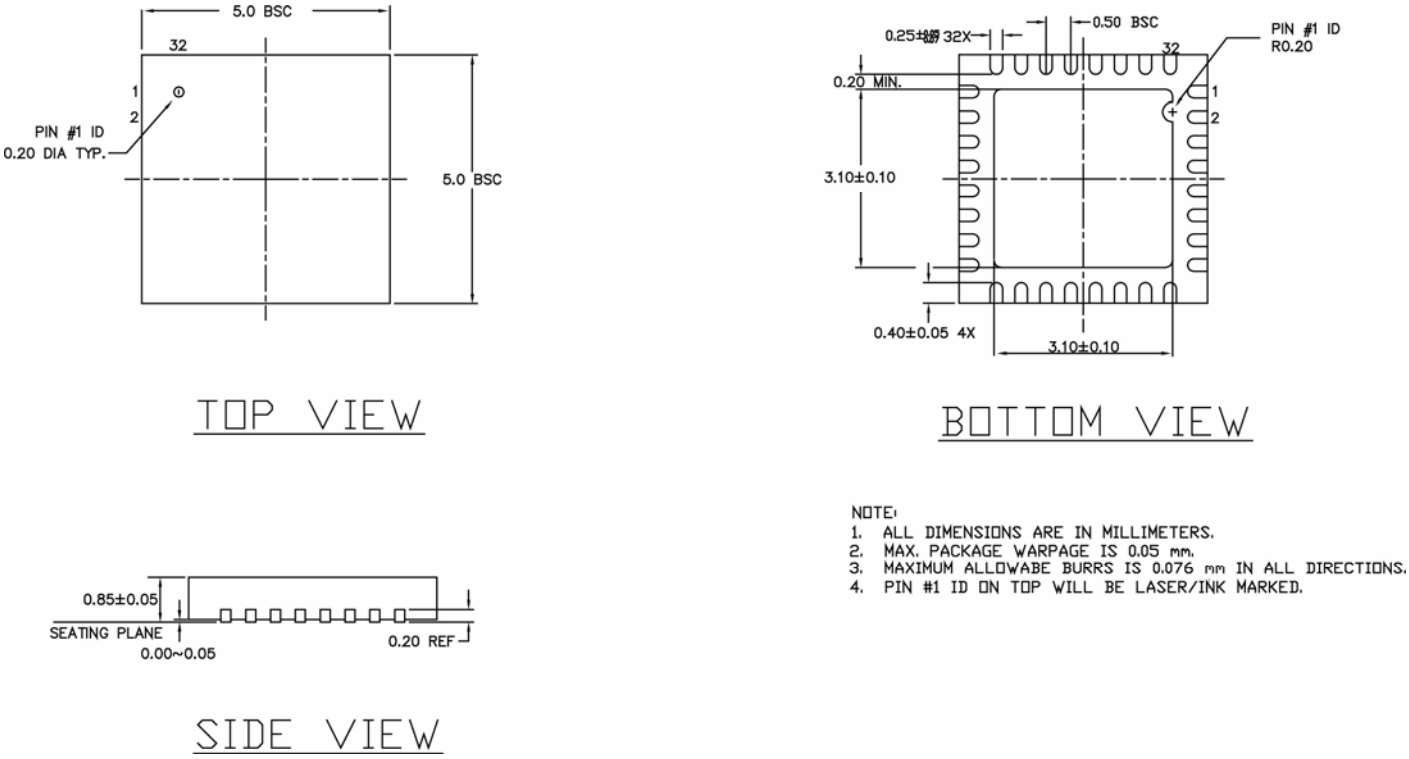


Figure 7f. CML AC-Coupled Termination

Related Product and Support Information

Part Number	Function	Data Sheet Link
SY58626L	DC-to-6.4Gbps Backplane Transmit Buffer with Selectable Output Pre-emphasis, I/O DC-Offset Control, and 200mV-3V_{PP} Output Swing	www.micrel.com/product-info/products/sy58626l.shtml
	MLF™ Application Note	www.amkor.com/products/notes_papers/MLFAppNote.pdf
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

Package Information



32-Pin MLF™ (MLF-32)

Package Notes:

1. Package meets Level 2 Moisture Sensitivity Classification.
2. All parts are dry-packed before shipment.
3. Exposed pad must be soldered to a ground for proper thermal management.

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