SY6321C

1A, High Accuracy, LDO Voltage Regulator

General Description

The SY6321C is a low-dropout (LDO) regulator capable of sourcing 1 A with only 200mV of dropout.

The SY6321C output is adjustable from 0.8V to 5.2V with external resistors. The SY6321C wide input-voltage range supports operation as low as 1.65V and up to 6.5V.

With 2% output voltage accuracy (over line, load, and temperature) and soft-start capabilities to reduce inrush current, the SY6321C is ideal for powering sensitive analog low-voltage devices [such as voltage-controlled oscillators (VCOs), analog-to-digital converters (ADCs), digital-to-analog converters (DACs), high-end processors, and field programmable gate arrays (FPGAs)].

The SY6321C is available in a compact DFN 2.5×2.5-10 package.

Features

- 2.0% Accuracy Over Line, Load, and Temperature
- Low Dropout: 200 mV (Max) at 1 A
- Wide Input Voltage Range: 1.65V to 6.5 V
- Wide Output Voltage Range: 0.8 V to 5.2V
- Fast Transient Response
- Adjustable Start-Up Inrush Control with Selectable Soft-Start Charge Current
- Open-Drain Power Good (PG) Output
- RoHS Compliant and Halogen Free
- Compact Package: DFN 2.5×2.5-10

Applications

- High-Speed Analog Circuits: VCO, LVDS
- Imaging: CMOS Sensors, Video ASICs
- Test and Measurement
- Instrumentation, Medical, and Audio
- Digital Loads: SerDes, FPGA, DSP

Typical Application

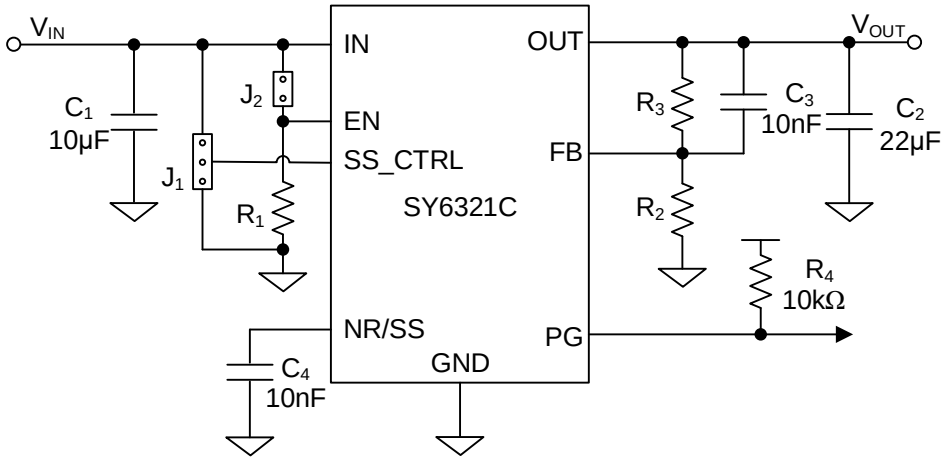


Figure1. Schematic Diagram

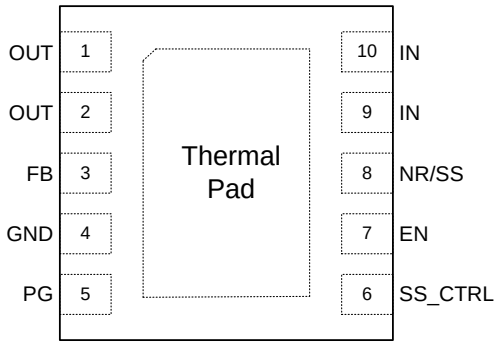
Ordering Information

Ordering Part Number	Package Type	Top Mark
SY6321CSED	DFN2.5×2.5-10 RoHS Compliant and Halogen Free	**m5*xyz***

Device code:m5

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Name	NO.	I/O	Pin Description
OUT	1, 2	O	Regulated output. A 22μF or greater capacitor must be connected from this pin to GND for stability.
FB	3	I	Feedback pin. This pin is the input to the control loop error amplifier and is used for setting the output voltage of the device.
GND	4	—	Device GND. Connected to the device thermal pad.
PG	5	O	Open-drain power-good indicator pin for the LDO output voltage. A 10kΩ to 100kΩ external pull-up resistor is required. This pin can be left floating or connected to GND if not used.
SS_CTRL	6	I	Soft-start control pin. Connect this pin either to GND or IN to change the NR/SS capacitor charging current. If a $C_{NR/SS}$ capacitor is not used, SS_CTRL must be connected to GND to avoid output overshoot.
EN	7	I	Enable pin. This pin turns the LDO on and off. If $V_{EN} \geq V_{EN\ (HI)}$, the regulator is enabled. If $V_{EN} \leq V_{EN\ (LO)}$, the regulator is disabled. The EN pin must be connected to IN if the enable function is not used.
NR/SS	8	—	Noise reduction pin. Connect this pin to an external capacitor to bypass the noise generated by the internal band gap reference. The capacitor reduces the output noise to very low levels and sets the output ramp rate to limit inrush current.
IN	9, 10	I	Input pin. A 10μF or greater input capacitor is required.
Thermal Pad		—	Connect the thermal pad to PCB ground plane.

Block Diagram

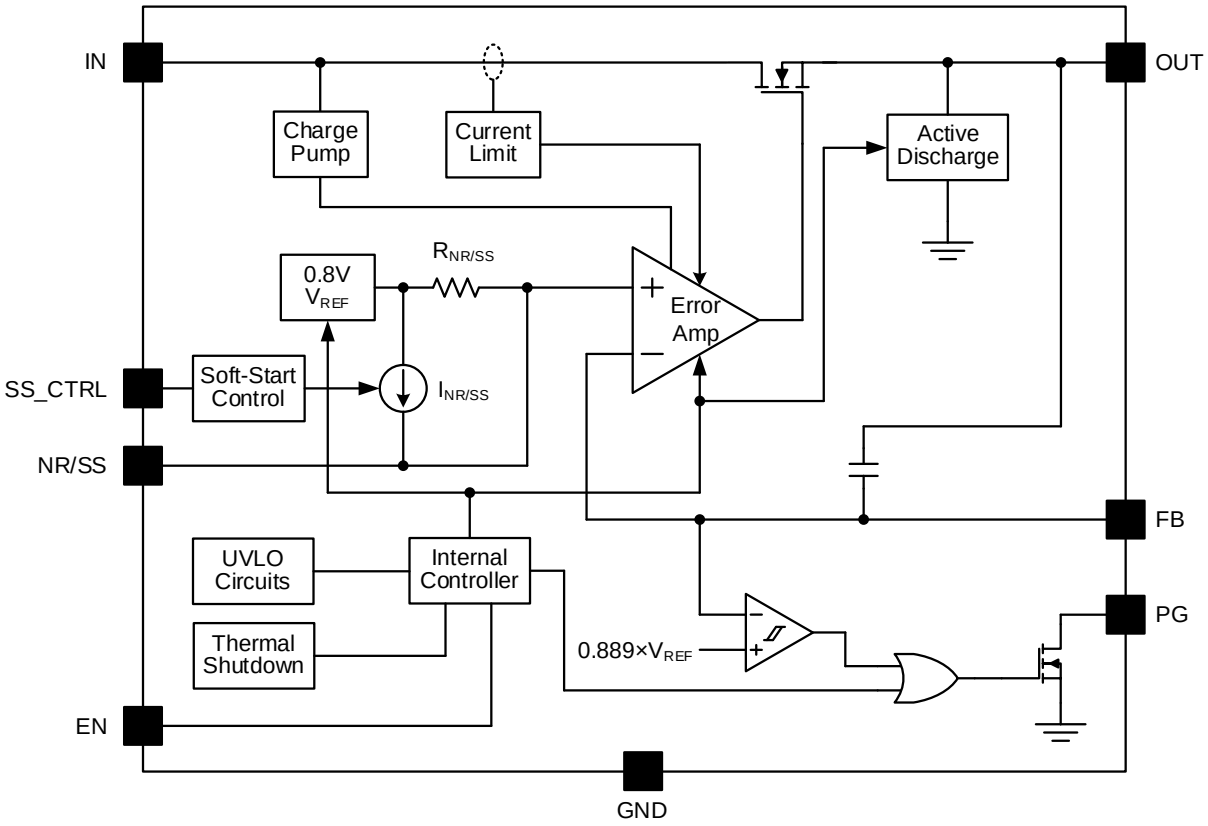


Figure2. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN, PG	-0.3	7	V
OUT, SS_CTRL, NR/SS, EN, FB	-0.3	IN+0.3	
Lead Temperature (Soldering, 10s)		260	°C
Junction Temperature, Operating	-40	150	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	61	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	15	
PD Power Dissipation TA = 25°C	1.64	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	1.65	6.5	V
OUT	0.8-2%	5.2+2%	
Maximum Output Current		1	A
C_{IN}	10		μF
C_{OUT}	22		
$C_{NR/SS}$		1	
R_{PG}	10	100	kΩ
Junction Temperature, Operating	-40	125	°C

Electrical Characteristics

(V_{IN} = 1.65 V≤ V_{IN} ≤ 6.5 V, V_{OUT} = 0.8 V, I_{OUT} = 5 mA, V_{EN} = 1.8 V, C_{IN} = 10μF, C_{OUT} = 22 μF, $C_{NR/SS}$ = 10 nF, C_{FF} = 0 nF, SS_CTRL=GND, R_{PG} =20 kΩ, T_J = -40°C ~125°C, typical value are at T_J=25°C, unless otherwise specified. (Note4))

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Voltage Range	V_{IN}			1.65		6.5	V
Reference Voltage	V_{REF}				0.8		V
Input Supply UVLO	V_{UVLO}	V_{IN} rising			1.35	1.65	V
UVLO Hysteresis	V_{HYS}				100		mV
Output Voltage Range	V_{OUT}			0.8–2.0%		5.2+2.0%	V
Output Voltage Accuracy		1.8 V ≤ V_{IN} ≤ 6.5 V, 5 mA ≤ I_{OUT} ≤ 1 A	T_J=25°C	–1.0%		1.0%	
			T_J= -40°C ~125°C	-2.0%		2.0%	
Line Regulation	ΔV_{OUT}	I_{OUT} = 5mA, 1.8 V ≤ V_{IN} ≤ 6.5 V			0.11		%/V
Load Regulation	ΔV_{OUT}	V_{IN} = 3.3V,5 mA ≤ I_{OUT} ≤ 1 A			0.45		%/A
Dropout Voltage	V_{DO}	V_{IN} ≥ 1.8 V, I_O =1A, V_{FB} = 0.8 V – 3%				200	mV
Output Current Limit	I_{LIMIT}	V_{OUT} forced at 0.9 × $V_{OUT(TARGET)}$, V_{IN} =3.3V		1	1.7	2.4	A
GND Pin Current	I_{GND}	V_{IN} = 6.5 V, I_{OUT} = 5 mA			1	2.5	mA
		V_{IN} = 1.8 V, I_{OUT} = 1 A				3	
Shutdown GND Pin Current	I_{SDN}	PGx = (open), V_{IN} = 6.5 V, V_{EN} = 0V, T_J = 25°C			0.1	15	μA
		PGx = (open), V_{IN} = 6.5 V, V_{EN} = 0V, T_J = 125°C				50	μA
FB Pin Leakage Current	I_{FB}	V_{IN} = 6.5 V, V_{FB} = 0.8 V		-100		100	nA
EN High Level	$V_{EN(HI)}$	V_{IN} = 3.3V		1.2		6.5	V
EN Low Level	$V_{EN(LO)}$	V_{IN} = 3.3V		0		0.4	V
Enable Pin Current	I_{EN}	V_{IN} = 6.5 V, 0 V ≤ V_{EN} ≤ 6.5 V		-0.2		0.2	μA
SS_CTRL Pin Current	I_{SS_CTRL}	V_{IN} = 6.5 V, 0 V ≤ V_{SS_CTRL} ≤ 6.5 V		-0.2		0.2	μA
PG Pin Threshold	$V_{IT(PG)}$	For PG transitioning low with falling V_{OUT}, expressed as a percentage of $V_{OUT(TARGET)}$		84%	89.3%	94.5%	
PG Pin Hysteresis	$V_{HYS(PG)}$	For PG transitioning high with rising V_{OUT}, expressed as a percentage of $V_{OUT(TARGET)}$			1%		
PG Pin Low-Level Output Voltage	$V_{OL(PG)}$	V_{OUT} < $V_{IT(PG)}$, I_{PG} = –1 mA (current into device)				0.4	V
PG Pin Leakage Current	$I_{lkg(PG)}$	V_{OUT} > $V_{IT(PG)}$, V_{PG} = 6.5 V				1	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
NR/SS Pin Charging Current	$I_{NR/SS}$	$V_{NR/SS}$ = GND, V_{IN} = 3.3 V, V_{SS_CTRL} = GND	4.5	8.5	13	μA
		$V_{NR/SS}$ = GND, V_{IN} = 3.3 V, V_{SS_CTRL} = V_{IN}	85	135	200	
Power Supply Ripple Rejection (Note 5)	PSRR	f = 500 kHz, V_{IN} = 3.8 V, V_{OUT} = 3.3 V, I_{OUT} = 750mA, $C_{NR/SS}$ = 10 nF, C_{FF} = 10 nF		40		dB
Output Active Discharge Resistance	R_{DIS}	V_{IN}=3.3V, V_{EN}=GND, V_{OUT}=0.1V	100	150	250	Ω
Thermal Shutdown Threshold (Note 5)	T_{SD}	Shutdown, temperature increasing		160		ºC
Thermal Shutdown Hysteresis (Note 5)		Reset, temperature decreasing		140		ºC

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is simulated in the natural convection at T_A=25°C on a Silergy evaluation board following JEDEC51-2 thermal measurement standard. Exposed Pad of DFN2.5×2.5-10 package is the case position for θ_{JC} measurement.

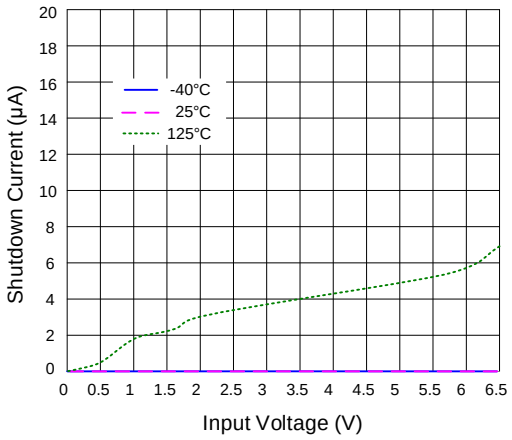
Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$ = 25°C. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

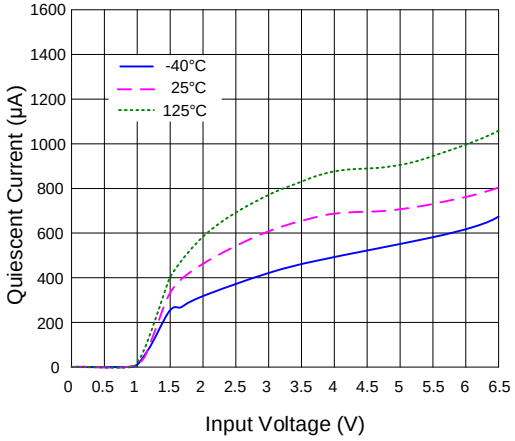
Note 5: Guaranteed by design.

Typical Performance Characteristics

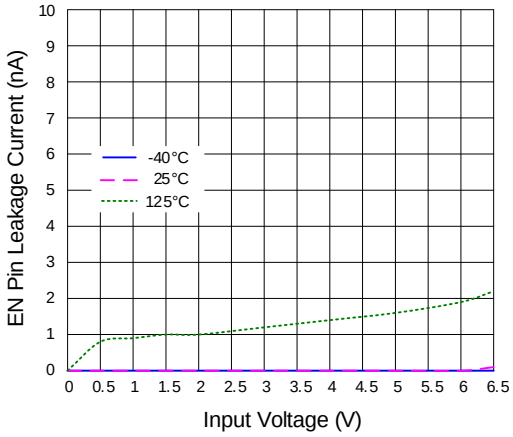
Shutdown Current vs. Input Voltage



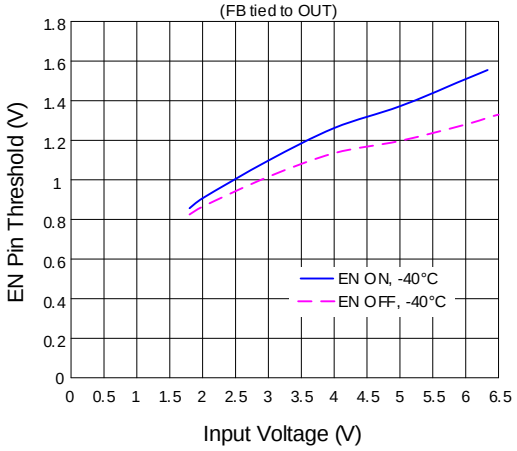
Quiescent Current vs. Input Voltage



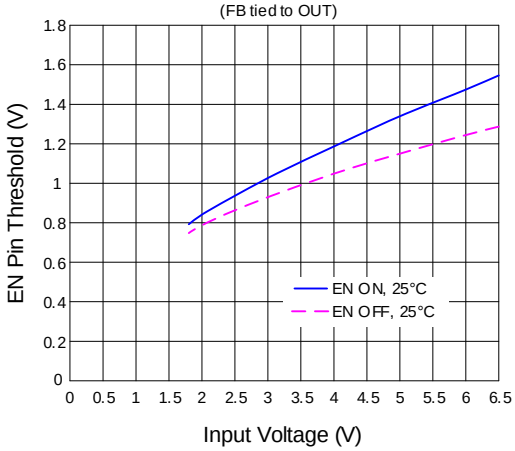
EN Pin Leakage Current vs. Input Voltage



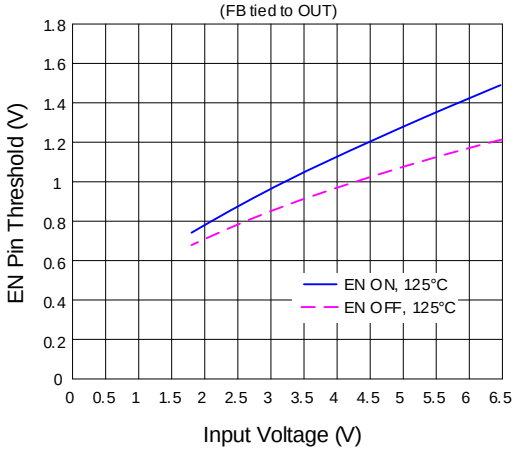
EN Pin Threshold vs. Input Voltage
(FB tied to OUT)



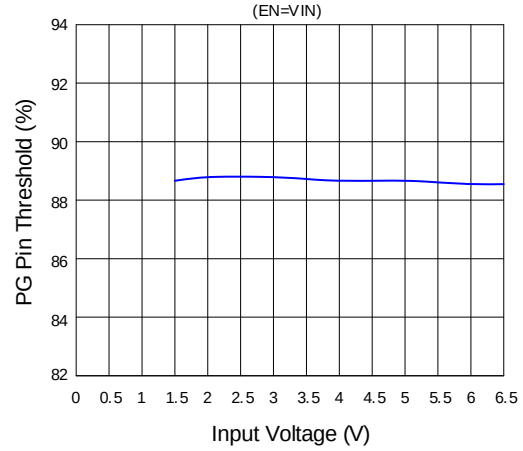
EN Pin Threshold vs. Input Voltage
(FB tied to OUT)



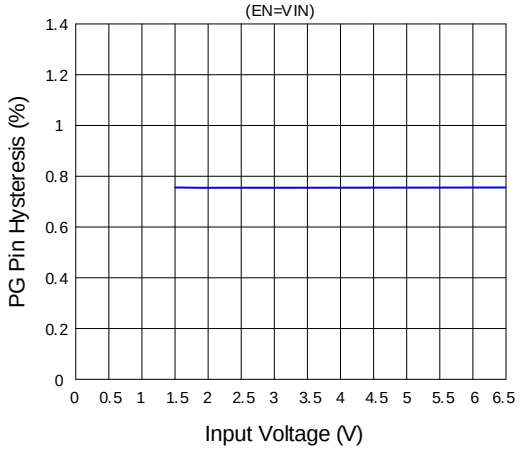
EN Pin Threshold vs. Input Voltage
(FB tied to OUT)



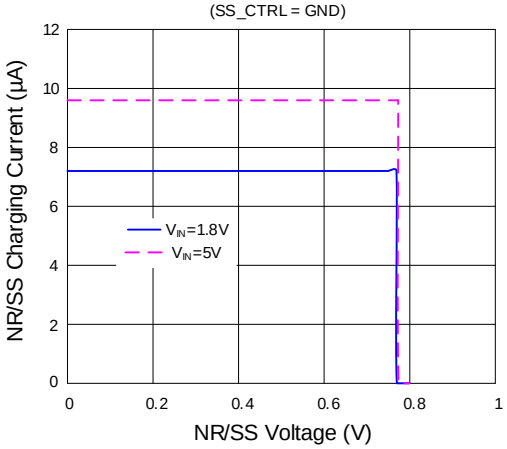
PG Pin Threshold vs. Input Voltage
(EN=VIN)



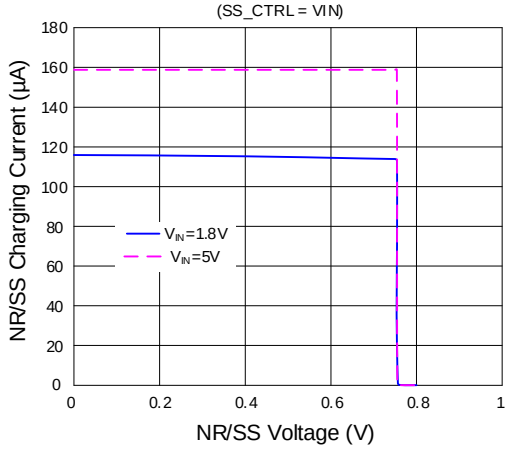
PG Pin Hysteresis vs. Input Voltage
(EN=VIN)



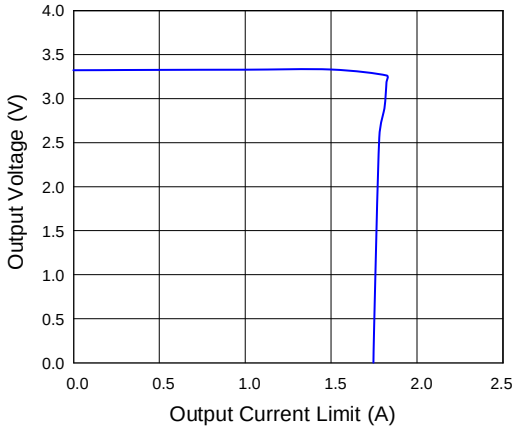
NR/SS Charging Current vs. NR/SS Voltage
(SS_CTRL = GND)



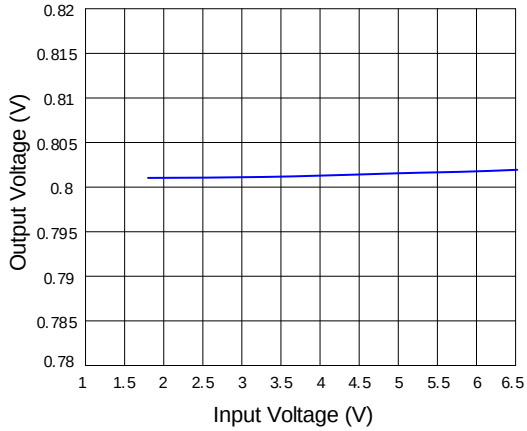
NR/SS Charging Current vs. NR/SS Voltage
(SS_CTRL = VIN)



Output Voltage vs. Output Current Limit
(V_{IN}=5V, EN=5V, V_{OUT}=3.3V)

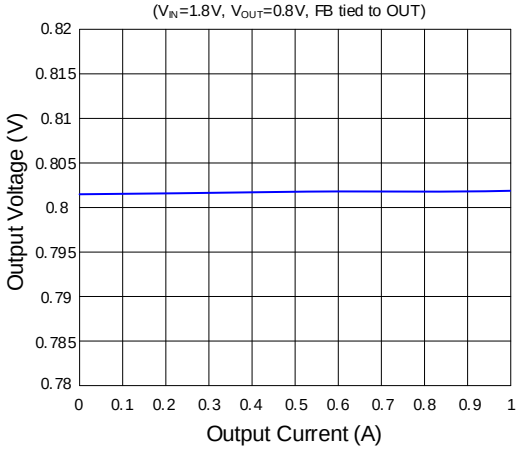


Line Regulation
(I_{OUT}=5mA)



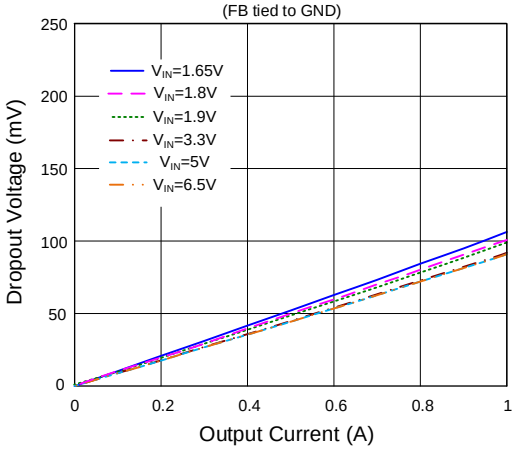
Load Regulation

(V_{IN}=1.8V, V_{OUT}=0.8V, FB tied to OUT)



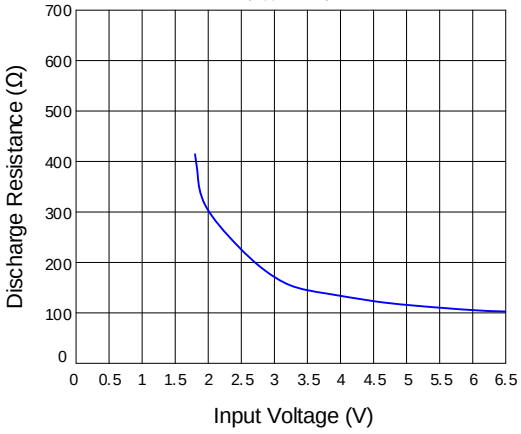
Dropout Voltage vs. Output Current

(FB tied to GND)



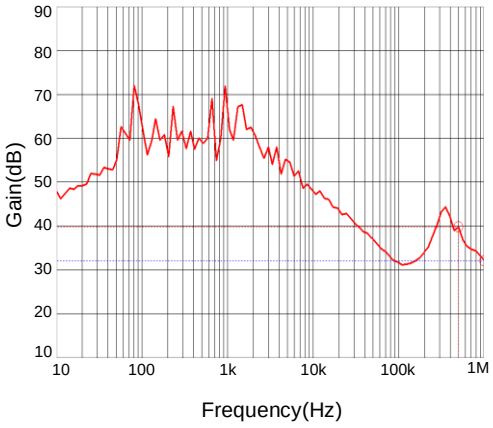
Discharge Resistance vs. Input Voltage

(V_{OUT}=0.1V)



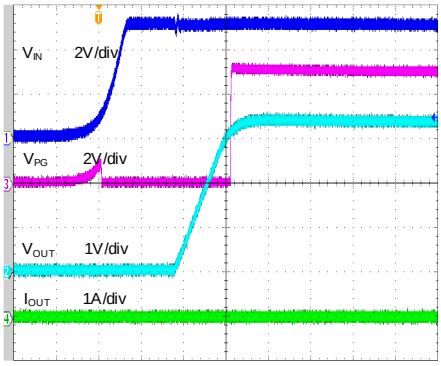
PSRR

(V_{IN}=3.8V, V_{OUT}=3.3V, I_{OUT}=750mA, $C_{NR/SS}$=10nF, C_{FF}=10nF)



Startup from V_{IN}

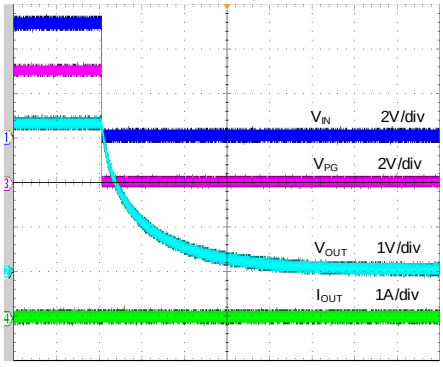
(V_{IN}=5V, V_{OUT}=3.3V, SS_CTRL=V_{IN}, C_{IN}=10µF, C_{OUT}=22µF, Null Load)



Time (40µs/div)

Shutdown from V_{IN}

(V_{IN}=5V, V_{OUT}=3.3V, SS_CTRL=V_{IN}, C_{IN}=10µF, C_{OUT}=22µF, Null Load)



Time (1s/div)

Startup from V_{IN}

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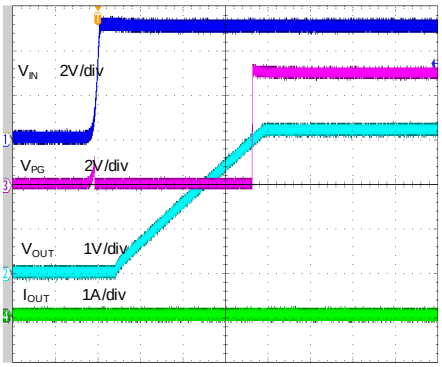
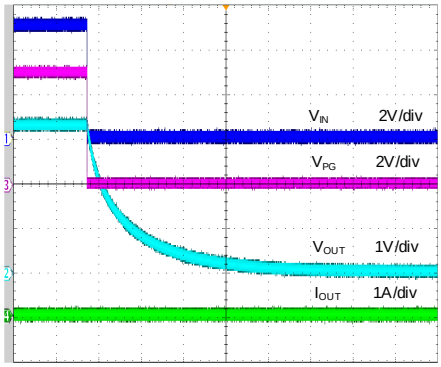


Time (200µs/div)

Shutdown from V_{IN}

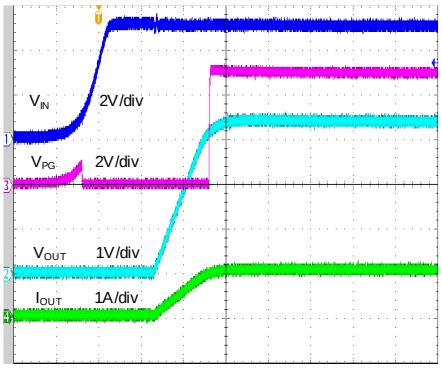
(V_{IN}=5V, V_{OUT}=3.3V, SS_CTRL=GND, C_{IN}=10µF, C_{OUT}=22µF, Null Load)



Time (1s/div)

Startup from V_{IN}

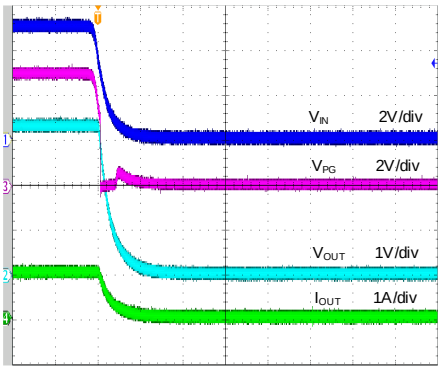
(V_{IN}=5V, V_{OUT}=3.3V, SS_CTRL=V_{IN}, C_{IN}=10µF, C_{OUT}=22µF, I_{OUT}=1A)



Time (40µs/div)

Shutdown from V_{IN}

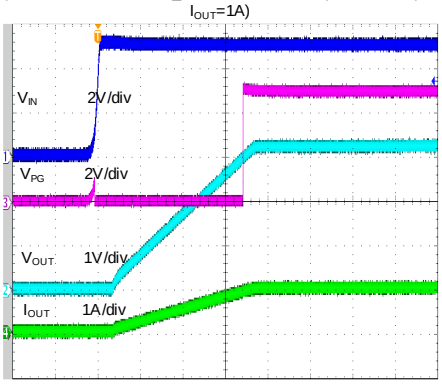
(V_{IN}=5V, V_{OUT}=3.3V, SS_CTRL=V_{IN}, C_{IN}=10µF, C_{OUT}=22µF, I_{OUT}=1A)



Time (200µs/div)

Startup from V_{IN}

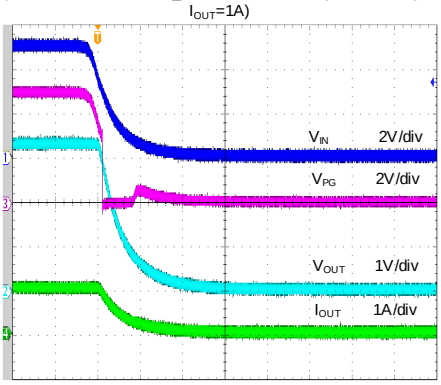
(V_{IN}=5V, V_{OUT}=3.3V, SS_CTRL=GND, C_{IN}=10µF, C_{OUT}=22µF, I_{OUT}=1A)



Time (200µs/div)

Shutdown from V_{IN}

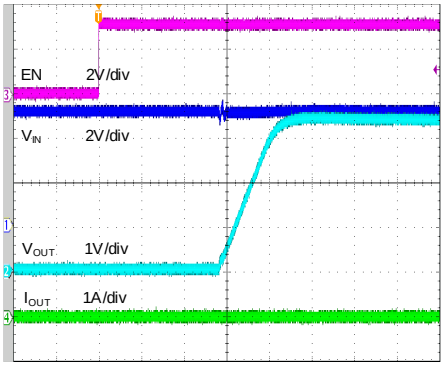
(V_{IN}=5V, V_{OUT}=3.3V, SS_CTRL=GND, C_{IN}=10µF, C_{OUT}=22µF, I_{OUT}=1A)



Time (100µs/div)

Startup from EN

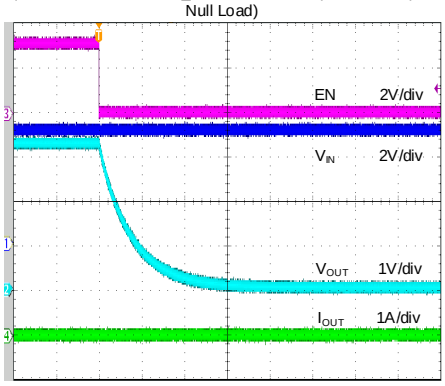
(V_{IN}=5V, V_{OUT}=3.3V, SS_CTRL=V_{IN}, C_{IN}=10µF, C_{OUT}=22µF, Null Load)



Time (40µs/div)

Shutdown from EN

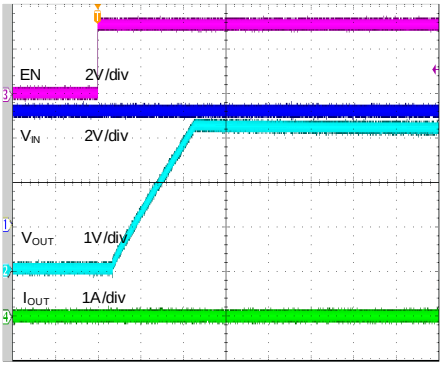
(V_{IN}=5V, V_{OUT}=3.3V, SS_CTRL=V_{IN}, C_{IN}=10µF, C_{OUT}=22µF, Null Load)



Time (4ms/div)

Startup from EN

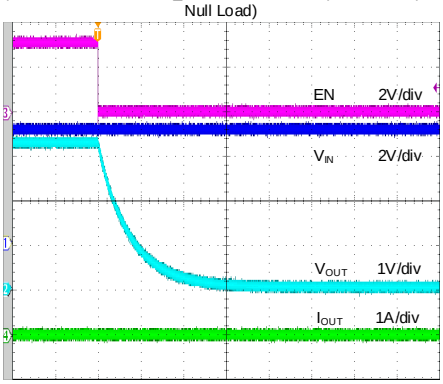
(V_{IN}=5V, V_{OUT}=3.3V, SS_CTRL=GND, C_{IN}=10µF, C_{OUT}=22µF, Null Load)



Time (400µs/div)

Shutdown from EN

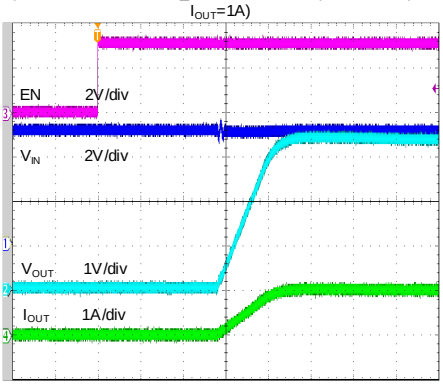
(V_{IN}=5V, V_{OUT}=3.3V, SS_CTRL=GND, C_{IN}=10µF, C_{OUT}=22µF, Null Load)



Time (4ms/div)

Startup from EN

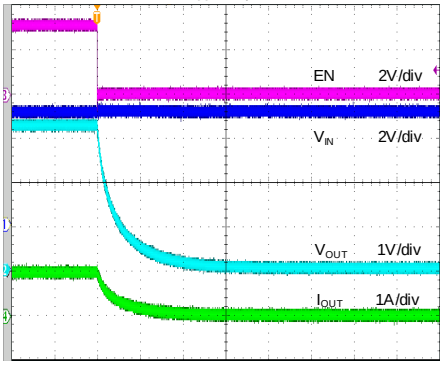
(V_{IN}=5V, V_{OUT}=3.3V, SS_CTRL=V_{IN}, C_{IN}=10µF, C_{OUT}=22µF, I_{OUT}=1A)



Time (40µs/div)

Shutdown from EN

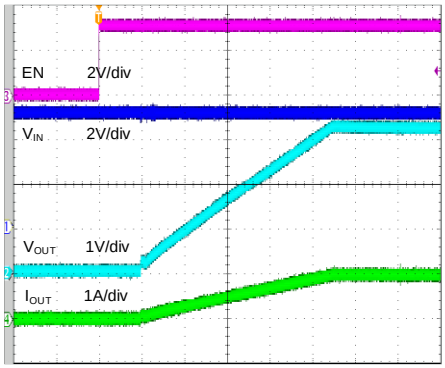
(V_{IN}=5V, V_{OUT}=3.3V, SS_CTRL=V_{IN}, C_{IN}=10µF, C_{OUT}=22µF, I_{OUT}=1A)



Time (100µs/div)

Startup from EN

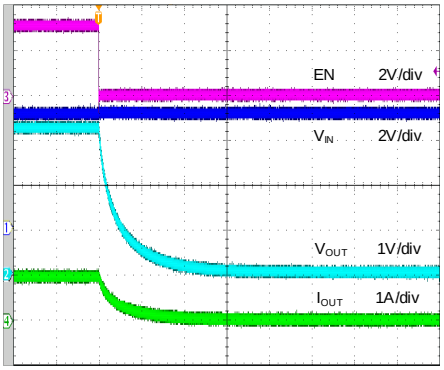
(V_{IN}=5V, V_{OUT}=3.3V, SS_CTRL=GND, C_{IN}=10μF, C_{OUT}=22μF, I_{OUT}=1A)



Time (200μs/div)

Shutdown from EN

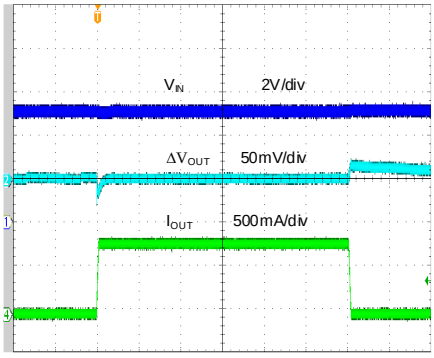
(V_{IN}=5V, V_{OUT}=3.3V, SS_CTRL=GND, C_{IN}=10μF, C_{OUT}=22μF, I_{OUT}=1A)



Time (100μs/div)

Load Transient

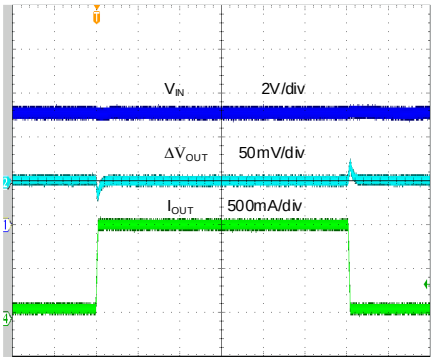
(V_{IN}=5V, V_{OUT}=3.3V, C_{OUT}=22μF, I_O=Null→750mA →Null)



Time (200μs/div)

Load Transient

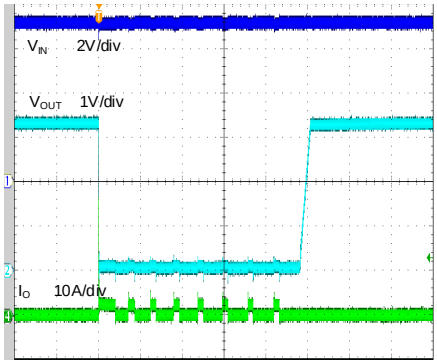
(V_{IN}=5V, V_{OUT}=3.3V, C_{OUT}=22μF, I_O=0.1A→1A →0.1A)



Time (200μs/div)

Short Protect

(V_{IN}=7V, V_{OUT}=3.3V)



Time (2ms/div)

Operation

The SY6321C is a high-performance positive voltage regulator designed for applications requiring very low input voltage and very low dropout voltage at up to 1A output. It operates with a V_{IN} as low as 1.65V, and the output voltage is programmable as low as 0.8V.

The SY6321C features ultra-low dropout, ideal for applications where V_{OUT} is very close to V_{IN}. Additionally, it has an enable pin to further reduce power dissipation when shutdown. The device provides excellent regulation over line, load, and temperature variations.

Applications Information

Input Capacitor C_{IN}

To minimize the potential noise problem and improve power-supply rejection ratio (PSRR) and transient response, place a typical X5R or better grade ceramic capacitor close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and the IN/GND pins. In this case, a 10μF low ESR ceramic capacitor is recommended.

Output Capacitor C_{OUT}

For stable operation over the full temperature range, a 22μF low-ESR ceramic capacitor is recommended. Use 22μF to reduce noise, improve load-transient response and PSRR.

Feedback Resistor Dividers R_3 and R_2

Choose R_3 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, choose large resistance values between 10kΩ and 1MΩ for both R_3 and R_2. If V_{OUT} is 3.3V, R_3=50KΩ is chosen, then using the following equation, R_2 can be calculated to be 16kΩ:

$$R_2 = \frac{0.8V}{V_{OUT} - 0.8V} R_3$$

Over Current Protection

The device features short-circuit protection. The current –limit circuit regulates the output current to its limit threshold to protect the IC from damage. In over current or short circuit conditions, the power loss of the IC is relatively high, this may trigger the thermal protection.

Power Good Function

The SY6321C provides an open-drain PG output that goes high when the output is within ±10% of REFOUT. PG is an open-drain output, and requires a pull-up resistor between 10kΩ and 100 kΩ, placed between PGOOD and a stable active supply voltage rail.

Soft Start Function

Soft-start refers to the ramp-up characteristic of the output voltage during the turn-on period of the LDO after the EN and UVLO thresholds are exceeded. The noise-reduction capacitor ($C_{NR/SS}$) serves a dual purpose of both controlling output noise reduction and programming the soft-start transitions during turn-on. Larger values of the noise-reduction capacitors decrease the noise but also result in a slower output turn-on ramp rate.

The SY6321C features an SS_CTRL pin. When the SS_CTRL pin is grounded, the charge current for the NR/SS pin is 8.5μA (typ); when this pin is connected to the IN, the charge current for the NR/SS pin is increased to 135 μA (typ). The higher current allows the use of a much larger noise-reduction capacitor and maintains a reasonable startup time.

t_{SS} is from 10%V_{OUT} to 90%V_{OUT} as Recommended Formula for Soft-start time Calculation:

$$t_{SS}=(0.8\times V_{REF}\times C_{NR/SS})/I_{NR/SS}$$

Enable Protection

The enable pin for the SY6321C is active high. The output voltage is enabled when the enable pin voltage is greater than $V_{EN(HI)}$ and disabled with the enable pin voltage is less than $V_{EN(LO)}$. If independent control of the output voltage is not needed, then connect the enable pin to the input.

Thermal Considerations

The SY6321C can deliver a current of up to 1A over the full operating temperature range. However, the maximum output current must be derated at higher ambient temperature. In all possible conditions, the junction temperature must be within the range specified under operating conditions. Power dissipation can be calculated based on the output current and the voltage drop across regulator.

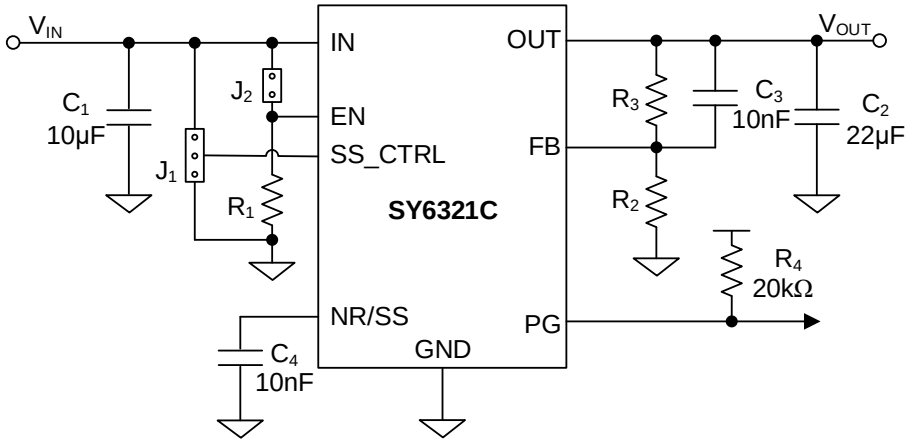
$$P_D=(V_{IN}-V_{OUT})\times I_{OUT}+V_{IN}\times I_{GND}$$

The final operating junction temperature for any set of condition can be estimated by the following thermal equation:

$$P_{D(MAX)}=(T_{J(MAX)}-T_A)/\theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum junction temperature of die (125°C) and T_A is the maximum ambient temperature. The junction to ambient thermal resistance (θ_{JA}) footprint is 61°C/W for DFN package.

Schematic



BOM List

Reference Designator	Description	Part Number	Manufacturer
C_1	10μF/10V, ±10%, X5R, 0805	GRM21BR71A106K	Muruta
C_2	22μF/10V, ±10%, X5R, 1206	GRM31CR61A226M	Muruta
C_3	10nF/50V, ±10%, X7R, 0603	GCE188R71H103K	Muruta
C_4	10nF/50V, ±10%, X7R, 0603	GCE188R71H103K	Muruta
R_1	10kΩ, 1%, 0.1W, 0603	RC0603FR-0710KL	YAGEO
R_2	16kΩ, 1%, 0.1W, 0603	RC0603FR-0716KL	YAGEO
R_3	49.9kΩ, 1%, 0.1W, 0603	RC0603FR-0749K9L	YAGEO
R_4	20kΩ, 1%, 0.1W, 0603	RC0603FR-0720KL	YAGEO
J_1	Header, 2.54 mm, 3x1, Gold, SMT		Any
J_2	Header, 2.54 mm, 2x1, Gold, SMT		Any

PCB Layout Guide:

For the best performance of the SY6321C, the following guidelines must be strictly followed:

1) Keep all Power traces (VIN / OUT / GND) as short and wide as possible and use at least 2-ounce copper for all Power traces.

2) Place a ground plane under all circuitry to lower both resistance and inductance and improve DC and transient performance.

3) Input and output capacitors should be placed closed to the SY6321C and connected to ground plane to reduce noise coupling.

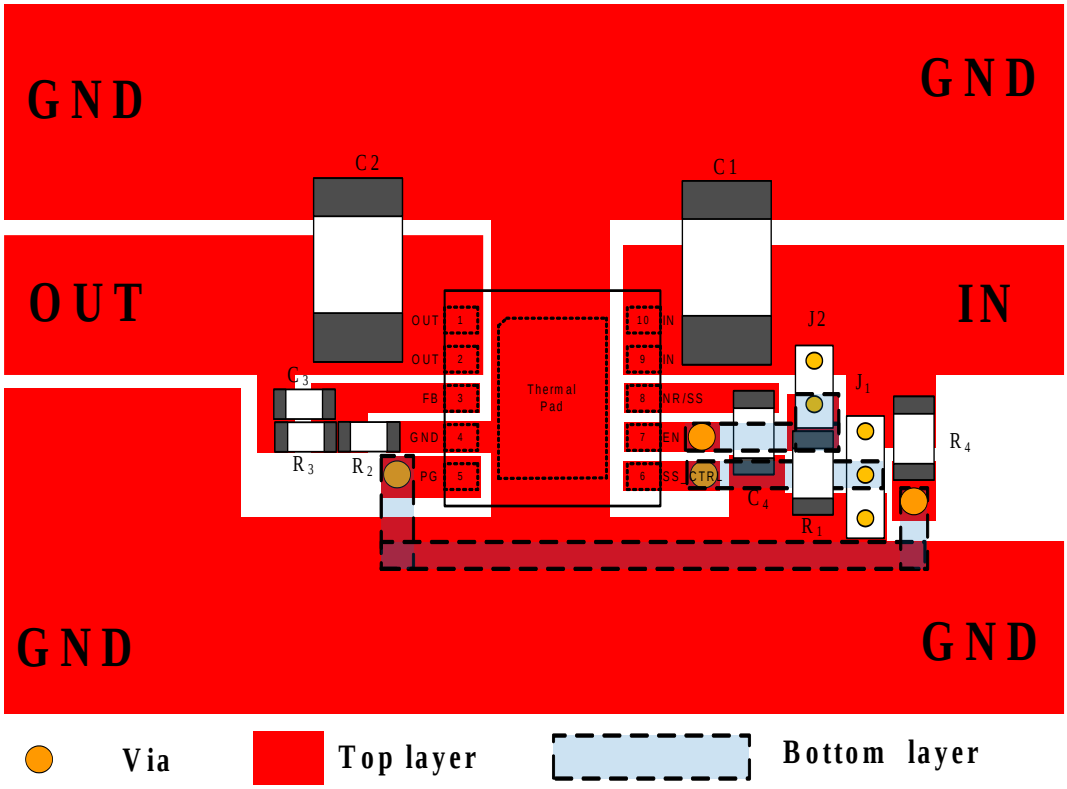
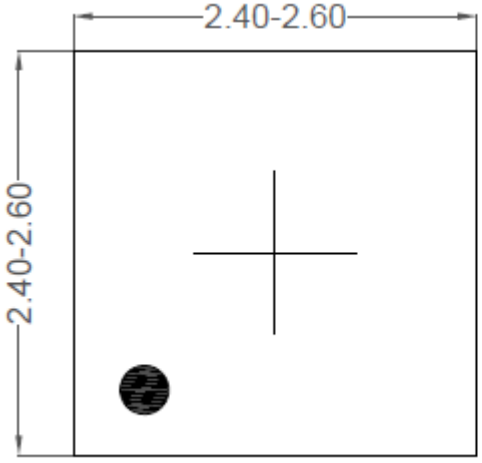
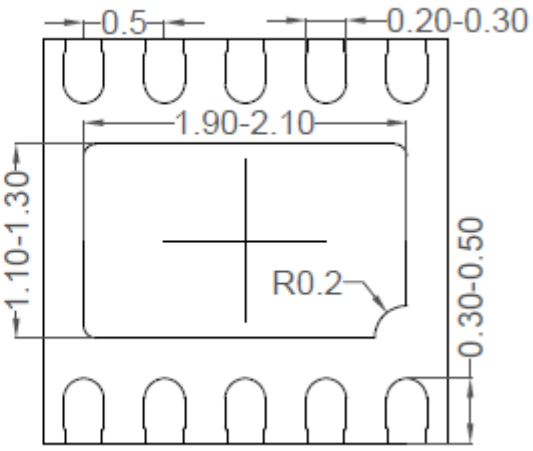


Figure3. PCB Layout Suggestion

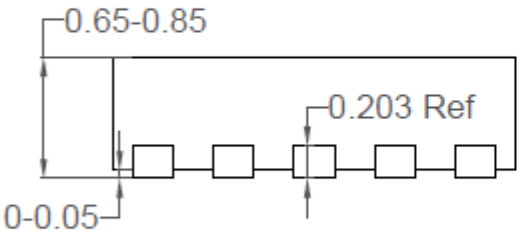
DFN2.5×2.5-10 Package Outline Drawing



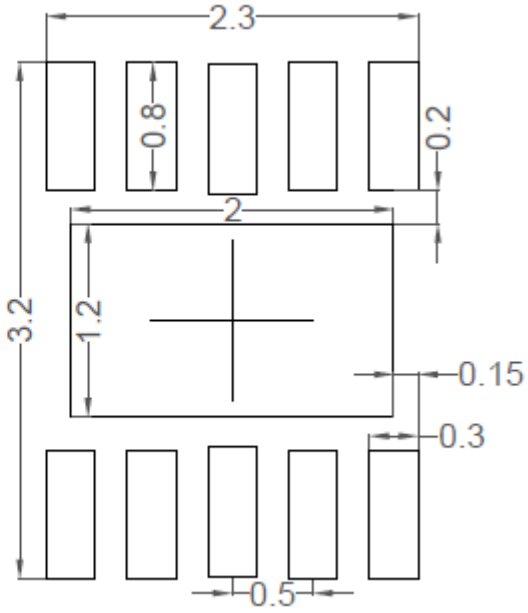
Top View



Bottom View



Front View

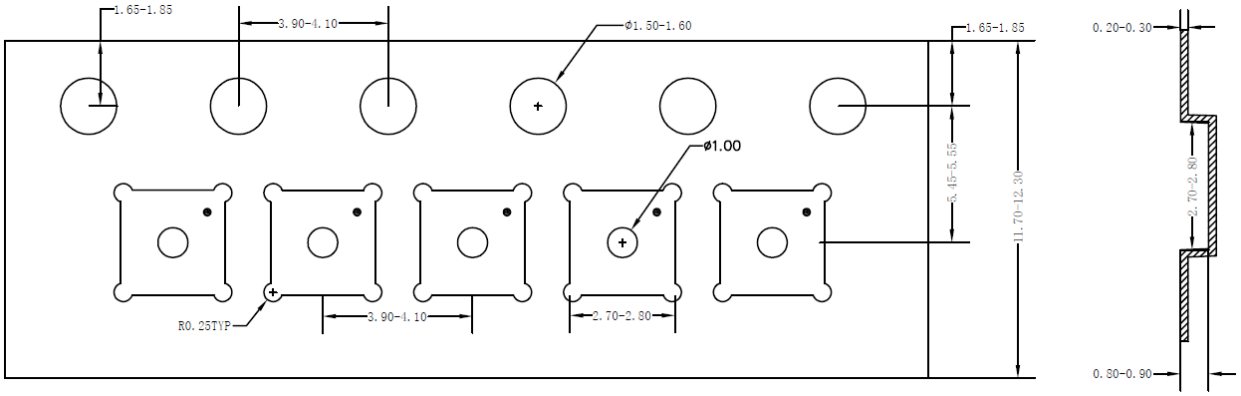


Recommended PCB Layout

Notes: 1, All dimension in millimeter and exclude mold flash & metal burr;
2, center line refers chip body center.

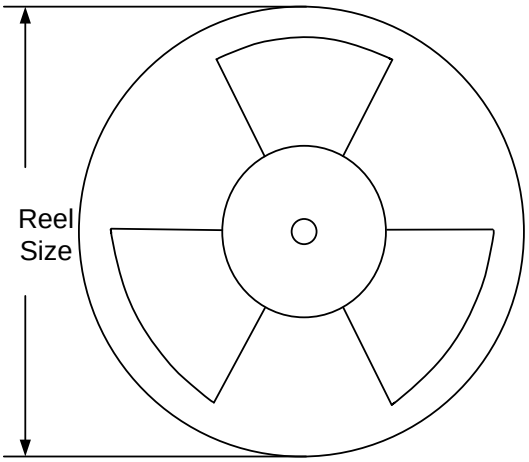
Tape and Reel Information

1. Tape dimensions and Pin1 orientation



Direction of Feed ⟶

2. Reel dimensions



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN2.5×2.5-10	12	4	7”	400	160	3000

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Jan.08, 2025	Revision 1.0	Initial Release

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