SY6340

150mA LDO Regulator

General Description

The SY6340 is a 150mA precise LDO. The device provides programmable output voltage with ±2% accuracy. The ultra low drop out voltage, wide input voltage range and low ground current make it suitable for USB and portable electronics applications with different inputs. Other features include the operation stability with low ESR ceramic capacitors due to the internal compensation, logic enable control, thermal shutdown, current limit, reverse leakage current protection.

The SY6340 is available in SOT23-5/DFN2×2-6 package.

Ordering Information

SY6340 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY6340AAC	SOT23-5	----
SY6340DEC	DFN2×2-6	

Features

- Wide Input Voltage Range: 2.3V to 30V
- Low Dropout Voltage(300mV @ 150mA)
- Low Ground Current
- Ultra-Low Shutdown Current
- High Output Accuracy of ±2% Over Operating Temperature Range
- Stable with Small Ceramic Capacitors
- Excellent Load And Line Regulation
- 150mA Output Current Capability
- Output Current Limitation
- Reverse Leakage Current Protection
- Reverse Input Voltage Protection
- TTL Logic Enable Input
- Thermal Shutdown
- RoHS Compliant and Halogen Free
- Compact SOT23-5/ DFN2×2-6 Package

Applications

- Battery Powered Applications
- Consumer And Portable Products
- Notebook
- Smart Phones
- SMPS Post-regulator/ DC-DC Modules

Typical Applications

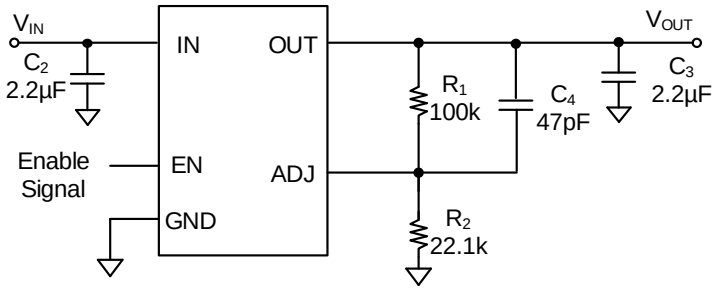


Figure 1. Schematic Diagram

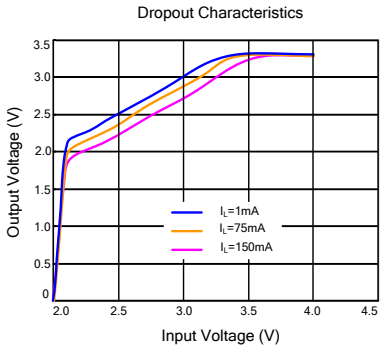
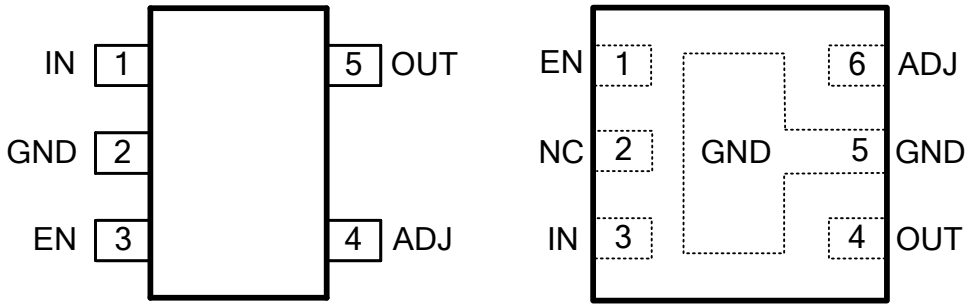


Figure 2. Dropout Characteristics

Pinout (top view)



(SOT23-5) (DFN2×2-6)

Top mark: **JN*xyz*** for SY6340AAC(Device code: JN, ***x=year code, y=week code, z= lot number code***)
Top mark: **PE*xyz*** for SY6340DEC(Device code: PE, ***x=year code, y=week code, z= lot number code***)

Pin Name	SOT23-5	DFN2×2-6	Pin Description
IN	1	3	Supply input pin.
GND	2	5	Ground pin.
OUT	5	4	LDO output pin.
EN	3	1	Enable pin. Pull it low to shutdown or pull it high to enable, do not leave open.
ADJ	4	6	Output voltage adjust pin. Feedback the output voltage through resistor voltage divider network. $V_O = 0.6 \times (1 + \frac{R1}{R2})$

Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- -20V to 36V
Output Voltage ---------- 0.3V+VIN
EN Voltage ---------- -0.3V to 0.3V+VIN
ADJ Voltage ---------- 0V to 3.6V
Power Dissipation, P_D @ T_A = 25°C SOT23-5/ DFN2×2-6 ----------1/1.6W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 100/62°C/W
θ_{JC} ---------- 25/8.5°C/W
Junction Temperature Range ---------- 125°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 2.3V to 30V
Output Voltage ---------- 0.3V+V_{IN}
EN Voltage ---------- 0V to 0.3V+V_{IN}
Junction Temperature (T_J) ---------- -40°C to +125°C

Electrical Characteristics

(V_{IN} =V_{OUT}+1V, or V_{IN}=2.3V, V_{EN}=V_{IN}, T_A = 25°C unless otherwise specified)

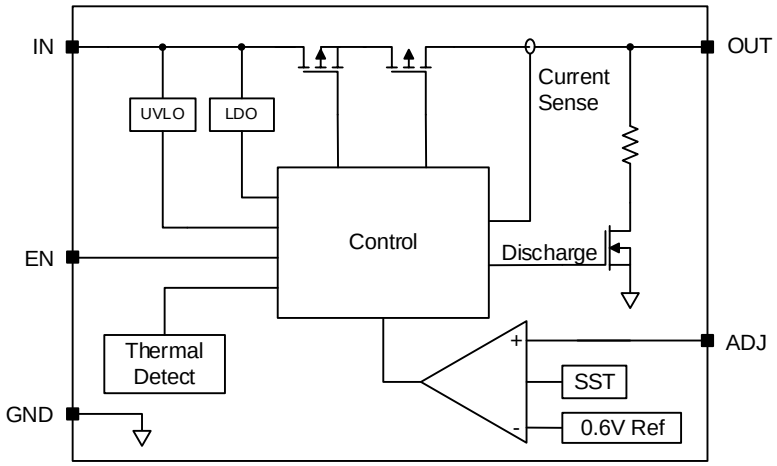
Parameter	Symbol	Test Conditions	Min	Typical	Max	Unit
Input Voltage	V_{IN}		2.3		30	V
Output Voltage Accuracy	V_{OUT}	I_O=100μA	-2		2	%
Line Regulation	ΔV_{LNR}	V_{IN}=(V_{OUT}+0.3) to 30V, I_O=100μA		0.04		%
Load Regulation	ΔV_{LDR}	I_O=0.1mA to 150mA		0.25	1	%
Dropout Voltage	V_{IN}-V_{OUT}	I_O=10mA		20		mV
		I_O=50mA		100		mV
		I_O=100mA		200		mV
		I_O=150mA		300		mV
Shutdown Current	I_{SHDN}	V_{EN}=0V, V_{IN}=24V		1		μA
Quiescent Current	I_Q	I_O=0.1mA		18	30	μA
		I_O=150mA		450		μA
Current Limit	I_{LIM}	V_{OUT}=0.9×V_{OUT}(normal)		350	500	mA
Reverse leakage current limit	I_{RLK}	V_{IN}= -15V, Load=500Ω		-0.1		uA
Power-supply Rejection Ratio	PSRR	f=1kHz, C_{OUT}=10μF		50		dB
Input UVLO Threshold	V_{UVLO}	V_{IN} rising			2.25	V
UVLO Hysteresis	V_{UVLO_TH}			100		mV
Shutdown Discharge Resistor				500		Ω
Enable Input Logic-High Voltage	V_{EN_H}	V_{IN}=2.8 to 5.5V	1.5			V
Enable Input Logic-Low Voltage	V_{EN_L}	V_{IN}=2.8 to 5.5V			0.6	V
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			20		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a two-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

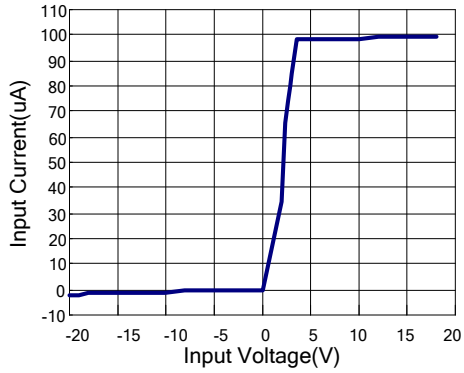
Function Block



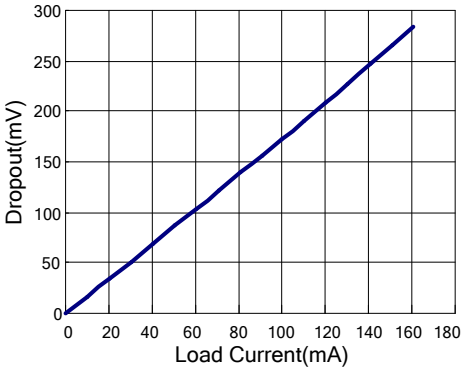
Typical Operating Characteristics

Input Current vs. Input Voltage

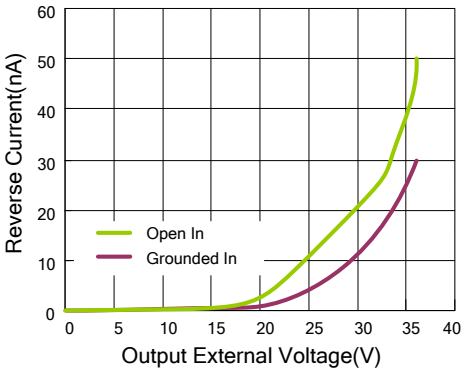
(V_{IN}=5V, V_{OUT}=3.3V, R_L=33ohm)



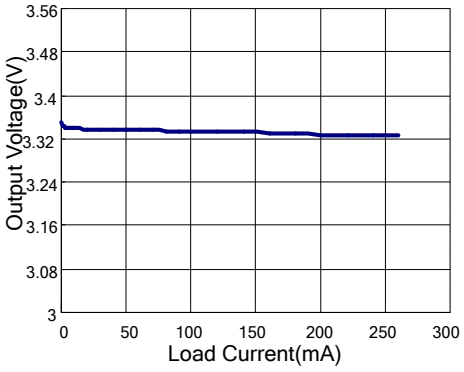
Dropout Voltage vs. Load Current



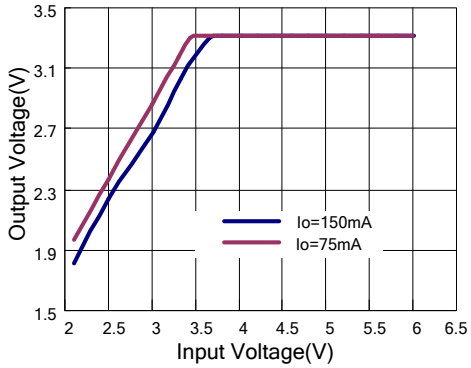
Reverse Current



Load Regulation

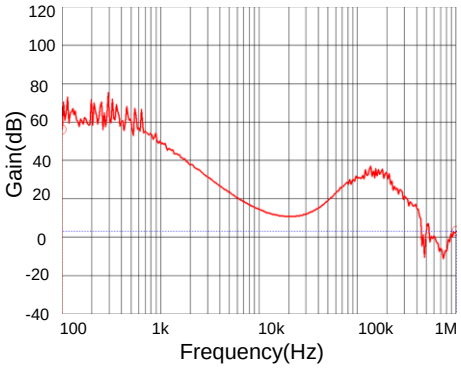


Line Regulation



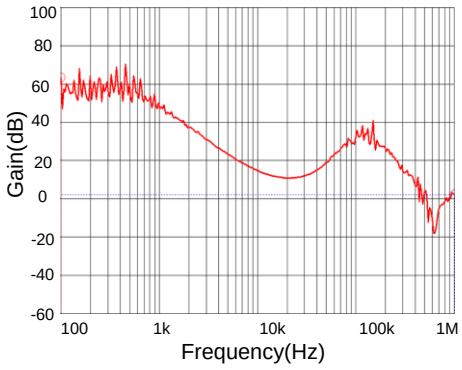
PSRR

(Vin=5,Vout=3.3,Iout=150mA)



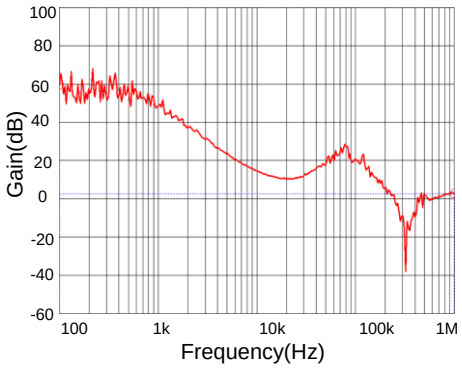
PSRR

(Vin=5,Vout=3.3,Iout=100mA)



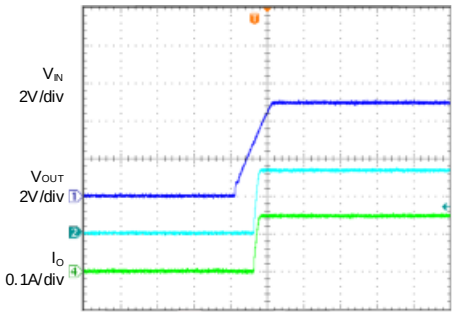
PSRR

(Vin=5,Vout=3.3,Iout=10mA)



Startup from V_{IN}

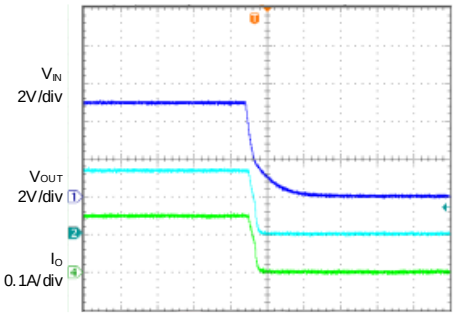
(V_{IN}=5.0V, V_{OUT}=3.3V, I_O=0.15A)



Time (1ms/div)

Shutdown from V_{IN}

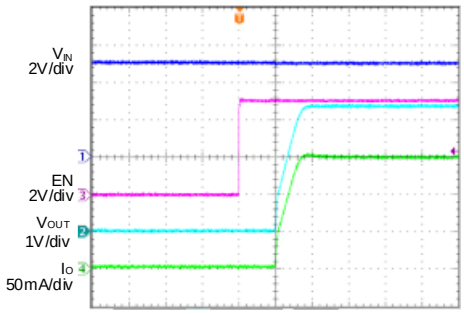
(V_{IN}=5.0V, V_{OUT}=3.3V, I_O=0.15A)



Time (1ms/div)

Startup from Enable

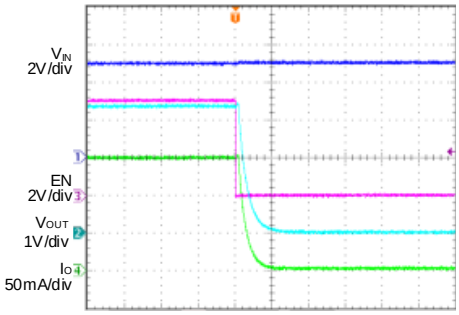
(V_{IN}=5.0V, V_{OUT}=3.3V, I_O=0.15A)



Time (200us/div)

Shutdown from Enable

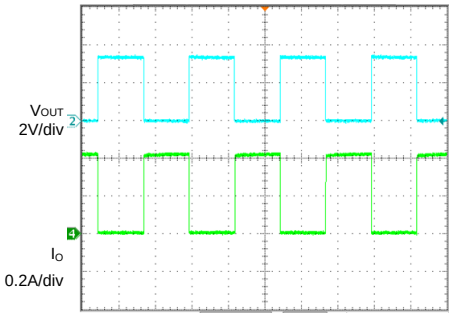
(V_{IN}=5.0V, V_{OUT}=3.3V, I_O=0.15A)



Time (200us/div)

Hard Short Protection

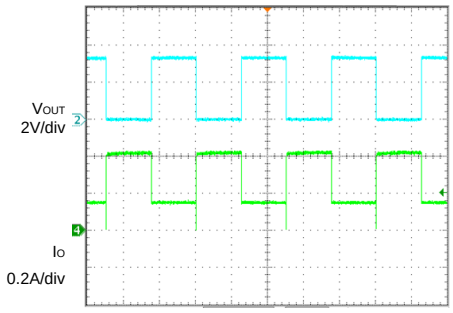
(V_{IN}=5.0V, V_{OUT}=3.3V, Null load to short)



Time (200ms/div)

Hard Short Protection

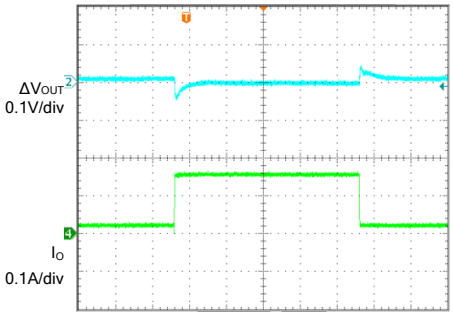
(V_{IN}=5.0V, V_{OUT}=3.3V, 0.15A to short)



Time (200ms/div)

Load Transient

(V_{IN}=5.0V, V_{OUT}=3.3V, I_O=15~150mA)



Time (40μs/div)

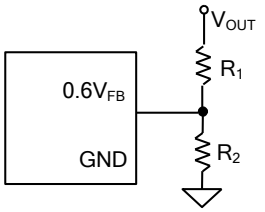
Application information

The SY6340 is a 150mA linear regulator with a low drop out voltage. Like any low-dropout regulator, SY6340 requires input and output decoupling capacitors.

Feedback Resistor Dividers R_1 and R_2:

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10kΩ and 1MΩ is highly recommended for both resistors. If V_{OUT} is 3.3V, R_1=100k is chosen, then using following equation, R_2 can be calculated to be 22.1k:

$$R_2 = \frac{0.6V}{V_{OUT} - 0.6V} R_1 .$$



Input Capacitor C_{IN}:

An input capacitor about 2.2μF is required between the device input pin and ground pin. A typical X5R or better grade ceramic capacitor is recommended in this application. This input capacitor must be located close to the device to minimize the input noise.

Output Capacitor C_{OUT}:

For transient stability, the SY6340 is designed specifically to work with very small ceramic output capacitors. 2.2μF output capacitance can be used in this application. Higher capacitance values help to improve transient. The output capacitor's ESR is critical because it forms a zero to provide phase lead which is required for loop stability.

Dropout Voltage:

The SY6340 has a very low dropout voltage due to its extra low $R_{DS(ON)}$ of the main PMOS determines the lowest usable supply.

$V_{DROPOUT}=V_{IN}-V_{OUT}=R_{DS(ON)}\times I_{OUT}$

Over Current and Short Circuit Protection:

The device includes over current and short circuit protection. The current limitation circuit regulates the output current to its limitation threshold to protect IC from damage. Under over current or short circuit condition, the power loss of the IC is relatively high. If have potential over current or short circuit scenario, the input voltage is not recommended to exceed 9V.

Thermal Considerations:

The SY6340 can deliver a current of up to 150mA over the full operating junction temperature range. However, the maximum output current must be derated at higher ambient temperature to ensure the junction temperature does not exceed 125℃. With all possible conditions, the junction temperature must be within the range specified under operating conditions. Power dissipation can be calculated based on the output current and the voltage drop across regulator.

$P_D=(V_{IN}-V_{OUT})\times I_{OUT}+V_{IN}\times I_{GND}$

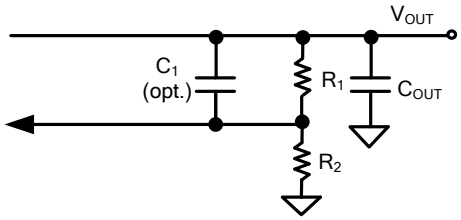
The final operating junction temperature for any set of condition can be estimated by the following thermal equation:

$P_{D(MAX)}=(T_{J(MAX)}-T_A)/\theta_{JA}$

Where $T_{J(MAX)}$ is the maximum junction temperature of die (125℃) and T_A is the maximum ambient temperature. The junction to ambient thermal resistance (θ_{JA}) footprint is 100℃/W for SOT23-5 package, 62℃/W for DFN2×2-6 package.

Load Transient Considerations:

The SY6340 integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a small ceramic capacitor in parallel with R_1 may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements.



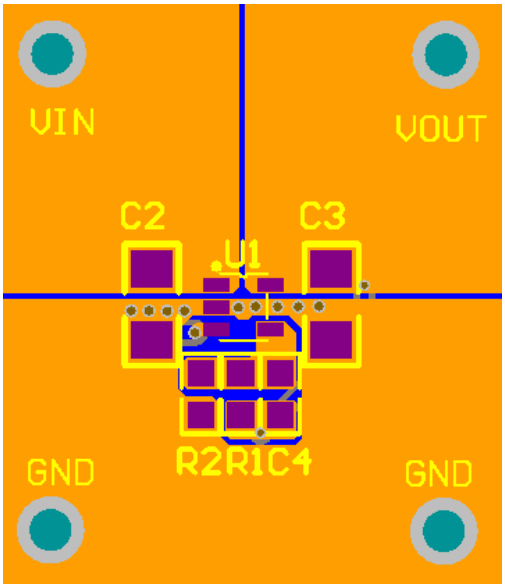
Layout Design:

Good board layout practices must be used or instability can be induced because of ground loops and voltage drops, and large PCB copper area can improve the thermal performance. The input and output capacitors MUST be directly connected to the input, output, and ground pins of the device using traces which have no other currents flowing through them.

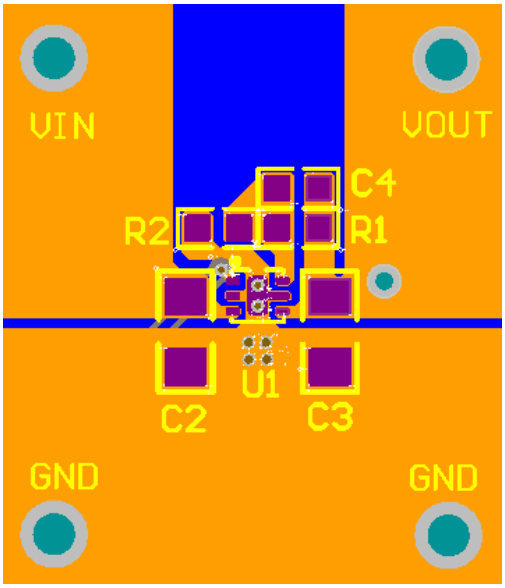
The best way to do this is to layout C_{IN} and C_{OUT} near the device with short traces to the V_{IN}, V_{OUT}, and ground pins. The regulator ground pin should be

connected to the external circuit ground so that the regulator and its capacitors have a “single point ground”.

Below is the recommended PCB layout diagram:

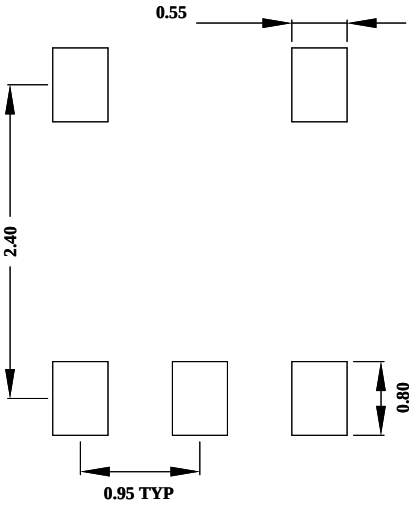


SOT23-5

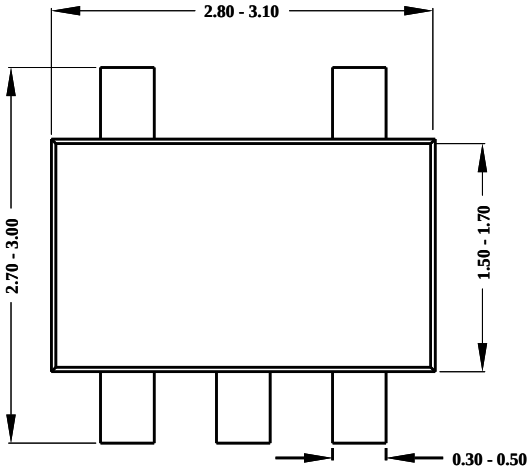


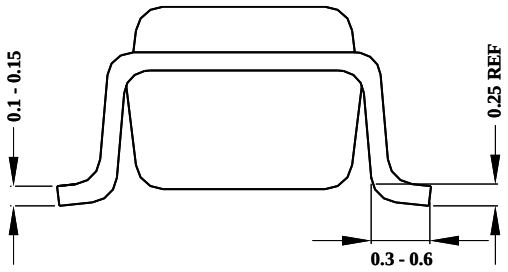
DNF2×2-6

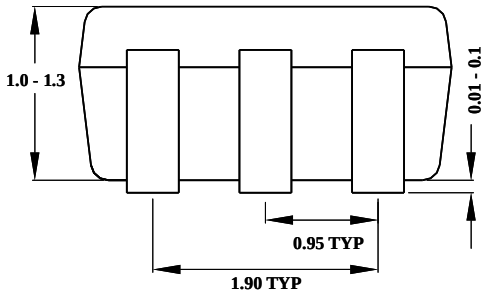
SOT23-5 Package outline & PCB layout design



Recommended Pad Layout

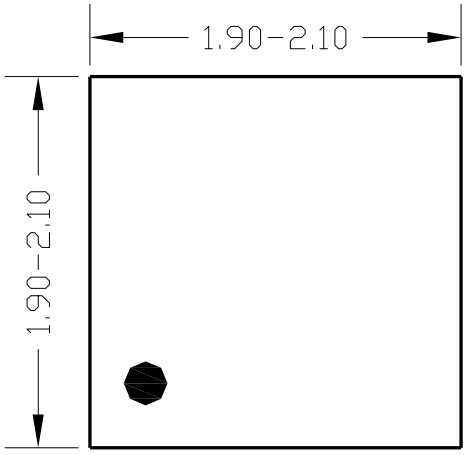




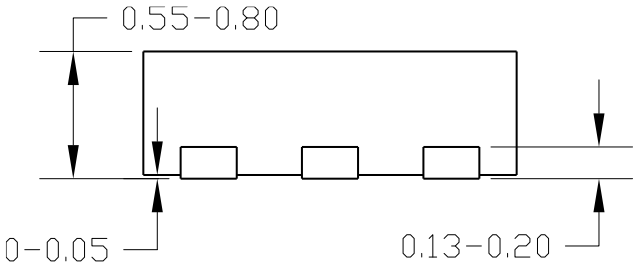


Notes: All dimensions are in millimeters.
All dimensions don't include mold flash & metal burr.

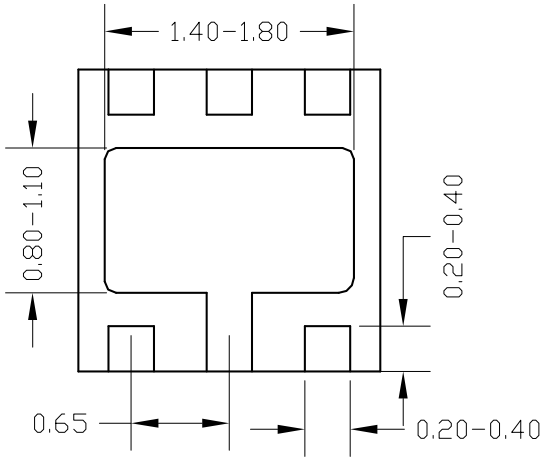
DFN2×2-6 Package outline



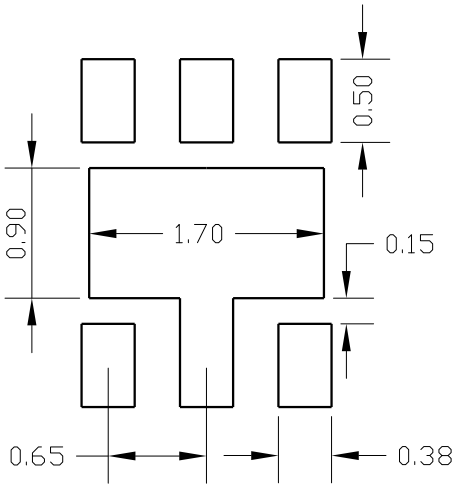
Top View



Side View



Bottom View



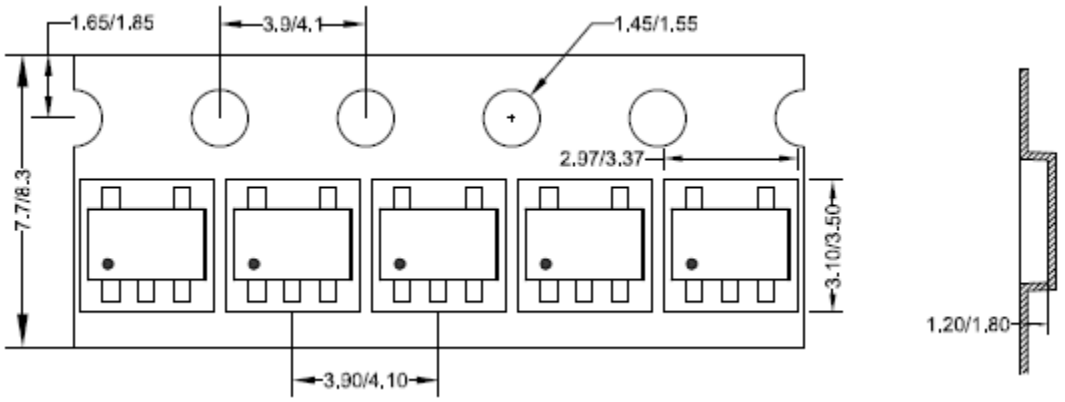
Recommended PCB layout

Notes: All dimensions are in millimeters.
All dimensions don't include mold flash & metal burr.

Taping & Reel Specification

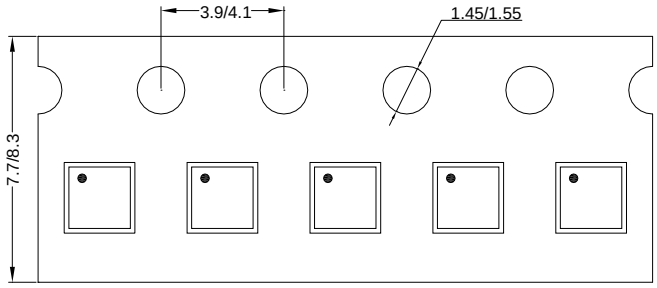
1. Taping orientation

SOT23-5



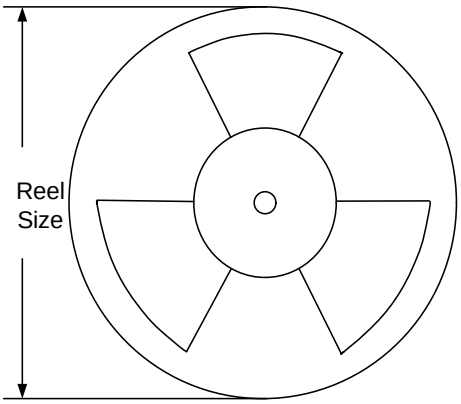
Feeding direction ⟶

2. DFN2×2 taping orientation



Feeding direction ⟶

3. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-5	8	4	7"	280	160	3000
DFN2×2	8	4	7"	400	160	3000

4. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Aug.20, 2023	Revision 1.0	Initial Production Release

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