SY67221

Dual H-bridge Stepper Motor Driver IC with I²C Integrated

General Description

The SY67221 is a four half-bridge driver solution for DC brush motors, bipolar stepper motors, solenoids, or other inductive loads. The highly integrated half-H-bridge driver block consists of half-H-bridge with internal logic control, gate driver, over current protection and charge pump circuit. I²C communication is also supported.

The SY67221 provides complete protection functions with a fault output pin for open circuit detection (OCD), over current protection (OCP), short circuit protection (SCP), under voltage lockout (UVLO) and thermal shutdown (TSD). A low-power sleep mode is also provided. The device is packaged in a 16-pin TSSOP.

Features

- Power Supply Voltage Range from 2.7V to 18V
- Different Operation Mode
  - Two H-bridge Operation with Four INx Input
  - Two H-bridge Operation with Two INx Input
  - One H-bridge Operation with Two INx Input, Parallel Operation
  - Four Half-H-bridge Operation with Four INx Input
- Maximum Drive Current of 1.5A RMS Current for Each H-bridge@T_A=25°C
- Internal Integrated Open Circuit Detection, Over Current Protection, Short Circuit Protection, Under Voltage Lockout and Thermal Shutdown
- Low-power Sleep Mode
- Fault Indication
- TSSOP16 Package

Ordering Information

SY67221 □(□□□)

- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY67221HKP	TSSOP-16	

Applications

- Refrigerators
- DC Brush Motors
- Solenoid Valve Load

Typical Application

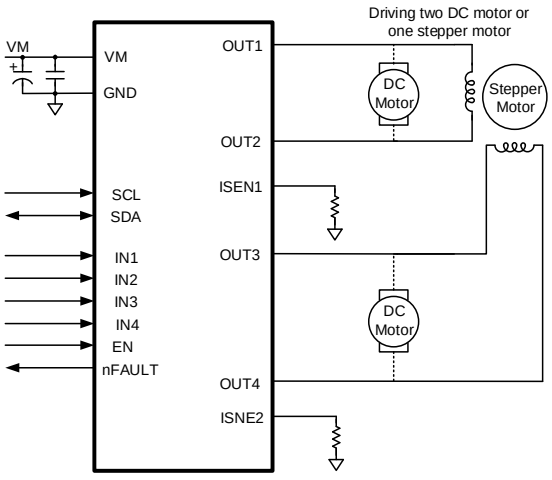

Figure1. Typical Application Circuit

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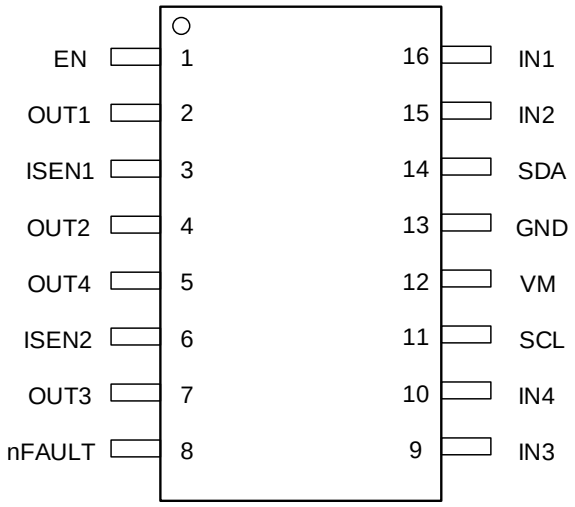
Pin out (Top View)



(TSSOP-16)

Top Mark: ENE*xyz* (device code: **ENE**, ***x=year code, y=week code, z= lot number code)***

Pin Name	Pin No.	Description
EN	1	Internal logic enable pin. Set this pin to logic high to enable the device. Logic low puts device in low-power sleep mode, this pin has an internal pulldown resistor.
OUT1	2	Half bridge 1 output pin. Connect this pin to motor winding.
ISEN1	3	Half bridge 1 and Half bridge 2 current sense pin. Connect a resistor between this pin and GND for current control, or connect to GND if current control is not needed.
OUT2	4	Half bridge 2 output pin. Connect this pin to motor winding.
OUT4	5	Half bridge 4 output pin. Connect this pin to motor winding.
ISEN2	6	Half bridge 3 and Half bridge 4 current sense pin. Connect a resistor between this pin and GND for current control, or connect to GND if current control is not needed
OUT3	7	Half bridge 3 output pin. Connect this pin to motor winding.
nFAULT	8	Fault state output pin. Logic low if fault is detected.
IN3	9	Half bridge 3 input pin. Control the state of bridge 3, this pin has an internal pull-down resistor.
IN4	10	Half bridge 4 input pin. Control the state of bridge 4, this pin has an internal pull-down resistor
SCL	11	I^2C clock input pin.
VM	12	Motor power supply pin. Decouple this pin to GND pin with a 0.1μF ceramic capacitor and a sufficient electrolytic capacitor.
GND	13	Device ground pin.
SDA	14	I^2C data signal pin.
IN2	15	Half bridge 2 input pin. Control the state of bridge 2, this pin has an internal pull-down resistor.
IN1	16	Half bridge 1 input pin. Control the state of bridge 1, this pin has an internal pull-down resistor.

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Block Diagram

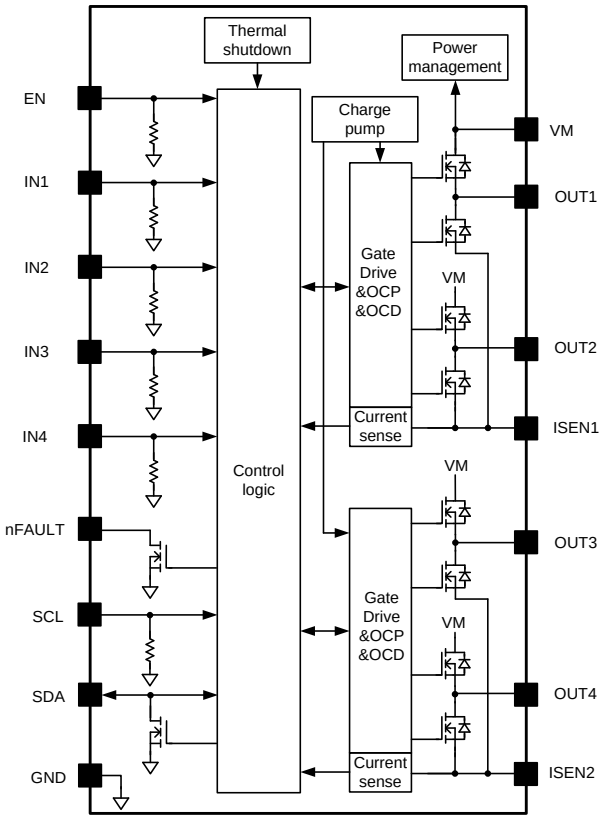

Figure3. SY67221 Block Diagram

Absolute Maximum Ratings (Note 1)

VM, OUTx, nFAULT ---------- 24V
INx, EN---------- -0.3V to 16V
SDA, SCL ---------- -0.3V to 16V
ISENx ---------- -0.4V to 0.4V
Ambient Temperature (T_A) ---------- -40°C to +125°C
Junction Temperature (T_J) ---------- -40°C to +150°C
Storage Temperature ---------- -65°C to +150°C
Electrostatic Discharge
HBM (Human Body Model) ---------- ±4kV
CDM (Charge Device Model) ---------- ±1kV
TSSOP16 Package Thermal Resistance (Note 2)
θ_{JA} ---------- 101.5°C/W
θ_{JCTOP} ---------- 24°C/W

Recommended Operating Conditions

VM, OUTx ---------- 2.7V to 18V
INx, EN---------- -0.1V to 5.5V
SDA, SCL ---------- -0.1V to 5.5V
H-Bridge Output RMS Current (Note3) ---------- less than 1.5A
Operation Ambient Temperature Range ---------- -40°C to 85°C
Operation Junction Temperature Range ---------- -40°C to 125°C

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Electrical Characteristics

(T_A = 25°C, VM=12V, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Power Supply						
VM Operating Supply Current	I_{VM}	VM=12V, INx=L, EN=H, SDA=SCL=H		2.3	3.5	mA
VM Sleep Mode Current	I_{VMS}	VM=12V, EN=L			3.8	μA
VM Under Voltage Lockout Voltage	V_{UVLO_RISE}	VM Rising		2.5	2.7	V
	V_{UVLO_FALL}	VM Falling	2	2.2		V
Logic Level Input						
Input Low Voltage	V_{IL}	EN, INx, SDA, SCL			0.6	V
Input High Voltage	V_{IH}	EN, INx, SDA, SCL	1.6			V
Input Low Current	I_{IL}	V_{IN}=0V			0.5	μA
Input High Current	I_{IH}	V_{IN}=5V			35	μA
Input Deglitch Time	t_{DEG}	(Note 4)		450		ns
nFAULT/SDA Output (Open-Drain Output)						
Output Low Voltage	V_{OL}	I_O=5mA			0.5	V
Output High Leakage Current	I_{OH}	V_O=3.3V			0.5	μA
H-Bridge MOSFETs						
High Side MOSFETs on Resistance	R_{dson}			350		mΩ
Low Side MOSFETs on Resistance				320		
Off-State Leakage Current	I_{OFF}		-0.5		+0.5	μA
Motor Driver						
Rise Time	t_R	VM=12V,OUT to GND with 16Ω, 10% to 90% V_M, (Note 4)		300		ns
Fall Time	t_F			200		ns
Propagation Delay INx to OUTx	t_{PROP}	(Note 4)		0.6		μs
Dead Time	t_{DEAD}	(Note 4)		200		ns
Current Control						
ISENx Trip Voltage	V_{TRIP}	Gain at 100%	135	150	165	mV
		Gain at 50%	63.75	75	86.25	mV
Current Sense Blanking Time	t_{BLANK}			2		μs
Current Regulate off Time	t_{OFF}			20		μs
Protection						
Output Over Current Protection	I_{OCP}		1.55	1.85	2.15	A
Over Current Retry Time	t_{OCPR}	(Note 4)		10		ms
Over Current Deglitch Time	t_{DEG}	(Note 4)		5		μs
Open Circuit Detection Current Threshold	I_{OCD}	<15nF on OUTx		270		μA
Thermal Shutdown Temperature	T_{SD}	(Note 4)		160		°C
Thermal Shutdown Hysteresis	T_{HYS}	(Note 4)		40		°C
Sleep Mode						
Startup Time	t_{WAKE}	EN Inactive high to H-bridge on (Note 4)			1.5	ms

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I²C Interface						
SCL Clock Frequency	f_{SCL}	(Note 4)			400	kHz
Bus Free Time between Stop/Start	t_{BUF}	(Note 4)	1.3			µs
Start Condition (Repeated) Hold Time	$t_{HD,STA}$	(Note 4)	600			ns
Repeat START Set up Time	$t_{SU,STA}$	(Note 4)	600			ns
Set up Time for STOP	$t_{SU,STO}$	(Note 4)	600			ns
Data Set up Time	$t_{SU,DAT}$	(Note 4)	100			ns
Data Hold Time	$t_{HD,DAT}$	(Note 4)	0		900	ns
Data Output Fall Time	t_{Of}	(Note 4)	20+ $0.1C_B$		300	ns

Note 1: Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2: θ_{JA}, θ_{JCTOP} is measured in the natural convection at T_A = 25°C on Silergy EVB.

Note 3: Power dissipation and thermal limits must be observed.

Note 4: Guaranteed by design and sample tested at bench.

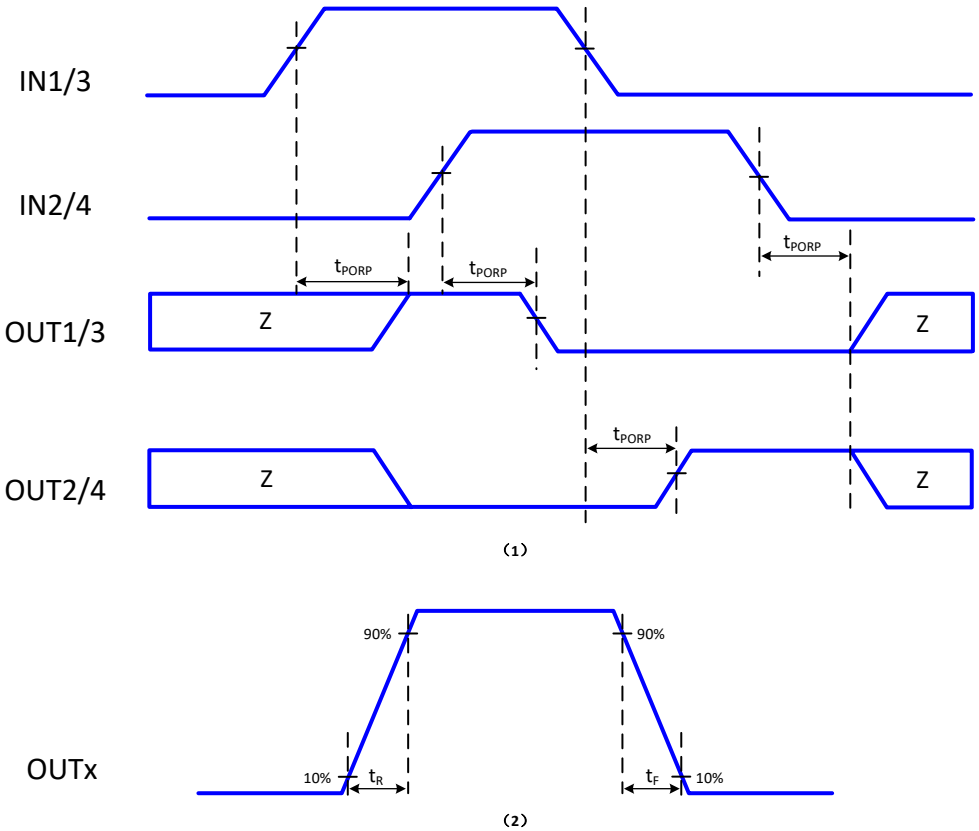

Figure 4. Timing Diagram

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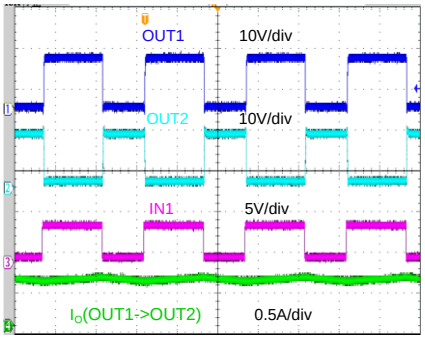
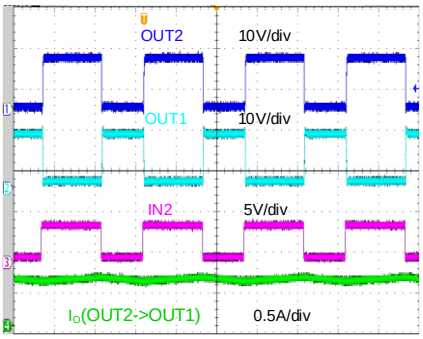
Operation Waveform

Forward
(mode0,VM=12V,IN1=20k,IN2=0,Io=0.5A,Rsense=0)



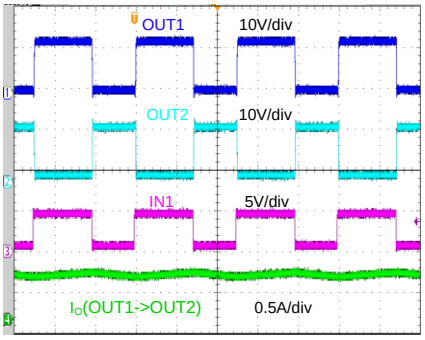
Time (20μs/div)

Reverse
(mode0,VM=12V,IN1=0,IN2=20k,Io=0.5A,Rsense=0)



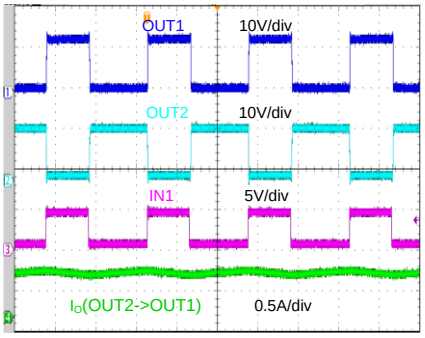
Time (20μs/div)

Forward
(mode1,VM=12V,IN1=20k,IN2=0,Io=0.5A,Rsense=0)



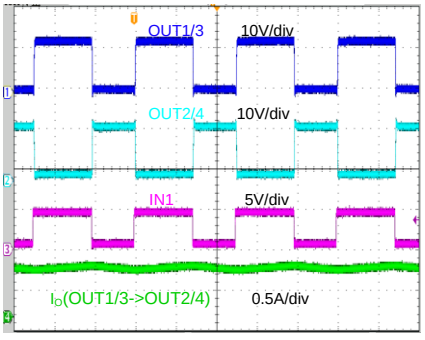
Time (20μs/div)

Reverse
(mode1,VM=12V,IN1=0,IN2=20k,Io=0.5A,Rsense=0)



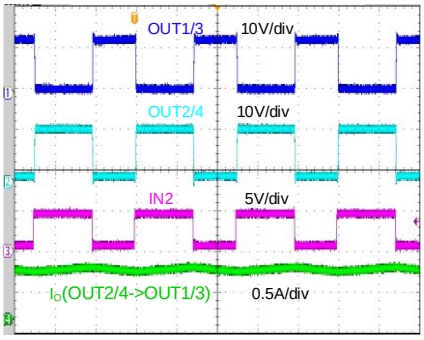
Time (20μs/div)

Forward
(mode2,VM=12V,IN1=20k,IN2=0,Io=0.5A,Rsense=0)



Time (20μs/div)

Reverse
(mode2,VM=12V,IN1=0,IN2=20k,Io=0.5A,Rsense=0)



Time (20μs/div)

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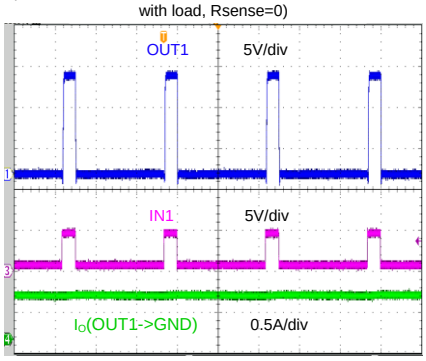
Forward

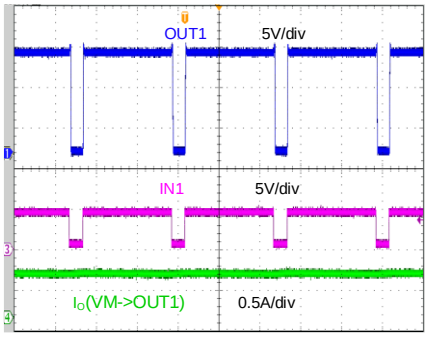
(mode3,VM=12V,IN1=20k,Io=0.5A, OUT connect to GND with load, Rsense=0)



Time (20μs/div)

Reverse

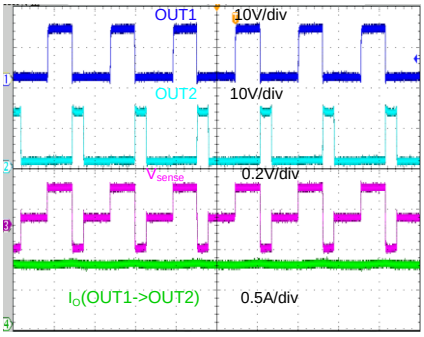
(mode3,VM=12V,IN1=20k,Io=0.5A, OUT connect to VM with load, Rsense=0)



Time (20μs/div)

Current Regulation

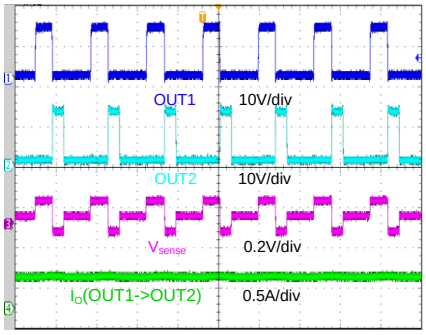
(Gain=100% mixed decay, VM=12V,IN1=5V,IN2=0, Rsense=0.2Ω)



Time (20μs/div)

Current Regulation

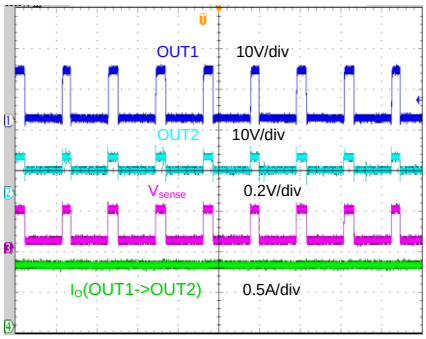
(Gain=50% mixed decay, VM=12V,IN1=5V,IN2=0, Rsense=0.2Ω)



Time (20μs/div)

Current Regulation

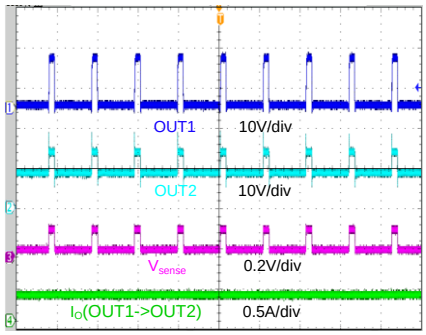
(Gain=100% Slow decay, VM=12V,IN1=5V,IN2=0, Rsense=0.2Ω)



Time (20μs/div)

Current Regulation

(Gain=50% Slow decay, VM=12V,IN1=5V,IN2=0, Rsense=0.2Ω)



Time (20μs/div)

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Functional Description

PWM Motor Drivers

SY67221 contains two identical H-bridge motor drivers with current-control PWM circuitry. A block diagram of the circuitry is shown below:

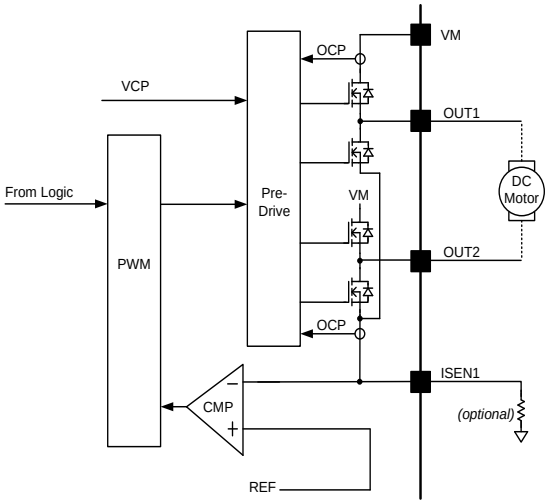
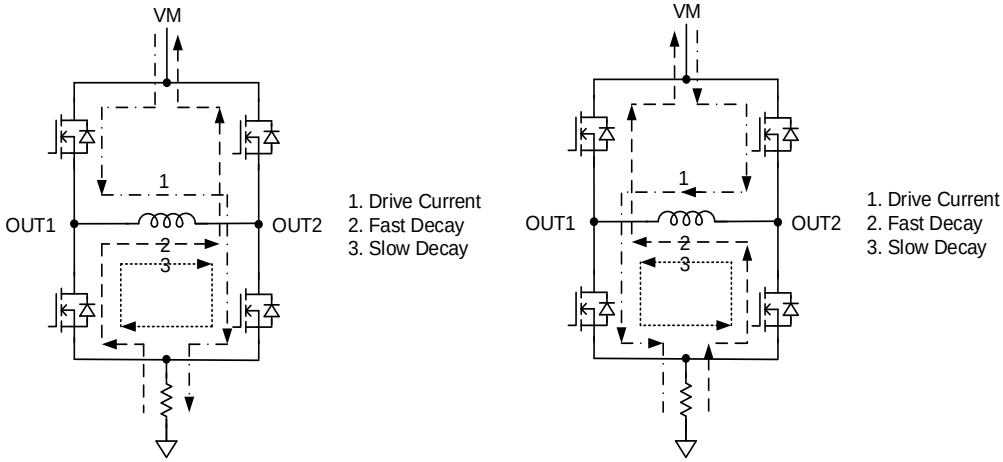


Figure 5. Motor Control Circuitry

Figure 6 shows the current paths in different drive and decay modes.



Forward Reverse

Figure 6. Decay Mode

Power MOSFETs Driving Control

The Bridge is controlled by I^2C or by INx input interface. The following table shows the operation mode control logic of the device:

Table 1 Mode Control Logic

PIN control	I^2C control	Four Half-H bridge work mode
HWMODE=4'b0000	MODE REGISTER	
SDA=L, SCL=L	11b	Half-H-bridge, Mode3
SDA=L, SCL=H	10b	One H-bridge, Mode2
SDA=H, SCL=L	01b	Two H-bridge, Mode1

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SDA=H, SCL=H	00b	Two H-bridge, Mode0

MODE 0 (Two H-bridge, four INx control input)

In this mode, SY67221 is configured to driver a stepper motor or two brushed DC motor.

Table 2 Mode 0 Truth table

EN	IN1	IN2	IN3	IN4	OUT1	OUT2	OUT3	OUT4	Function
0	X	X	X	X	Z	Z	Z	Z	Sleep mode
1	0	0			Z	Z			Coast
1	0	1			L	H			Reverse
1	1	0			H	L			Forward
1	1	1			L	L			Brake
1			0	0			Z	Z	Coast
1			0	1			L	H	Reverse
1			1	0			H	L	Forward
1			1	1			L	L	Brake

MODE 1 (Two H-bridge, IN1, IN2 control input)

In this mode, SY67221 is configured to driver a stepper motor or two brushed DC motor with lower number of control inputs to save the I/O of MCU.

Table 3 Mode 1 Truth table

EN	IN1	IN2	IN3	IN4	OUT1	OUT2	OUT3	OUT4	Function
0	X	X	X	X	Z	Z	Z	Z	Sleep mode
1	0		X	X	L	H			Reverse
1	1		X	X	H	L			Forward
1		0	X	X			L	H	Reverse
1		1	X	X			H	L	Forward

MODE 2 (One H-bridge, IN1, IN2 control input)

In this mode, SY67221 is configured to driver a brushed DC motor with larger current.

Table 4 Mode 2 Truth table

EN	IN1	IN2	IN3	IN4	OUT1	OUT2	OUT3	OUT4	Function
0	X	X	X	X	Z	Z	Z	Z	Sleep mode
1	0	0	X	X	Z	Z	Z	Z	Coast
1	0	1	X	X	L	H	L	H	Reverse
1	1	0	X	X	H	L	H	L	Forward
1	1	1	X	X	L	L	L	L	Brake

MODE 3 (Four Half-H-bridge, four INx control input)

In this mode, SY67221 is configured to driver four independent loads such as relays and other inductive loads.

Table 5 Mode 3 Truth table

EN	IN1	IN2	IN3	IN4	OUT1	OUT2	OUT3	OUT4	Function
0	X	X	X	X	Z	Z	Z	Z	Sleep mode
1	0				L				OUT1=L
1	1				H				OUT1=H
1		0				L			OUT2=L
1		1				H			OUT2=H
1			0				L		OUT3=L
1			1				H		OUT3=H
1				0				L	OUT4=L

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1				1				H	OUT4=H

Current Control

The current through the motor windings may be limited, or controlled, by a fixed-frequency PWM current regulation, or current chopping. For DC motors, current control is used for limiting the start-up and stalling current of the motor. For stepper motors, current control is used frequently at all times.

When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage and inductance of the winding. If the current reaches the current chopping threshold, the bridge will disable the current until the beginning of the next PWM cycle. Note that immediately after the current is enabled, the voltage on the ISENx pin is ignored for a fixed period of time before enabling the current sense circuitry. This blanking time is fixed at about 2μs. This blanking time also sets the minimum on time of the PWM when operating in current chopping mode.

The PWM chopping current is set by a comparator which compares the voltage across a current sense resistor connected to the ISENx pins with a reference voltage.

The chopping current is calculated in Equation 1.

$$I_{CHOP} = \frac{Gain \times V_{TRIP}}{R_{SENSE}} \quad (1)$$

Example:

CONT 2 bit[4] DECAY=1b,once the chopping current threshold is reached, the H-bridge will switch to slow decay mode. Winding current is re-circulated by enabling both of the low-side FETs in the bridge. This state is held until the beginning of the next fixed-frequency PWM cycle.

Note that if current control is not needed, the ISENx pins should be connected directly to ground.

Current Recirculation and Decay Modes

During PWM current trip operation, the H-bridge is enabled to drive current through the motor winding until the trip threshold of the current regulation is reached. After the trip current threshold is reached, the drive current is interrupted, but, because of the inductive nature of the motor, current must continue to flow for some time. This continuous flow of current is called recirculation current. A mixed decay allows a better current regulation by optimizing the current ripple by using fast and slow decay.

Mixed decay is a combination of fast and slow decay modes. Mixed decay starts with fast decay, then goes to slow decay. In the SY67221 device, the mixed decay ratio is 25% fast decay and 75% slow decay as shown in Figure 7.

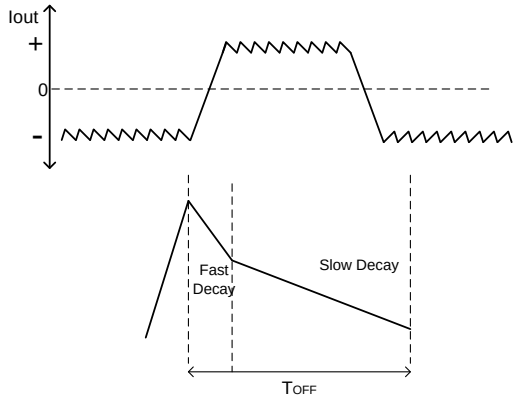

Figure 7. Current Regulation and Decay timing

Sleep Mode

Driving EN pin low will put the device into a low power sleep state. In this state, the H-bridges are disabled, all internal logic is reset, and all internal clocks are stopped. All inputs are ignored until the EN pin is pulled logic high. When returning from sleep mode, some time needs to pass before the motor driver becomes fully operational.

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Multi-Slave Operation

Figure 8 shows the schematic diagram of SY67221 Multi-slave operation. Multi-slave operation can use a microcontroller to control multiple devices at the same time. The steps to configure the multi-slave of SY67221 are as follows：

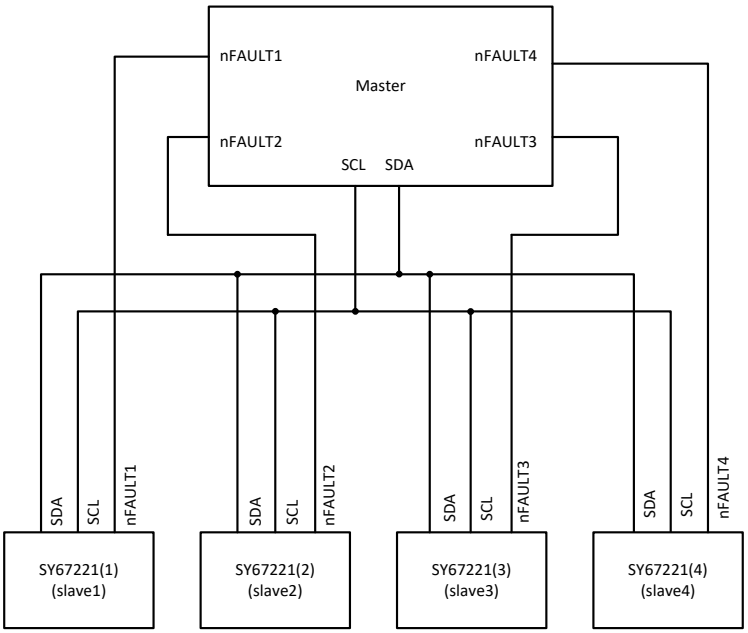

Figure 8. Multi-Slave Operation of SY67221

- Scan the addresses of all cascaded slavers, configure *CONT2*(0x02) to 0x40, disable nFAULT;
- Select a slaver, and then pull down the nFAULT PIN of the remaining slaver, 0x00 (address of 0x60) write an arbitrary number as the new address of the selected slaver (for example, write 0x61 for 0x00), Pull down the slaver's nFAULT
- Then select a slaver to cancel its external pull-down state, and write an arbitrary number with 0x00 as the new address (for example, 0x00 write 0x62, pay attention to be different from the previous 0x61), Pull down the slaver's nFAULT. other slavers can be deduced by analogy;
- Configure *CONT2*(0x02) to 0x00, restore the DISFLT bit to the default state, and then cancel the external pull-down of all slaver's nFAULT;
- Now all connected slave devices can be accessed using the newly reprogrammed address;
- The above steps should be repeated for any device in case of a power reset (EN).

Protection Circuits

The device is fully protected against under voltage lockout, over current protection, open circuit detection and thermal shutdown.

Under Voltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled, and all internal logic will be reset. Operation will resume when VM rises above the UVLO threshold. nFAULT is driven low in the event of an undervoltage condition.

Over Current Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET. If this analog current limit persists for longer than the OCP regulation time, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. The driver will be re-enabled after the OCP retry period (t_{OCPR}) has passed; nFAULT becomes high again at this time. If the fault condition is still present, the cycle repeats. If the fault is no longer present, normal operation resumes. Please note that only the H-bridge in which the OCP is detected will be disabled while the other bridge will function normally. The SY67221 has a programmable option for auto-retry or the latch mode. If *CONT2* bit[3] OCPR=0b, OCP is in retry mode. If *CONT2* bit[3] OCPR=1b, OCP is in latch mode. Overcurrent conditions

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are detected independently on both high and low side devices; i.e., a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown.

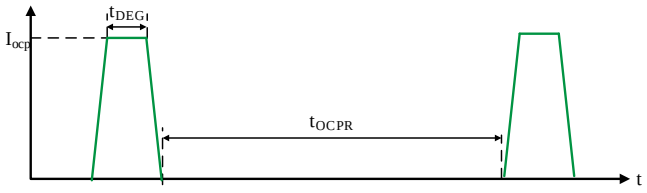


Figure 9. SY67221 OCP Waveform

Open Circuit Detection (OCD)

Both high-side and low-side switches of the half-bridge power outputs are capable of detecting an open circuit. OCD runs at power up or when the device comes out from sleep mode, and also can run at any time by using OCDOD bit. The OCD implementation is done on the full-bridge and the half-bridge. In the SY67221 device, during an open circuit condition, the half-bridges, full-bridges, or both bridges (depending on the MODE bit) are always operating and the nFAULT pin is pulled low, the user must reset the power to release the nFAULT pin by doing the OCD sequence again. In the SY67221 device, the user can program the full-bridge or half-bridge to be in the operating mode or the Hi-Z state, whenever an open circuit condition is detected by using the OCDBO bit. Moreover, the nFAULT signaling on the OCD bit can be disabled using the OCDOD bit.

Thermal Shut down (TSD)

If the die temperature exceeds safe limits, all MOSFETs in the both H-bridge are disabled. Once the die temperature has fallen to a safe level, operation automatically resumes.

I^2C Compatible Interface

The SY67221 features an I^2C interface that allows the HOST processor to program or to control the motor. The I^2C interface supports clock speeds of up to 400 kHz and uses standard I^2C commands. The SY67221 always operates as a slave device, and is addressed using a 7-bit slave address followed by an 8^{th} bit, which indicates whether the transaction is a read-operation or a write-operation.

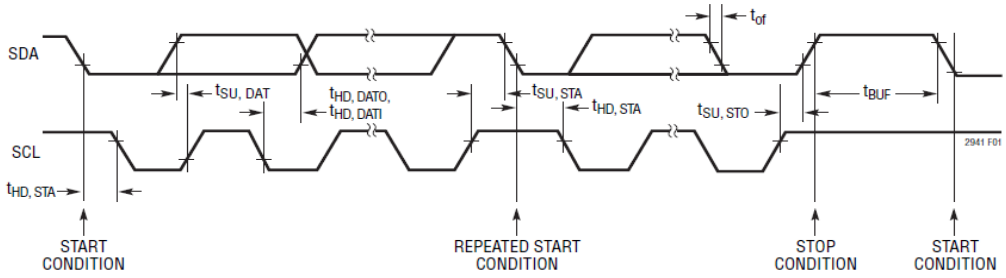
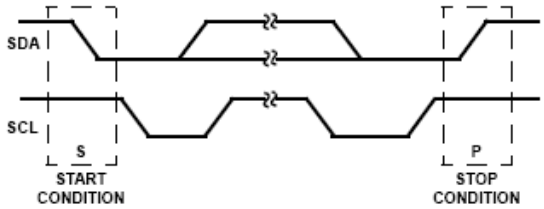


Figure 10. I^2C Timing Diagram

START and STOP Conditions

The SY67221 is controlled via an I^2C compatible interface. The START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition. The I^2C master always generates the START and STOP conditions.



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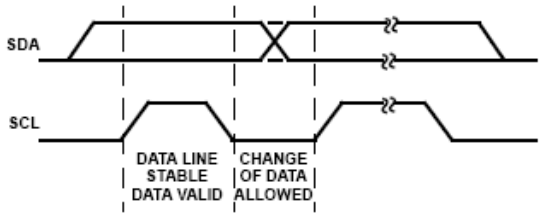
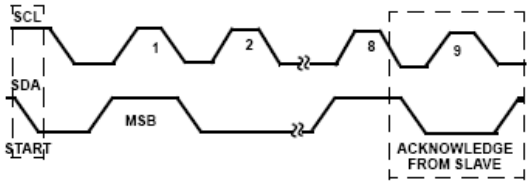
Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.



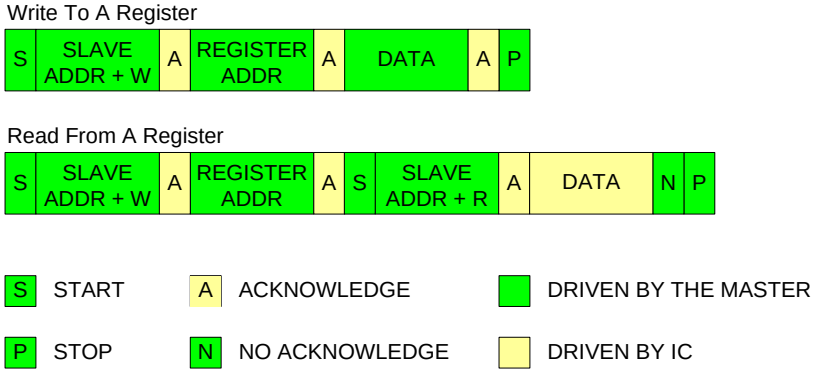
Acknowledge:

Each address and data transmission uses 9-clock pulses. The ninth pulse is the acknowledge bit (ACK). After the START condition, the master sends 7-slave address bits and an R/$\overline{W}$ bit during the next 8-clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge. The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data.



Data Transactions:

All transactions start with a control byte sent from the I²C master device. The control byte begins with a START condition, followed by 7-bits of slave address 0x60 followed by the 8th bit, R/$\overline{W}$ bit. The R/$\overline{W}$ bit is 0 for a write or 1 for a read. If any slave devices on the I²C bus recognize their address, they will acknowledge by pulling the SDA line low for the last clock cycle in the control byte. If no slaves exist at that address or are not ready to communicate, the data line will be 1, indicating a Not Acknowledge condition. Once the control byte is sent, and the SY67221 acknowledges it, the 2nd byte sent by the master must be a register address byte. The register address byte tells the IC which register the master will write or read. Once the SY67221 receives a register address byte it responds with an acknowledge signal.



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Register Map

Table 6. Registers

Add.	Sym.	Des.	R/W	7	6	5	4	3	2	1	0
0x00	SL_ADD	Slave address	R/W	RSVD	1	1	0	0	0	0	0
0x01	CONT1	IC control	R/W	GAIN	IN4	IN3	IN2	IN1	I2CBC	MODE	
0x02	CONT2	IC control	R/W	CLFLT	DISFLT	RSVD	DECAY	OCPR	OCDOD	OCDFD	OCDBO
0x03	STATUS1	IC status	R	RSVD	RSVD	RSVD	FLT	OCP	OCD	TSD	UVLO
0x04	STATUS2	IC status	R	OCD4	OCD3	OCD2	OCD1	OCP4	OCP3	OCP2	OCP1
0x05	STATUS3	IC status	R	RSVD						OCDBY	RSVD
0x06	STATUS4	OCD/OCP Status	R	OCD4RC	OCD3RC	OCD2RC	OCD1RC	OCP4RC	OCP3RC	OCP2RC	OCP1RC
0x07	STATUS5	IC status	R	RSVD	RSVD	RSVD	RSVD	HWMODE			

CONT1 register (Address= 0x01, default 0x00)

Bit	Name	R/W	Reset	Description
7	GAIN	R/W	0b	0b= 100% 1b= 50%
6	IN4			Bridge operation input
5	IN3			
4	IN2			
3	IN1			
2	I2CBC			0b= Using INx pins to control the bridge; 1b= Using INx bits to control the bridge
1,0	MODE			00b=4 pin interface 01b= 2 pin interface 10b= Parallel interface 11b= Independent interface

CONT2 register (Address= 0x02, default 0x00)

Bit	Name	R/W	Reset	Description
7	CLRFLT	R/W	0b	Set 1 to clear all FAULT bits other than the OCD and OCDx bits. This bit reset to 0b after clearing all the faults.
6	DISFLT	R/W		0b= nFAULT pin enable 1b= nFAULT pin disable
5	RSVD	R		-
4	DECAY	R/W		0b= 25% fast decay, 75% slow decay 1b= 100% slow decay
3	OCPR	R/W		0b= OCP auto retry 1b= OCP latch
2	OCDOD	R/W		0b= Idle 1b= OCD on demand is actived
1	OCDFD	R/W		0b= Fault signaling on OCD 1b= No Fault signaling on OCD
0	OCDBO	R/W		0b= Bridge operating on OCD 1b= Bridge Hi-Z on OCD

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STATUS1 register (Address= 0x03, default 0x00)

Bit	Name	R/W	Reset	Description
7	RSVD	R	0b	-
6	RSVD	R		-
5	RSVD	R		-
4	FLT	R		0b= No Fault detected 1b= Fault detected
3	OCP	R		0b= No OCP detected 1b= OCP detected
2	OCD	R		0b= No OCD detected 1b= OCD detected
1	TSD	R		0b= No TSD detected 1b= TSD detected
0	UVLO	R		0b= No UVLO detected 1b= UVLO detected

STATUS2 register (Address= 0x04, default 0x00)

Bit	Name	R/W	Reset	Description
7	OCD4	R	0b	0b= No OCD detected on OUT4 1b= OCD detected on OUT4
6	OCD3	R		0b= No OCD detected on OUT3 1b= OCD detected on OUT3
5	OCD2	R		0b= No OCD detected on OUT2 1b= OCD detected on OUT2
4	OCD1	R		0b= No OCD detected on OUT1 1b= OCD detected on OUT1
3	OCP4	R		0b= No OCP detected on OUT4 1b= OCP detected on OUT4
2	OCP3	R		0b= No OCP detected on OUT3 1b= OCP detected on OUT3
1	OCP2	R		0b= No OCP detected on OUT2 1b= OCP detected on OUT2
0	OCP1	R		0b= No OCP detected on OUT1 1b= OCP detected on OUT1

STATUS3 register (Address= 0x05, default 0x00)

Bit	Name	R/W	Reset	Description
7,6,5,4,3,2	RSVD	R	0b	-
1	OCDBUSY	R		0b= OCD end 1b= OCD ongoing
0	RSVD	R		-

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STATUS4 register (Address= 0x06, default 0x00)

Bit	Name	R/W	Reset	Description	
7	OCD4RC	R	0b	0b= No OCD detected on OUT4 1b= OCD detected once on OUT4	Once OCD detected on OUTx, and can't be clear even the circuit is normal, only be cleared by EN=0, CLFLT and power cycle.
6	OCD3RC	R		0b= No OCD detected on OUT3 1b= OCD detected once on OUT3	
5	OCD2RC	R		0b= No OCD detected on OUT2 1b= OCD detected once on OUT2	
4	OCD1RC	R		0b= No OCD detected on OUT1 1b= OCD detected once on OUT1	
3	OCP4RC	R		0b= No OCP detected on OUT4 1b= OCP detected once on OUT4	Once OCP detected on OUTx, and can't be clear even the circuit is normal, only be cleared by EN=0, CLFLT and power cycle.
2	OCP3RC	R		0b= No OCP detected on OUT3 1b= OCP detected once on OUT3	
1	OCP2RC	R		0b= No OCP detected on OUT2 1b= OCP detected once on OUT2	
0	OCP1RC	R		0b= No OCP detected on OUT1 1b= OCP detected once on OUT1	

STATUS5 register (Address= 0x07, default 0x00)

Bit	Name	R/W	Reset	Description
7,6,5,4	RSVD	R	0b	-
3,2,1,0	HWMODE			4b'0000= Hardware mode, SDA pin and SCL pin logic decides the half H bridge work mode: SDA / SCL / MODE L / L / MODE3 L / H / MODE2 H / L / MODE1 H / H / MODE0 Once I^2C enable, the default value of the *STATUS5* register becomes 0x01 and hardware mode disable.

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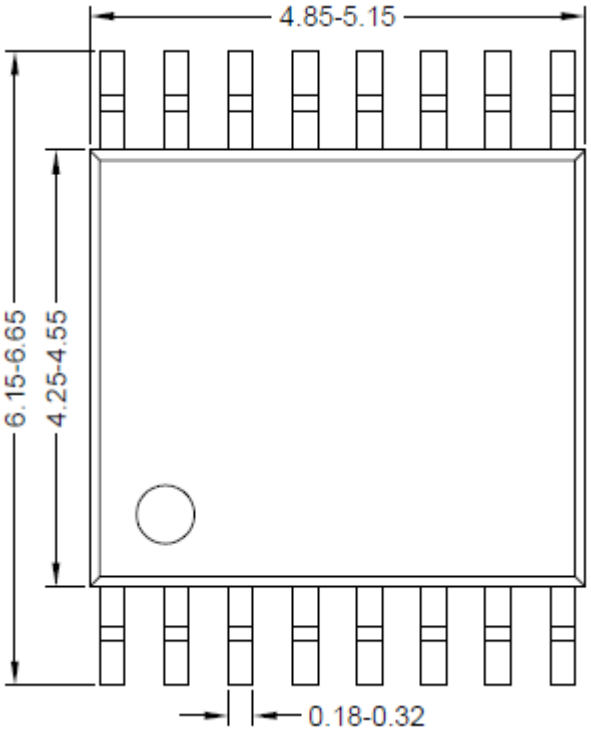
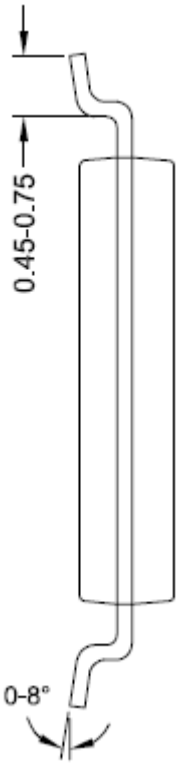
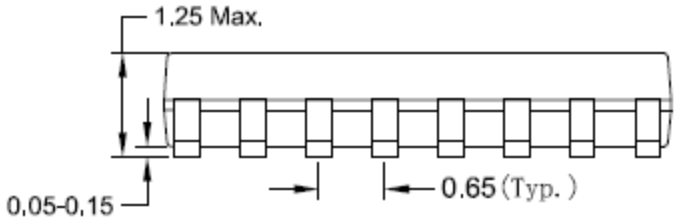
TSSOP16 Package Outline Drawing



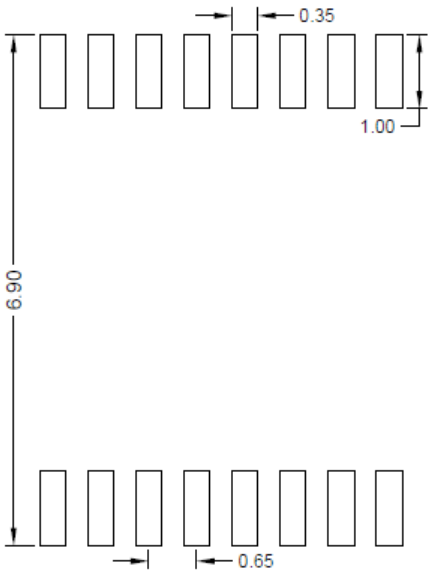
Top view



Side view A



Side view B



Recommended PCB Layout

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

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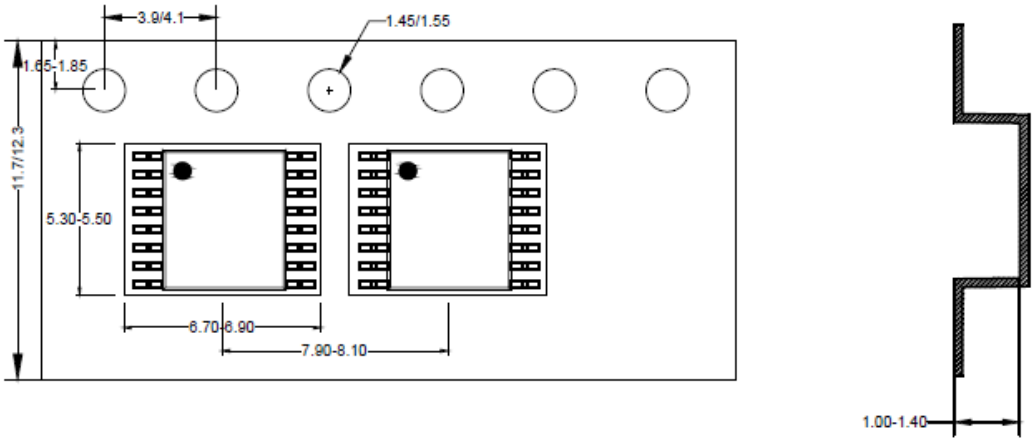
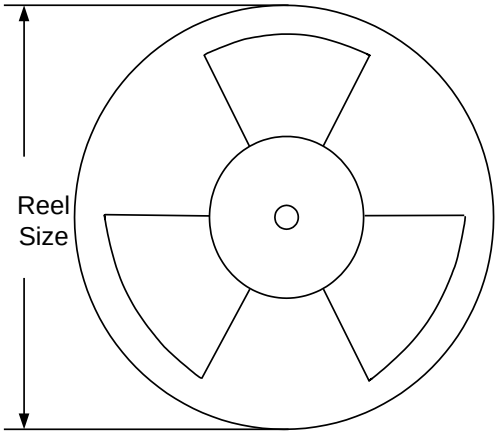
Taping & Reel Specification

1. TSSOP16 Taping orientation



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
TSSOP16	12	8	13"	400	400	3000

3. Others: NA

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Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Dec 07, 2024	Revision 1.0	Production Release
Dec 07, 2023	Revision 0.9C	1. page 6 Modify the marked areas in red circles according to the notes 2. page 7 Modify the marked areas in red circles according to the notes 3. 0x00 SL_ADD register type from R change to R/W
Oct 24, 2023	Revision 0.9B	Add ESD information
Aug. 25, 2022	Revision 0.9A	Update power supply recommended capacitor from “Decouple this pin to GND pin with a 10μF ceramic capacitor and a sufficient electrolytic capacitor.” to "Decouple this pin to GND pin with a 0.1μF ceramic capacitor and a sufficient electrolytic capacitor."
Apr.1, 2021	Revision 0.9	Initial Release

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