SY6821A

Single 4A, Ultra Low Loss Load Switch

General Description

The SY6821A is a single 4A load switch, 2.5V-5.5V V_{BIAS} with internal charge pump. It develops an ultra-low $R_{DS(ON)}$ load switch for power distribution in computer systems. Ultra low power loss and tiny DFN1.5×1.5-6 compatible package achieves small solution size.

Ordering Information

SY6821 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY6821ADQC	DFN 1.5×1.5-6	

Features

- Input Voltage Range: 0.6V to 3.6V
- Bias Range: 2.5V to 5.5V
- Low $R_{DS(ON)}$ for Internal Pass Switch:16mΩ
- Maximum Output Current: 4A
- Accurate Turn on Threshold to Allow Programmable Turn on Delay to Enable Power Sequencing
- Programmable Turn on Slew Rate
- Quiescent Bias Current: 100μA
- Automatic Shutdown Discharge: 100Ω
- RoHS Compliant and Halogen Free
- Compact Package: DFN1.5×1.5-6

Applications

- Notebook PC
- Desktop PC
- Server
- Set Top Box
- E-Book
- LCD-TV
- Portable Device

Typical Applications

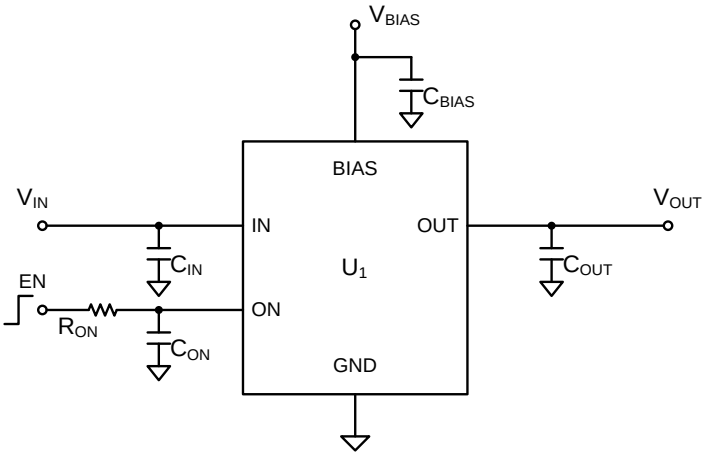

Figure 1. Schematic Diagram

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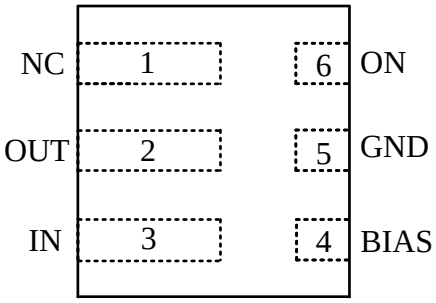
Pinout (Top view)



(DFN1.5×1.5-6)

Top Mark: ZB*xyz* (device code: **ZB**, ***x=year code, y=week code, z= lot number code)***

Pin Name	Pin Number	Pin Description
NC	1	Leave this pin floating or connect it to the OUT pin.
OUT	2	Output pin.
IN	3	Input pin.
BIAS	4	Bias supply for overdriving the gate of the pass switch between input and output.
GND	5	Ground pin.
ON	6	ON/OFF control. Connect this pin to RC circuit (as shown in Figure 1) to control slew rate and turn on delay.

Block Diagram

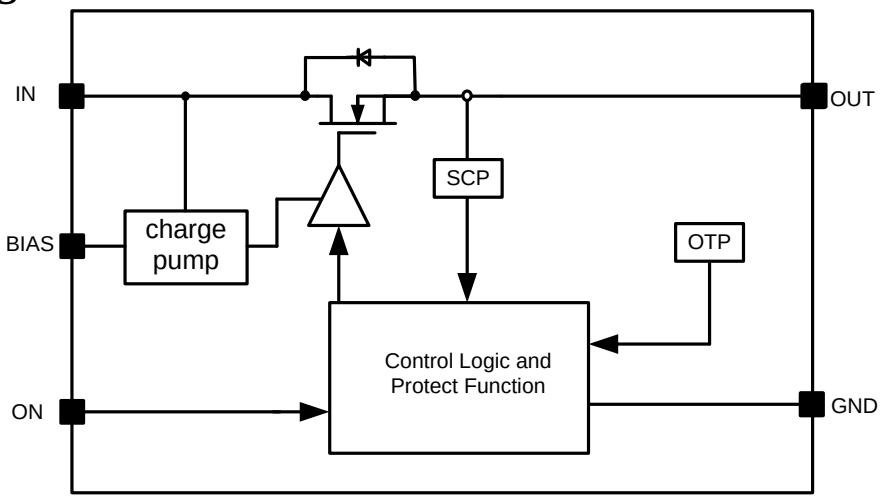


Figure2. Block Diagram

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Absolute Maximum Ratings (Note 1)

IN,OUT---------- 4.2V
BIAS,ON---------- 6V
Power Dissipation, P_D @ T_A = 25°C
DFN1.5×1.5-6---------- 1.6W
Package Thermal Resistance (Note 2)
θ_{JA}, DFN1.5×1.5-6----------145.33°C /W
θ_{JC}, DFN1.5×1.5-6----------81.21°C /W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
ESD Susceptibility (Note 2)
HBM (Human Body Mode) ---------- 2kV
MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 3)

IN, OUT ---------- 0.6V to 3.6V
BIAS ---------- 2.5V to 5.5V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

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Electrical Characteristics

(V_{IN} = 3.3V, V_{BIAS}=5V, T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		0.6	3.3	3.6	V
Bias Voltage Range	V_{BIAS}		2.5		5.5	V
Shutdown Bias Current	I_{SHDN}	ON=0		2		μA
Quiescent Bias Current	I_{BIAS}	ON=3.3V, I_{OUT}=0		100		μA
FET R_{ON}	$R_{DS(ON)}$	V_{IN} = 0.6V to 3.6V, V_{BIAS} = 3V to 5.5V, I_{LOAD}=1A		16		mΩ
Bias UVLO Threshold	$V_{BIAS,UVLO}$				2.4	V
Bias UVLO Hysteresis	$V_{BIAS,HYS}$			0.2		V
ON Clamping Threshold	$V_{ON,CLP}$		1.16	1.26	1.36	V
Turn On Slew Rate		ON=3.3V, C_{OUT}=20μF, R_{ON}=300k Ω		7		V/ms
Min Rise Time	t_{RISE_MIN}			100		μs
Min Delay Time	t_{DELAY_MIN}	C_{ON}=NULL		300		μs
Discharge Resistor	$R_{DISCHARGE}$	EN=0V		100		Ω
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective four-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

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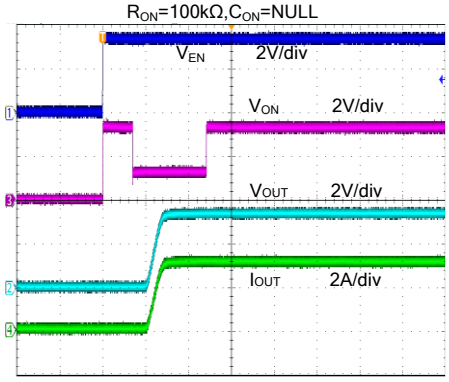
Typical Operating Characteristics

Startup From Enable

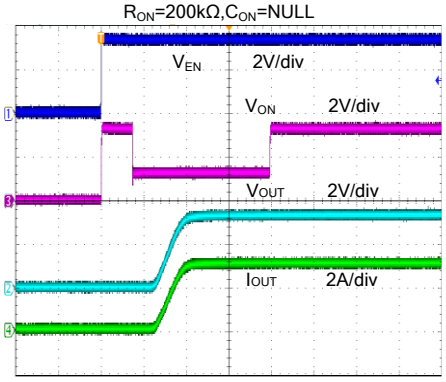
V_{IN}=3.3V,V_{BIAS}=5V,V_{EN}=3.3V,R_{LOAD}=1.1Ω,
R_{ON}=100kΩ,C_{ON}=NULL



Time (400us/div)

Startup From Enable

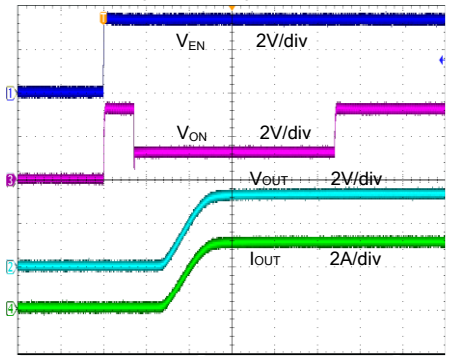
V_{IN}=3.3V,V_{BIAS}=5V,V_{EN}=3.3V,R_{LOAD}=1.1Ω,
R_{ON}=200kΩ,C_{ON}=NULL



Time (400us/div)

Startup From Enable

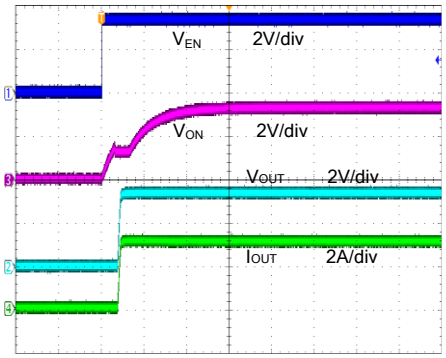
V_{IN}=3.3V,V_{BIAS}=5V,V_{EN}=3.3V,R_{LOAD}=1.1Ω,
R_{ON}=300kΩ,C_{ON}=NULL



Time (400us/div)

Startup From Enable

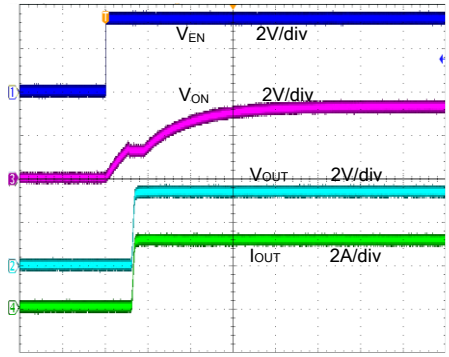
V_{IN}=3.3V,V_{BIAS}=5V,V_{EN}=3.3V,R_{LOAD}=1.1Ω,
R_{ON}=100kΩ,C_{ON}=10nF



Time (2ms/div)

Startup From Enable

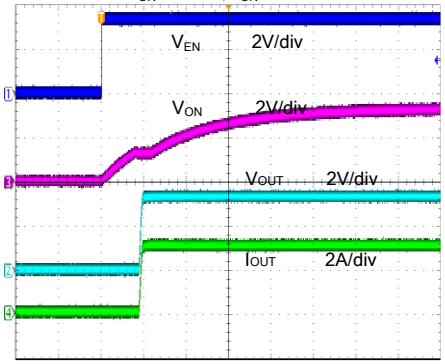
V_{IN}=3.3V,V_{BIAS}=5V,V_{EN}=3.3V,R_{LOAD}=1.1Ω,
R_{ON}=100kΩ,C_{ON}=20nF



Time (2ms/div)

Startup From Enable

V_{IN}=3.3V,V_{BIAS}=5V,V_{EN}=3.3V,R_{LOAD}=1.1Ω,
R_{ON}=100kΩ,C_{ON}=30nF



Time (2ms/div)

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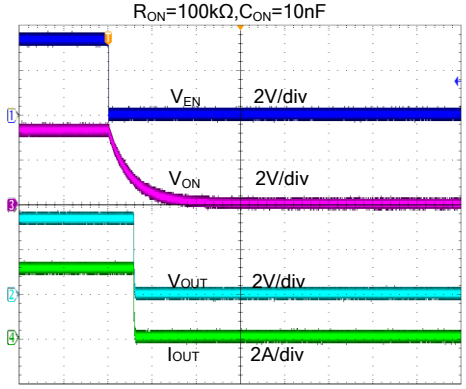
Shutdown From Enable

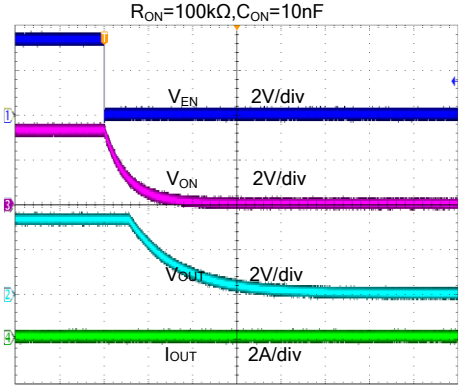
V_{IN}=3.3V,V_{BIAS}=5V,V_{EN}=3.3V,R_{LOAD}=1.1Ω,
R_{ON}=100kΩ,C_{ON}=10nF



Time (2ms/div)

Shutdown From Enable

V_{IN}=3.3V,V_{BIAS}=5V,V_{EN}=3.3V,R_{LOAD}=NULL,
R_{ON}=100kΩ,C_{ON}=10nF



Time (2ms/div)

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Operation

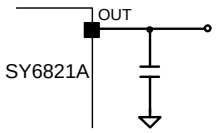
The SY6821A is a single 4A, ultra low loss load switch. It develops an ultra-low $R_{DS(ON)}$ load switch for power distribution in computer systems. The turn on delay time and rise time can be programmed by R_{ON} and C_{ON} connected to the EN pin.

Applications Information

Supply Filter Capacitor:
In order to limit the voltage drop on the input supply during hot-plug events, a 2.2μF ceramic capacitor placed close to IN and GND pins is recommended. Higher values of C_{IN} can be used for further reducing the voltage drop during high current application.

Bias Filter Capacitor:
A 0.1μF ceramic capacitor should be placed between the BIAS and the GND pins to bypass the high frequency noise of bias supply.

Output Filter Capacitor:
A 2.2μF output ceramic capacitor is recommended to be placed close to the IC and output connector to reduce voltage drop during load transient. Higher values of C_{OUT} can be used for further reducing the voltage drop during high current application. If long cables are connected to the output terminals, an anti-parallel schottky diode is suggested to be placed on the output terminal to absorb the negative ringing caused by the cable inductance.



Output Turn on Delay and Rise Time:
Turn on delay time and rise time can be easily programmed by R_{ON} and C_{ON}. The delay time can be calculated using following equation:

$$T_{Delay} = R_{ON} \times C_{ON} \times \ln\left(\frac{V_{EN}}{V_{EN} - 1.26}\right)$$

The minimum delay time is 300μs.

The rise time is proportional to $\frac{R_{ON}}{V_{EN} - 1.26}$, where V_{EN} is the control input voltage. The typical rise time is 380μs when R_{ON}=300kΩ, V_{EN}=3.3V, V_{IN}=3.3V

Output Discharge:
When the MOSFET is off, a 100Ω on-chip load resistor is connected to the output to quickly discharge the output.

Short Circuit Protection:
When the V_{DS} of the MOSFET exceeds 200mV, a hard short condition is detected. The device will latch off until the ON pin is reset.

PCB Layout Guide

For best performance of the SY6821A, the following guidelines must be strictly followed:

1. Keep all power trace as short and wide as possible. And it is desirable to use 4-layer or 6-layer board for thermal performance and better capability of current flow. At least 6 vias are suggested to put around each power pin to distribute current to different PCB layer. These power pins include V_{IN}, V_{OUT}.
2. Place the input capacitor close to the IC, and output capacitor close to the IC and connectors for better transient performance.
3. Place bias capacitor close to the IC to reduce the noise on bias supply.

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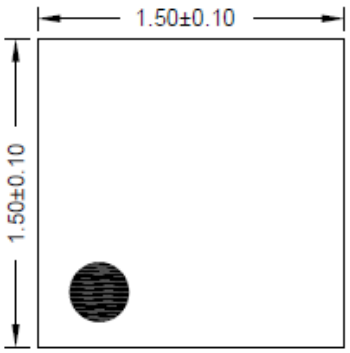
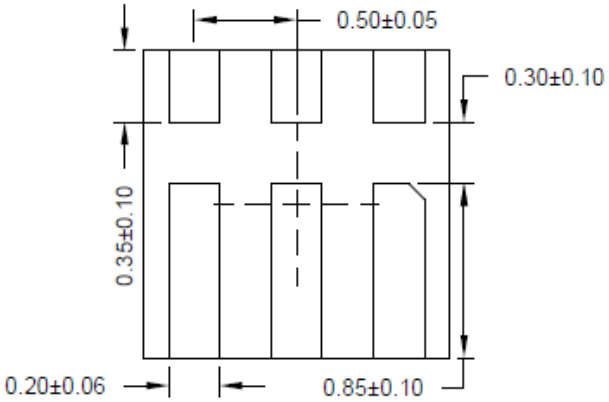
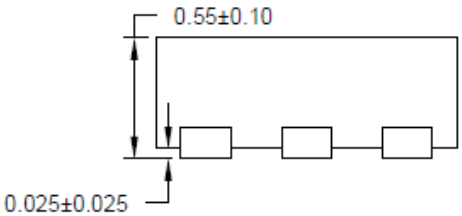
DFN1.5×1.5-6 Package Outline



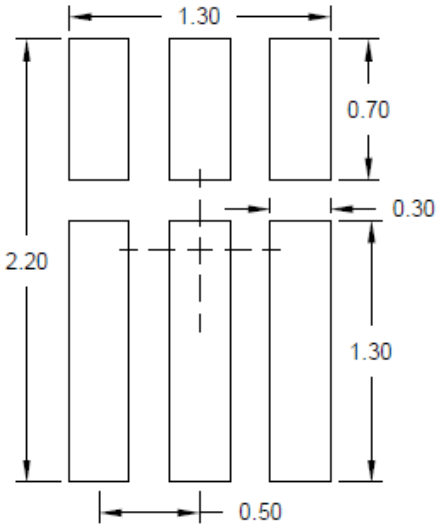
Top View



Bottom View



Side View



Recommended PCB layout
(only for reference)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

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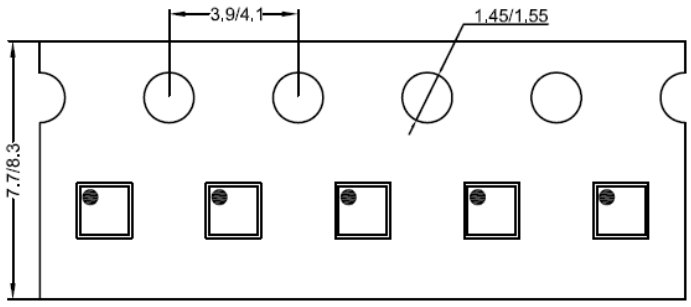
Taping & Reel Specification

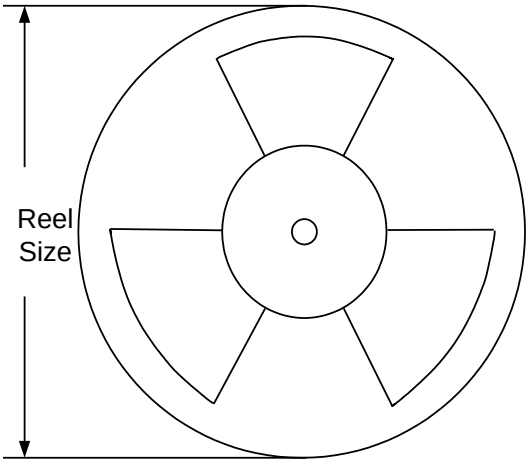
1. Taping orientation

DFN1.5x1.5



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN1.5x1.5	8	4	7"	400	160	3000

3. Others: NA

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