Application Note: AN_SY6907

2.5A, Single Cell Li-Ion DC/DC Switching Charger with I^2C Control, USB OTG, Power Path Management

General Description

SY6907 is a fully-integrated switching battery charger with an I^2C serial interface and system power path management devices for single cell Li-ion and Li-polymer battery in a wide range of tablets and other portable devices.

SY6907 supports the standard USB host port, the USB charging port and the high power DC adapter. The device takes the result from detection circuit in the system, such as USB PHY device. Meanwhile, SY6907 meets USB On-The-Go operation power rating specification by supplying 5V on VBUS with current limit up to about 1A.

The power path management keeps the system voltage from dropping below 3.5V minimum system voltage (programmable), even when the battery is completely depleted or removed. In order to prevent overloading the input source, when the input current limit or voltage limit is reached, the power path management will reduce the charging current to zero firstly, and will discharge the battery to provide the power required by system.

The device initiates and completes a charging cycle without control of the software. It automatically detects the battery voltage and charges the battery in three phases: trickle current, constant current and constant voltage. At the end of the charging cycle, the charger will automatically terminate when the charge current is below a preset limit in the constant voltage phase. When the full battery falls below the recharge threshold, the charger will automatically start another charging cycle. The device contains the negative thermistor monitoring, charging safety timer and over-voltage / over-current protections for safe charging and system operation. The thermal regulation will reduce charge current when the junction temperature exceeds 120 ℃ (programmable).

The /PG output in SY6907 indicates whether a good power source is present or not. The STAT output reports the charging status and all fault conditions. The INT will immediately notify the host when a fault occurs.

SY6907 is available in a 24-pin, 4x4mm^2 QFN package.

Ordering Information

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SY6907 □(□ □)□
        |  |   └ Temperature Code
        |  └──── Package Code
        └─────── Optional Spec Code
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Ordering Number	Package type	Note
SY6907QCC	QFN4×4-24	

Features

- Single Input USB-Compliant/Adapter Charger
  - Input Voltage and Current Limit Supports USB2.0 and USB 3.0
  - Input Current Limit: 100mA, 150mA, 500mA, 900mA, 1A, 1.5A, 2A and 3A
- 3.9V–6 V Input Operating Voltage Range
- USB OTG 5V at about 1A Synchronous Boost Converter Operation
- Narrow VDC (NVDC) Power Path Management
- 1.5MHz Switching Frequency for Low Profile Inductor
- Autonomous Battery Charging with or without Host Management
- High Accuracy
  - ±1% Charge Voltage Regulation
  - ±10% Fast Charge Current Regulation
  - ± 2% Output Regulation in Boost Mode
- High Integration
  - Power Path Management
  - Synchronous Switching MOSFETs
  - Integrated Current Sensing
  - Bootstrap Diode
  - Internal Loop Compensation
- Safety
  - Battery Temperature Sensing and Charging Safety Timer
  - Thermal Regulation and Thermal Shutdown
  - Input System Over Voltage Protection
  - MOSFET Over Current Protection
  - Charge Status Outputs for LED or Host Processor
- Low Battery Leakage Current and Support Shipping Mode

Applications

- Tablet PC
- Smart Phone
- Portable Audio Speaker
- Portable Media Players
- Internet Device

Typical Application

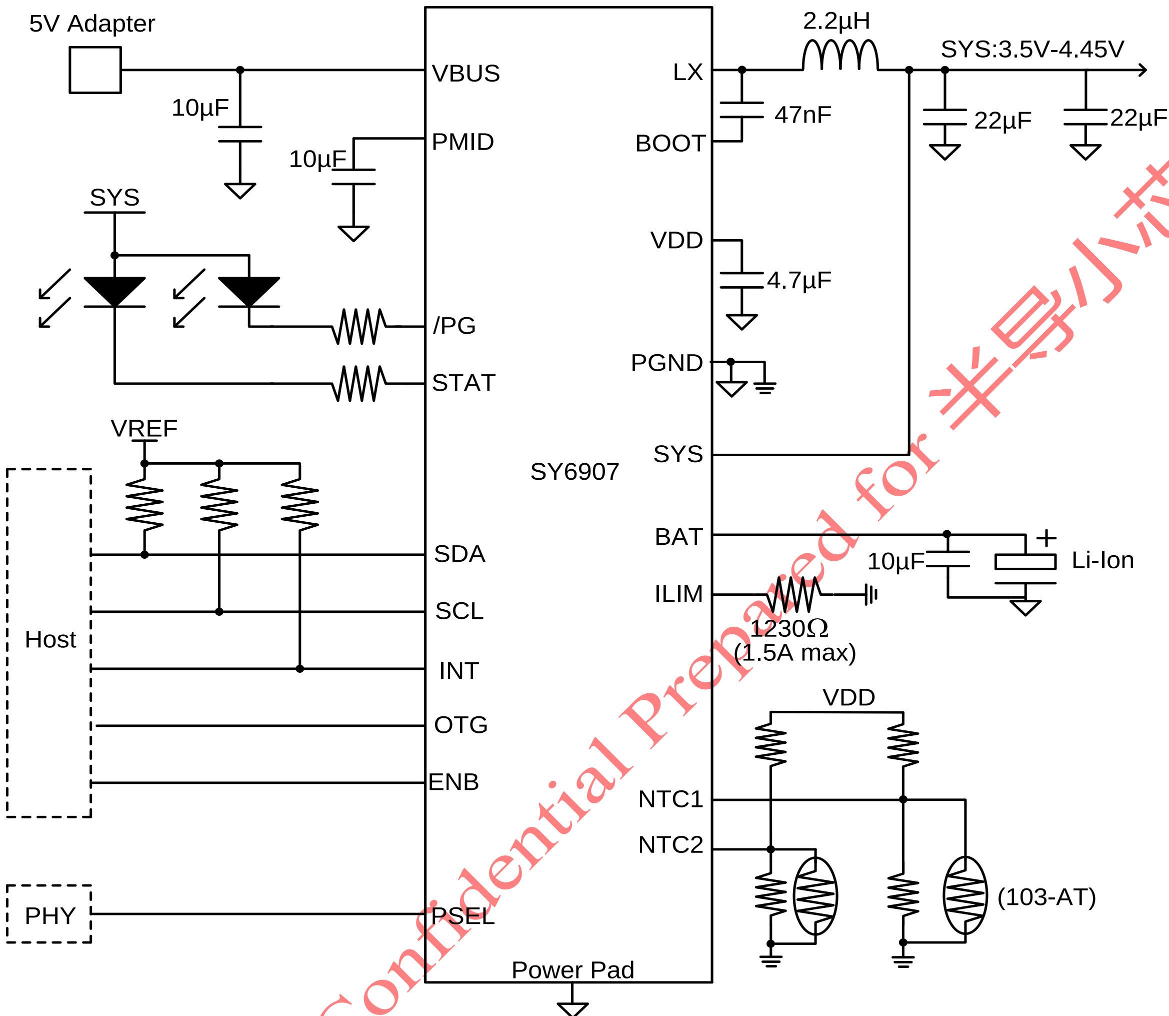
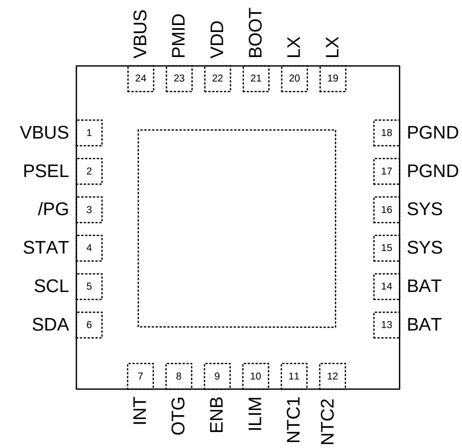


Figure1. Schematic Diagram

Pinout (top view)



(QFN4×4-24)

Top Mark: AQZ*xyz* (device code: **AQZ**, ***x=year code, y=week code, z= lot number code)***

Pin Name	**Pin Number**	**Pin Description**
VBUS	1,24	Charger input voltage. Place a 10μF ceramic capacitor from VBUS to PGND as close as possible to the IC.
PSEL	2	Power source selection input. Low indicates an adapter source. High indicates a USB host source
/PG	3	Open-drain active low power good indicator.
STAT	4	Open-drain charge status output to indicate various charger operations.
SCL	5	I^2C interface clock. Connect SCL to the logic rail through a 10k resistor.
SDA	6	I^2C interface data. Connect SDA to the logic rail through a 10k resistor.
INT	7	Open-drain interrupt output.
OTG	8	USB current limit selection pin during Buck mode and active high enable pin during Boost mode
ENB	9	Active low charge enable pin. Battery charging will be enabled when REG01[5:4]=01 and ENB pin =Low. ENB pin must be pulled high or low.
ILIM	10	ILIM pin sets the maximum input current, which is calculated as $I_{INMAX}=(1V/R_{ILIM}) \times 1845$. The actual input current limit is the lower one set by ILIM and I^2C REG00[2:0].
NTC1	11	Battery thermal protection pin #1. Connect a negative temperature coefficient thermistor. A resistor divider from VDD to NTC1 to GND can program the temperature window. Charge will suspend when either NTC pin is out of range. Recommend 103AT-2 thermistor.
NTC2	12	Temperature qualification voltage input #2. As NTC1.
BAT	13,14	Battery connection point to the positive terminal of the battery pack. Connect a 10 μF close to the BAT pin.
SYS	15,16	System connection point. The internal BATFET is connected between BAT and SYS.

PGND	17,18	Power ground.
LX	19,20	Switching node connected to the output inductor. Internally LX is connected to the source of the n-channel HSFET and the drain of the n-channel LSFET.
BOOT	21	Bootstrap capacitor connection for the HSFET gate driver. Connect the 0.047µF bootstrap capacitor from LX to BOOT.
VDD	22	Internal linear regulator output. Connect a 4.7µF (10V rating) ceramic capacitor from VDD to analog GND. The capacitor should be placed close to the IC. VDD also serves as a bias rail of NTC1 and NTC2 pins.
PMID	23	Connected to the drain of the reverse blocking MOSFET and the drain of HSFET. Place a ceramic capacitor at least 10µF from PMID to PGND.
Exposed pad	-	Exposed pad beneath the IC for heat dissipation.

Absolute Maximum Ratings (Note 1)

VBUS, PMID, STAT, /PG, LX -- -0.3V to +18V
BAT, SYS, SDA, SCL, INT, OTG, ILIM, VDD, NTC1, NTC2, ENB, PSEL, BST-LX ----------------- -0.3V to +6V
Package Thermal Resistance (Notes 2)
QFN4×4-24 θ_{JA} -- 33.3 ℃/W
QFN4×4-24 θ_{JC_TOP} -- 29.7 ℃/W
Junction Temperature Range --- -40℃ to +150℃
Operating Temperature Range --- -40℃ to +100℃
Storage Temperature -- -65℃ to +150℃
Lead Temperature (Soldering, 10s) -- +260℃

Recommended Operating Conditions (Note 3)

VBUS, PMID, STAT, /PG, LX -- -0.3V to +6V
BAT, SYS, SDA, SCL, INT, OTG, ILIM, VDD, NTC1, NTC2, ENB, PSEL, BST-LX ---------------- -0.3V to +5.5V
Junction Temperature Range --- -40℃ to +125℃
Ambient Temperature Range --- -40℃ to +85℃

Electrical Characteristics

(V_{VBUS}=5V, T_J = 25 ℃ for typical values, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Currents						
Battery Discharge Current	I_{BAT}	V_{VBUS} < V_{VBUS_UVLOZ}, V_{BAT} =4.2V, leakage between BAT and VBUS			5	µA
		High-Z mode, or no VBUS, BATFET disabled(REG07[5] = 1)		25		µA
		High-Z mode or no VBUS, REG07[5] = 0		55		µA
Input Supply Current (VBUS)	I_{VBUS}	V_{VBUS} = 5 V, High-Z mode		66		µA
		V_{VBUS} > V_{VBUS_UVLOZ}, V_{VBUS} > V_{BAT}, converter not switching		1.5	3	mA
		V_{VBUS} > V_{VBUS_UVLOZ}, V_{VBUS} >V_{BAT}, converter switching, V_{BAT} = 3.2V, I_{SYS} = 0A		4		mA
Battery Discharge Current in Boost Mode	$I_{OTGBOOST}$	V_{BAT} = 4.2V, Boost mode, I_{VBUS} = 0A, converter switching		4		mA
VBUS/BAT Power Up						
VBUS Operating Range	V_{VBUS_OP}		3.9		6	V
VBUS for Active I²C, No Battery	V_{VBUS_UVLOZ}	V_{VBUS} rising	3.1			V
Sleep Mode Falling Threshold	V_{SLEEP}	V_{VBUS} falling, V_{VBUS}-V_{BAT}	40	80	140	mV
Sleep Mode Rising Threshold	V_{SLEEPZ}	V_{VBUS} rising, V_{VBUS}-V_{BAT}	200	250	380	mV
VBUS Over Voltage Rising Threshold	V_{ACOV}	V_{VBUS} rising	6.35	6.65	6.95	V
VBUS Over Voltage Falling Hysteresis	V_{ACOV_HYST}	V_{VBUS} falling		100		mV
Battery for Active I²C, No VBUS	V_{BAT_UVLOZ}	V_{BAT} rising	2.35			V
Battery Depletion Threshold	V_{BAT_DPL}	V_{BAT} falling		2.4	2.7	V
Battery Depletion Rising Hysteresis	$V_{BAT\_DPL\_HYST}$	V_{BAT} rising		170		mV
Bad Adapter Detection Threshold	$V_{VBUSMIN}$	V_{VBUS} rising		3.8		V
Bad Adapter Detection Current Source	I_{BADSRC}			30		mA
Bad Source Detection Duration	t_{BADSRC}			30		ms

Power Path Management						
System Regulation Voltage	V_{SYS_RANGE}	I_{SYS} = 0A, Q4 off, V_{BAT} = 4.2V, REG01[3:1]=101, V_{SYSMIN} = 3.5V		4.35		V
System Voltage Output	V_{SYS_MIN}	REG01[3:1]=101, V_{SYSMIN} = 3.5V	3.54	3.65		V
Internal Top Reverse Blocking MOSFET ON Resistance	$R_{ON(RBFET)}$	Measured between VBUS and PMID	29	43	55	mΩ
Internal Top Switching MOSFET ON Resistance Between PMID and LX	$R_{ON(HSFET)}$		40	60	72	mΩ
Internal Bottom Switching MOSFET ON Resistance Between LX and PGND	$R_{ON(LSFET)}$		30	60	65	mΩ
Battery Good Comparator Rising Threshold	V_{BATGD}	V_{BAT} rising	3.3	3.45	3.6	V
Battery Good Comparator Falling Threshold	V_{BATGD_HYST}	V_{BAT} falling		100		mV
Battery Charger						
Charge Voltage Regulation Accuracy	$V_{BAT\_REG\_ACC}$	V_{BAT} = 4.208V	-1%		1%	
Fast Charge Current Regulation Accuracy	$I_{ICHG\_REG\_ACC}$	V_{BAT} = 3.8V, V_{SYSMIN} = 3.5V, I_{CHG} = 1792mA	-10%		10%	
Charge Current with 20% Option ON	I_{CHG_20pct}	V_{BAT} = 3.1V, REG02=01	50	120	190	mA
Battery LOWV Falling Threshold	$V_{BATLOWV}$	Fast charge to trickle charge, REG04[1] = 1	2.7	2.8	2.95	V
Battery LOWV Rising Threshold	$V_{BATLOWV\_HYST}$	Trickle to fast charge, REG04[1] = 1	2.8	3.0	3.1	V
Trickle Charge Current Regulation Accuracy	I_{TC_ACC}	V_{BAT} = 2.6V, I_{TC} = 256mA	-55%		55%	
Termination Current Accuracy	I_{TERM_ACC}	I_{TERM} = 256mA, I_{CHG} = 960mA	-40%		50%	
Battery Short Voltage	V_{SHORT}	V_{BAT} falling		1.8		V
Battery Short Voltage Hysteresis	V_{SHORT_HYST}	V_{BAT} rising		200		mV
Battery Short Current	I_{SHORT}	V_{BAT}<V_{SHORT}		100		mA
Recharge Threshold Below V_{BAT_REG}	V_{RECHG}	V_{BAT} falling, REG04[0] = 0		100		mV
Recharge Deglitch Time	t_{RECHG}	V_{BAT} falling, REG04[0]=0		100		ms
SYS-BAT MOSFET ON Resistance	R_{ON_BATFET}		15	36	38	mΩ

Input Voltage/Current Regulation						
Input Voltage Regulation Accuracy	$V_{INDPM\_REG\_ACC}$	V_{INDPM} = 4.36V	-2%		2%	
USB Input Current Regulation Limit, V_{BUS} =5V, Current Pulled from LX	I_{USB_DPM}	USB100	55		100	
		USB500	300		500	
		USB900	750		900	
Input Current Limit During System Start UP	I_{IN_START}	V_{SYS}<2.2V		100		mA
I_{IN} = K_{ILIM}/R_{ILIM}	K_{ILIM}	I_{INDPM} = 1.5A	1490	1845	2080	A x Ω
BAT Over-Voltage Protection						
Battery Over-Voltage Threshold	V_{BATOVP}	V_{BAT} rising, as percentage of V_{BAT_REG}		104%		
Battery Over-Voltage Hysteresis	V_{BATOVP_HYST}	V_{BAT} falling, as percentage of V_{BAT_REG}		2%		
Battery Over-Voltage Deglitch Time to Disable Charge	t_{BATOVP}			1		µs
Thermal Regulation and Thermal Shutdown						
Junction Temperature Regulation Accuracy	$T_{Junction\_REG}$	REG06[1:0] = 11		120		℃
Thermal Shutdown Rising Temperature	T_{SHUT}	Temperature rising		160		℃
Thermal Shutdown Hysteresis	T_{SHUT_HYST}			30		℃
Cold/Hot Thermistor Comparator						
Cold Temperature Threshold, NTC Pin Voltage Rising Threshold	V_{LTF}	Charger suspends charge. as percentage to V_{VDD}	73	73.5	74	%
Cold Temperature Hysteresis, NTC Pin Voltage Falling	V_{LTF_HYST}	As percentage to V_{VDD}		0.56		%
Hot Temperature Threshold, NTC Pin Voltage Falling Threshold	V_{HTF}	As percentage to V_{VDD}	44.2	44.6	45	%
Hot Temperature Hysteresis, NTC Pin Voltage Rising Threshold	V_{HTF_HYST}	As percentage to V_{VDD}		2.5		%
Deglitch Time for Temperature Out of Range Detection		$V_{NTC} > V_{LTF}$, or $V_{NTC} < V_{HTF}$		10		ms
Charge Over-Current Comparator						
HSFET Over Current Threshold	I_{HSFET_OCP}		3	5		A
System Over Load Threshold	I_{BATFET_OCP}		5			A

PWM Operation						
PWM Switching Frequency, and Digital Clock	F_{LX}		1300	1500	1700	kHz
Maximum PWM Duty Cycle	D_{MAX}			93%		
Bootstrap Refresh Comparator Threshold	$V_{BOOT\_REFRESH}$	V_{BOOT}-V_{LX} when LSFET refresh pulse is requested, V_{BUS}=5V		3.25		V
Boost Mode Operation						
OTG Output Voltage	V_{OTG_REG}	I_{VBUS} = 0		5.05		V
OTG Output Voltage Accuracy	$V_{OTG\_REG\_ACC}$	I_{VBUS} = 0	-2%		2%	
OTG Over-Voltage Threshold	V_{OTG_OVP}			5.3	5.6	V
LSFET Cycle-by-Cycle Current Limit	V_{OTG_ILIM}		1.3	2.2		A
RBFET Over-Current Threshold	I_{RBFET_OCP}	REG01[0] = 1	1.2	1.8		A
		REG01[0] = 0		2.3		
VDD LDO						
VDD LDO Output Voltage	V_{VBUS}	V_{VBUS} = 6V, I_{VDD} = 20mA		5.1		V
VDD LDO Current Limit	I_{VDD}	V_{VBUS} = 6V, V_{VDD} = 3.8V	50			mA
Logic I/O Pin Characteristics (OTG, ENB, PSEL, STAT, /PG)						
Input Low Threshold	V_{ILO}				0.4	V
Input High Threshold	V_{IH}		1.3			V
Output Low Saturation Voltage	V_{OUT_LO}	Sink current = 5mA			0.4	V
High Level Leakage Current	I_{BIAS}	Pull up rail 1.8V			1	μA
I^2C Interface (SDA, SCL, INT)						
Input High Threshold Level	V_{IH}	VPULL-UP = 1.8V, SDA and SCL	1.3			V
Input Low Threshold Level	V_{IL}	VPULL-UP = 1.8V, SDA and SCL			0.4	V
Output Low Threshold Level	V_{OL}	Sink current = 5mA			0.4	V
High-Level Leakage Current	I_{BIAS}	VPULL-UP = 1.8V, SDA and SCL			1	μA
SCL Clock Frequency	F_{SCL}				400	kHz
Watchdog Timer						
REG05[5:4]=11	t_{WDT}	VDD LDO enabled	100	160		s

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

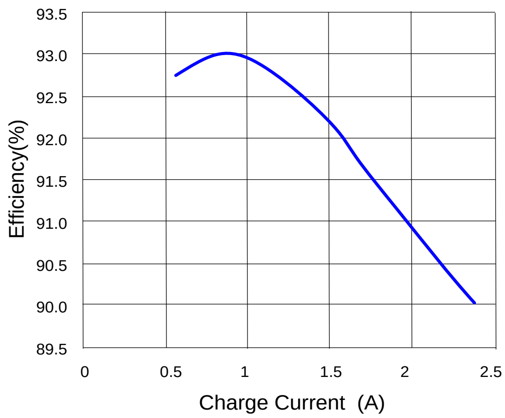
Note 2: θ_{JA} is measured in the natural convection at T_A = 25℃ on a low effective four-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

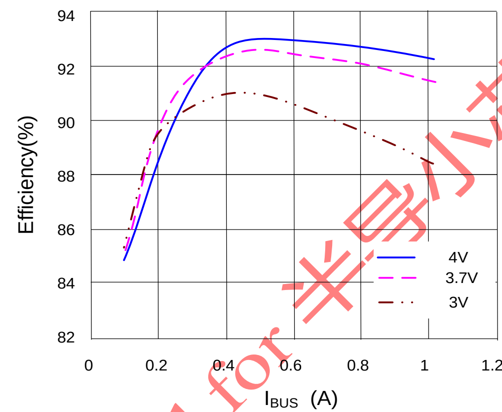
Typical Performance Characteristics

T_A=25 ℃, V_{IN}=5V, single-cell battery, unless otherwise specified.

Efficiency vs. Charge Current (CV Mode)

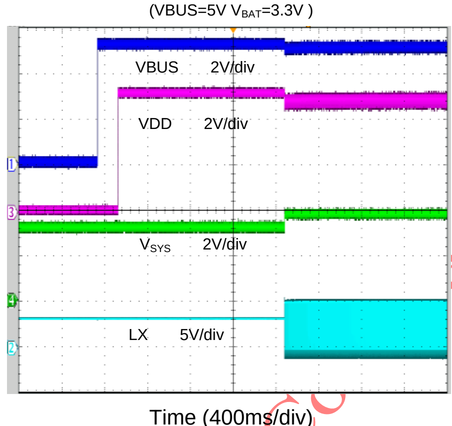


Efficiency vs. I_{BUS} (Boost Mode)



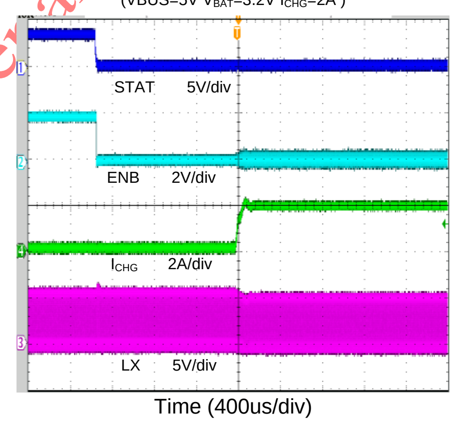
Power ON

(VBUS=5V V_{BAT}=3.3V)



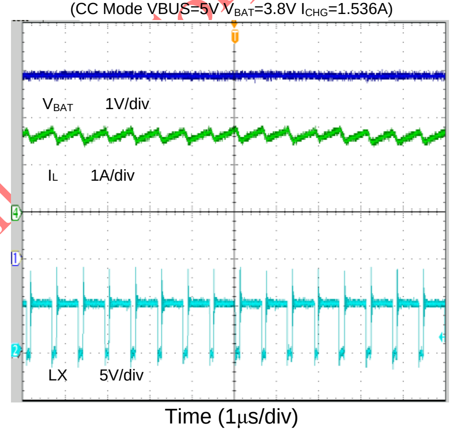
ENB ON

(VBUS=5V V_{BAT}=3.2V I_{CHG}=2A)



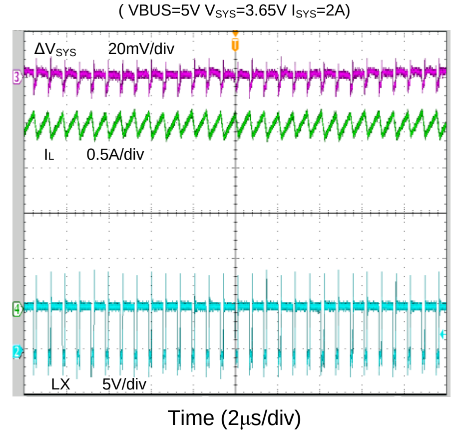
Constant Current Charge State

(CC Mode VBUS=5V V_{BAT}=3.8V I_{CHG}=1.536A)



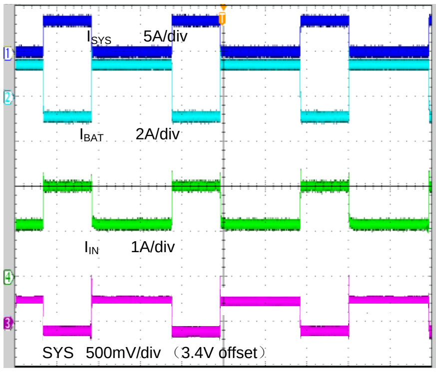
SYS State

(VBUS=5V V_{SYS}=3.65V I_{SYS}=2A)



SYS Load Transient

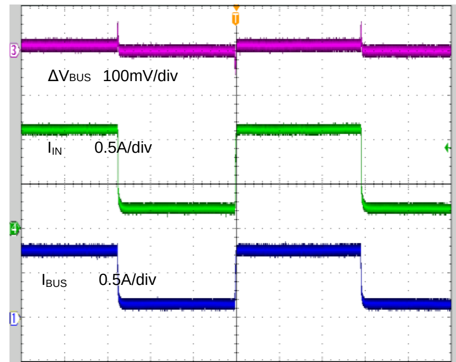
(V_{BUS}=5V V_{BAT}=3.2V I_{IN_LIMIT}=1.5A)



Time (10ms/div)

Boost Mode Load Transient

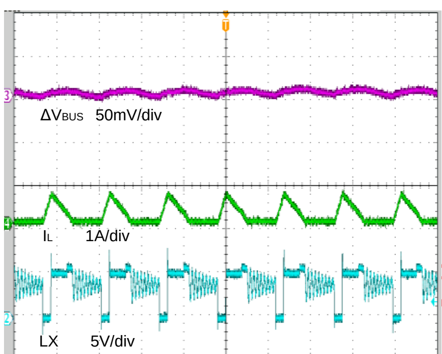
(V_{BAT}=3.8V)



Time (4ms/div)

Boost Mode State

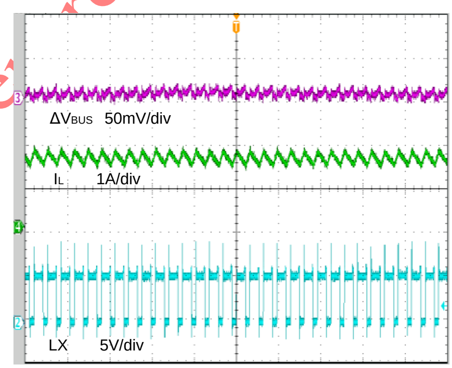
（V_{BAT}=3.6V I_{BUS}=0.1A）



Time (2µs/div)

Boost Mode State

(V_{BAT}=3.7V I_{BUS}=1A)



Time (2µs/div)

I^2CRegisters

Address: 6BH. REG00-07 support Read and Write. REG08-0A are Read only.

Input Source Control Register REG00 (default 00110000, or 30)

Bit		**Description**	**Note**
Bit 7	EN_HIZ	0 – Disable,1 – Enable	Default: Disable (0)
Input Voltage Limit			
Bit 6	VINDPM[3]	640mV	Offset: 3.88V, Range: 3.88V-5.08V Default: 4.36V (0110)
Bit 5	VINDPM[2]	320mV	
Bit 4	VINDPM[1]	160mV	
Bit 3	VINDPM[0]	80mV	
Input Current Limit(Actual input current limit is the lower of I^2C and ILIM)			
Bit 2	IINLIM[2]	000-0.1A,001-0.15A,010-0.5A,011-0.9A,100-1A,101-1.5A,110-2A,111-3A	Default :0.1A (000) (PSEL=1，OTG =0) or 0.5A (010) (PSEL=1,OTG=1) or 3A (PSEL=0)
Bit 1	IINLIM[1]		
Bit 0	IINLIM[0]		

Power-ON Configuration Register REG01 (default 00011011, or 1B)

Bit		**Description**	**Note**
Bit 7	Register Reset	0 – Keep current register setting, 1 – Reset to default	Default: Keep current register setting (0) Back to 0 after register reset
Bit 6	I^2C Watchdog Timer Reset	0 – Normal; 1 – Reset	Default: Normal (0) Back to 0 after timer reset
Charger Configuration			
Bit 5	CHG_CONFIG[1]	00 – Charge Disable, 01 – Charge Battery, 10/11 – OTG	Default: Charge Battery (01)
Bit 4	CHG_CONFIG[0]		
Minimum System Voltage Limit			
Bit 3	SYS_MIN[2]	0.4V	Offset: 3.0V, Range 3.0V-3.7V Default: 3.5V (101)
Bit 2	SYS_MIN[1]	0.2V	
Bit 1	SYS_MIN[0]	0.1V	
Boost Mode Current Limit			
Bit 0	BOOST_LIM	0 – About 500mA, 1 – About 1A	Default: About 1A (1)

Charge Current Control Register REG02 (default 01100000, or 60)

Bit		**Description**	**Note**
Fast Charge Current Limit			
Bit 7	ICHG[5]	2048mA	Offset: 512mA Range: 512-2496mA Default:2048mA (011000)
Bit 6	ICHG[4]	1024mA	
Bit 5	ICHG[3]	512mA	
Bit 4	ICHG[2]	256mA	
Bit 3	ICHG[1]	128mA	
Bit 2	ICHG[0]	64mA	
Bit 1	Reserved	0-Reserved	
Bit 0	FORCE_20PCT	0 – ICHG as REG02[7:2] programmed 1 – ICHG as 20% of REG02[7:2] programmed	Default: ICHG as REG02[7:2] programmed (0)

Trickle/Termination Current Control Register REG03 (default 00010001, or 11)

Bit		**Description**	**Note**
Trickle Charge Current Limit			
Bit 7	ITC[3]	1024mA	Offset: 128mA Range: 128mA–2048mA Default: 256mA (0001)
Bit 6	ITC[2]	512mA	
Bit 5	ITC[1]	256mA	
Bit 4	ITC[0]	128mA	
Termination Current Limit			
Bit 3	ITERM[3]	1024mA	Offset: 128mA Range: 128mA–2048mA Default: 256mA (0001)
Bit 2	ITERM[2]	512mA	
Bit 1	ITERM[1]	256mA	
Bit 0	ITERM[0]	128mA	

Charge Voltage Control Register REG04 (default 10110010, or B2)

Bit		**Description**	**Note**
Charge Voltage Limit			
Bit 7	VREG[5]	512mV	Offset: 3.504V Range: 3.504V–4.400V (111000) Default: 4.208V (101100)
Bit 6	VREG[4]	256mV	
Bit 5	VREG[3]	128mV	
Bit 4	VREG[2]	64mV	
Bit 3	VREG[1]	32mV	
Bit 2	VREG[0]	16mV	
Battery Trickle to Fast Charge Threshold			
Bit 1	BATLOWV	0 – 2.8V,1 – 3.0V	Default: 3.0V (1)
Battery Recharge Threshold (below battery regulation voltage)			
Bit 0	VRECHG	0 – 100mV,1 – 300mV	Default: 100mV (0)

Charge Termination/Timer Control Register REG05 (default 10011010, or 9A)

Bit		**Description**	**Note**
Charging Termination Enable			
Bit 7	EN_TERM	0 – Disable, 1 – Enable	Default: Enable termination (1)
Termination Indicator Threshold			
Bit 6	TERM_STAT	0 – Match ITERM, 1 – STAT pin high before actual termination when charge current below 800mA	Default: Match ITERM(0)
I^{2}C Watchdog Timer Setting			
Bit 5	WATCHDOG[1]	00 – Disable timer, 01 – 40s, 10 – 80s, 11 – 160s	Default: 40s(01)
Bit 4	WATCHDOG[0]		
Charging Safety Timer Enable			
Bit 3	EN_TIMER	0 – Disable,1 – Enable	Default: Enable (1)
Fast Charge Timer Setting			
Bit 2	CHG_TIMER[1]	00 – 5 hrs, 01– 8 hrs, 10 – 12 hrs, 11 – 20 hrs	Default: 8 hours (01) (See Charging Safety Timer for details)
Bit 1	CHG_TIMER[0]		
Bit 0	Reserved	0-Reserved	

Thermal Regulation Control Register REG06 (default 00000011, or 03)

Bit		**Description**	**Note**
Bit 7	Reserved	0 - Reserved	
Bit 6	Reserved	0 - Reserved	
Bit 5	Reserved	0 - Reserved	
Bit 4	Reserved	0 - Reserved	
Bit 3	Reserved	0 - Reserved	
Bit 2	Reserved	0 - Reserved	
Thermal Regulation Threshold			
Bit 1	TREG[1]	00 – 60 ℃, 01 – 80 ℃, 10 – 100 ℃, 11 – 120 ℃	Default: 120 ℃ (11)
Bit 0	TREG[0]		

Misc Operation Control Register REG07 (default 01001011, or 4B)

Bit		**Description**	**Note**
Bit 7	Reserved	0 – Reserved	
Safety Timer Setting during Input DPM and Thermal Regulation			
Bit 6	TMR2X_EN	0 – Safety timer not slowed by 2X during input DPM or thermal regulation, 1 – Safety timer slowed by 2X during input DPM or thermal regulation	Default: Safety timer slowed by 2X (1)
Force BATFET Off			
Bit 5	BATFET_Disable	0 – Allow Q4 turn on, 1 – Turn off Q4	Default: Allow Q4 turn on(0)
Bit 4	Reserved	0 - Reserved	
Bit 3	Reserved	1 - Reserved	
Bit 2	Reserved	0 - Reserved	

Bit 1	INT_MASK[1]	0 – No INT during CHRG_FAULT, 1 – INT on CHRG_FAULT	Default: INT on CHRG_FAULT (1)
Bit 0	INT_MASK[0]	0 – No INT during BAT_FAULT, 1 – INT on BAT_FAULT	Default: INT on BAT_FAULT (1)

System Status Register REG08

Bit		Description
Bit 7	VBUS_STAT[1]	00 – Unknown (no input), 01 – USB host, 10 – Adapter port, 11 – OTG
Bit 6	VBUS_STAT[0]	
Bit 5	CHRG_STAT[1]	00 – Not Charging, 01 – Trickle (<$V_{BATLOWV}$),10 – Fast Charging, 11 – Charge Termination Done
Bit 4	CHRG_STAT[0]	
Bit 3	DPM_STAT	0 – Not DPM, 1 – VINDPM or IINDPM
Bit 2	PG_STAT	0 – Not power good, 1 – power good
Bit 1	THERM_STAT	0 – Normal, 1 – In thermal regulation
Bit 0	VSYS_STAT	0 – Not in VSYSMIN regulation ($V_{BAT}>V_{SYSMIN}$), 1 – in VSYSMIN regulation ($V_{BAT}<V_{SYSMIN}$)

Fault Register REG09

Bit		Description
Bit 7	WATCHDOG_FAULT	0 – Normal,1 - Watchdog timer expiration
Bit 6	OTG_FAULT	0 – Normal,1 – Boost mode OCP or BUS OVP
Bit 5	CHRG_FAULT[1]	00 – Normal, 01 – input fault (VBUS OVP or V_{BAT}<VBUS<3.8V), 10 - Thermal shutdown, 11 – Charge Safety Timer Expiration
Bit 4	CHRG_FAULT[0]	
Bit 3	BAT_FAULT	0 – Normal,1 – BATOVP
Bit 2	NTC_FAULT[2]	000 – Normal,101 – Cold,110 – Hot
Bit 1	NTC_FAULT[1]	
Bit 0	NTC_FAULT[0]	

Vender / Part / Revision Status Register REG0A

Bit		Description
Bit 7	Reserved	0 - Reserved
Bit 6	Reserved	0 - Reserved
Device Configuration		
Bit 5	PN[2]	101
Bit 4	PN[1]	
Bit 3	PN[0]	
Bit 2	NTC_PROFILE	0 - Cold/Hot window
Bit 1	DEV_REG[0]	11
Bit 0	DEV_REG[1]	

General Function Description

SY6907 is a fully-integrated switching battery charger with system power path management devices for single cell Li-Ion and Li-polymer battery in a wide range of tablets and other portable devices. It integrates the input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and BATFET (Q4) between system and battery. The extremely low R_{DSON} achieves very high conversion efficiency up to 2.5A charging current.

1. POR

The internal bias circuits are powered from the higher voltage between VBUS and BAT. When VBUS or V_{BAT} rises above UVLOZ, the sleep comparator, battery depletion comparator and BATFET driver are active. I^2C interface is ready for communication and all the registers are reset to default value. The host can access all the registers after POR (power-on-reset).

2. Battery Power UP without DC Source

Only if the battery is present and the voltage is above depletion threshold (V_{BAT_DPL}), the BATFET will turn on and provide power to system. The device will stay in HIZ mode and the VDD LDO will stay off to minimize the quiescent current. The device always monitors the discharge current through BATFET. When the system is overloaded or shorted, the device will immediately turn off BATFET and latch off until the input source plugs in again.

3. DC Source Power UP

When the DC source plugs in, SY6907 will check the input source voltage to turn on VDD LDO and all the bias circuits. It will also check the input current limit before starting the Buck converter.

4. Input Source Qualification

After VDD LDO powers up, SY6907 checks the current capability of the input source. The input source capability is qualified by the internal active detection circuit with the pulled down current source.

1. VBUS voltage below 6.4V (not in ACOV)

2. VBUS voltage above 3.8V when pulling 30mA during 30ms (poor source detection)

Once the input source passes all the conditions above, the status register REG08[2] will go high and the /PG pin will go low. An INT is asserted to the host.

If the device fails the poor source detection, it will repeat the detection every 2 seconds.

5. Input Current Limit Detection

The USB ports on personal computers are convenient charging sources for portable devices (PDs). If the portable device is attached to a USB host SDP, the USB specification will require the portable device to draw limited current (100mA/500mA in USB 2.0, and 150mA/900mA in USB 3.0). If the portable device is attached to a charging port, it will be allowed to draw up to 3A.

After the /PG is LOW or REG08[2] goes HIGH, the charger device will always run input current limit detection when a DC source plugs in unless the charger is in HIZ during the host mode.

SY6907 can set input current limit through PSEL and OTG pins. After the input current limit detection is done, the host can write REG00[2:0] to change the input current limit.

PSEL/OTG Pins Set Input Current Limit

The SY6907 has PSEL, it will directly take the USB PHY device output to decide whether the input is the USB host or charging port.

Table 1. SY6907 Input Current Limit Detection

PSEL	OTG	INPUT CURRENT LIMIT	REG08[7:6]
HIGH	LOW	100 mA	01
HIGH	HIGH	500 mA	01
LOW	/	3A	10

HIZ State with 100mA USB Host

In battery charging spec, the good battery threshold is the minimum charge level of the battery to power up the portable device successfully. When the input source is a 100mA USB host, and the battery is above bat-good threshold (V_{BATGD}), the device will follow the battery charging spec and enter high impedance state (HIZ), and REG08[7:6](VBUS_STAT) will keep 00. In HIZ state, the device is in the lowest quiescent state with VDD LDO and the bias circuits off. The charger device sets REG00[7] to 1, and the VBUS current during HIZ state will be small. The system is supplied by the battery. The safety timer for the charging with 100mA USB port is about 45min. When the time is up, the device will enter HIZ mode.

Once the charger device enters HIZ state in the host mode, it will stay in HIZ until the host writes

REG00[7]=0. When the processor host wakes up, it is recommended to firstly check if the charger is in HIZ state.

In default mode, the charger will reset REG00[7] back to 0 when the input source is removed. When another source plugs in, the charger will run detection again, and update the input current limit.

6. Converter Power-UP

After the input current limit is set, the converter will be enabled and the HSFET and LSFET will start switching. If the battery charging is disabled, the BATFET turns off. Otherwise, the BATFET will stay on to charge the battery.

SY6907 provides soft-start when ramping up the system rail. When the system rail is below 2.2V, the input current limit is forced to 100mA. After the system rises above 2.2V, the charger device will set the input current limit set by the lower value between register and ILIM pin.

As a battery charger, SY6907 deploys a 1.5MHz step down switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of the input voltage, the battery voltage, the charge current and the temperature, which simplifies the output filter design.

The internal compensation network allows to minimize the peripheral circuit design.

In order to improve light load efficiency, the device will switch to PFM control at light load when the battery is below the minimum system voltage setting or charging is disabled. During the PFM operation, the switching duty cycle is set by the ratio of SYS and VBUS.

7. Boost Mode Operation

SY6907 supports Boost converter operation to deliver power from the battery to other portable devices through USB port. The Boost mode output current rating meets the USB on-the-go 500mA output requirement. The maximum output current is about 1A.

In Boost mode, SY6907 employs a 1.5MHz step-up switching regulator. Similar to Buck operation, the device switches from PWM operation to PFM operation at light load to improve efficiency.

During Boost mode, the status register REG08[7:6] is set to 11, the VBUS output is 5V and the output current can reach up to about 500mA or about 1A, selected via the I^{2}C (REG01[0]).

Any fault during Boost operation, including VBUS over-voltage or over-current, sets the fault register REG09[6] to 1 and an INT is asserted.

8. Power Path Management

SY6907 accommodates a wide range of input sources from USB, adapter, to car battery. The device provides automatic power path selection to supply the system (SYS) from the input source (VBUS), the battery (BAT), or both.

Narrow VDC Architecture

The device deploys the narrow VDC architecture (NVDC) with BATFET separating system from the battery. The minimum system voltage is set by REG01[3:1]. Even with a fully depleted battery the system is regulated above the minimum system voltage (default 3.5V).

When the battery is below the minimum system voltage, the BATFET will operate in linear mode (LDO mode) and the system will be 150mV higher than the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, the BATFET will be fully on. The voltage difference between the system and battery will be the VDS of BATFET.

When the battery charging is disabled or terminated, the system will be always regulated at 150mV above the higher voltage of the minimum system voltage setting and the battery voltage. The status register REG08[0] will go high when the system is in the minimum system voltage regulation.

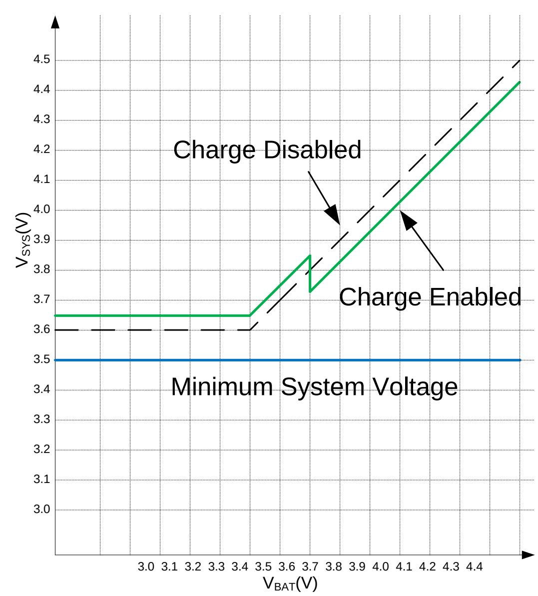


Figure 2. V_{SYS} vs. V_{BAT}

Dynamic Power Management

To meet the maximum current limit in USB spec and avoid over loading the adapter, SY6907 features dynamic power management (DPM) which continuously monitors the input current and the input voltage.

When the input source is over loaded, either the current exceeds the input current limit (REG00[2:0]) or the voltage falls below the input voltage limit (REG00[6:3]), the device will reduce the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero but the input source is still overloaded, the system voltage will start to drop. Once the system voltage falls below the battery voltage, the device will automatically enter the supplement mode where the BATFET turns on and the battery starts discharging so that the system will be supported from both the input source and the battery.

During DPM mode (either VINDPM or IINDPM), the status register REG08[3] will go high.

Supplement Mode

When the system voltage falls below the battery voltage, the battery will start to support the system load through the BATFET. In Buck mode, the BATFET will be latched off if the overload occurs or the system is shorted. In Boost mode, the BATFET will be latched off if the overload occurs. The BATFET can be turned off through the I²C directly.

9. Battery Charging Management

SY6907 charges 1-cell Li-Ion battery with up to 2.5A charge current for high capacity tablet battery. The 40mohm BATFET improves charging efficiency and minimizes the voltage drop during discharging.

Autonomous Charging Cycle

With battery charging enabled at POR (REG01[5:4]=01), SY6907 can complete a charging cycle without host involvement. The device default charging parameters are listed in.

Table 2. Charging Parameter Default Setting

Default Mode	SY6907
Charging Voltage	4.208V
Charging Current	2.048 A
Trickle Current	256 mA
Termination Current	256 mA
Temperature Profile	Hot/Cold
Safety Timer	8.0 hours

A new charge cycle will start when the following conditions are valid:

- The converter starts.
- Battery charging is enabled by the I²C register bit (REG01[5:4]) = 01 and ENB is low.
- No thermistor fault on NTC1 or NTC2.
- No safety timer fault.
- BATFET is not forced to be turned off (REG07[5]).

The charger device will automatically terminate the charging cycle when the charging current is below the termination threshold and the charge voltage is above recharge threshold. When a full battery voltage is discharged below the recharge threshold (REG04[0]), SY6907 will automatically start another charging cycle.

The status register REG08[5:4] indicates the different charging phases: 00-charging disable, 01-trickle, 10-fast charge (constant current) and constant voltage mode, 11-charging done. Once a charging cycle is completed, an INT will be asserted to notify the host.

The host can always control the charging operation and optimize the charging parameters by writing to the registers through the I²C.

Battery Charging Profile

The device charges the battery in three phases: trickle current, constant current and constant voltage. At the beginning of a charging cycle, the device checks the battery voltage and applies current.

Table 3. Charging Current Setting

V_{BAT}	Charging Current	Reg Default Setting	REG08[5:4]
<2V	100mA	/	01
2V-3V	REG03[7:4]	256mA	01
>3V	REG02[7:2]	2048mA	10

If the charger device is in DPM regulation or thermal regulation during charging, the actual charging current will be less than the programmed value. In this case, the termination is temporarily disabled and the charging safety timer is counted at half of the clock rate.

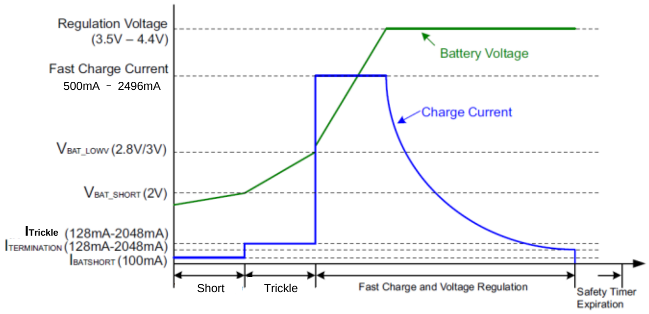


Figure 3. Battery Charging Profile

10. Thermistor Cold/Hot Temperature Window

SY6907 continuously monitors the battery temperature by measuring the voltage between the NTC pins and the ground, typically determined by a negative temperature coefficient thermistor and an external voltage divider. The device compares this voltage against its internal thresholds to determine if charging is allowed. During the charge cycle, the battery temperature must be within the V_{LTF} to V_{HTF} thresholds, or else the device will suspend charging.

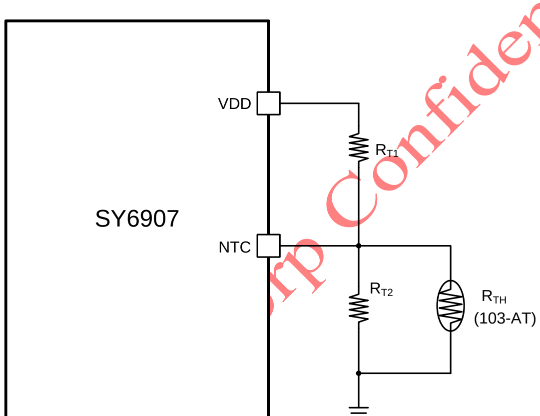


Figure4. NTC Resistor Network

When the NTC fault occurs, the fault register REG09[2:0] will indicate the actual condition on each NTC pin and an INT will be asserted to the host. The STAT pin will indicate the fault when charging is suspended.

11. Charging Termination

SY6907 will terminate a charge cycle when the battery voltage is above the recharge threshold, and the current is below termination current. After the charging cycle is completed, the BATFET will be turned off. The converter will keep running to power the system, and the BATFET can turn back on to be in supplement mode.

When termination occurs, the status register REG08[5:4] will be 11, and an INT will be asserted to the host. Termination will be temporarily disabled if the charger device is in the input current/voltage regulation or the thermal regulation. Termination can be disabled by writing 0 to REG05[7].

Termination when REG02[0] = 1

When REG02[0] is HIGH to reduce the charging current by 80%, the charging current will be less than the termination current. The charger device termination function will be disabled. When the battery is charged to fully capacity, the host will be disabled charging through ENB pin or REG01[5:4].

Termination when REG05[6] = 1

Usually the STAT bit will indicate charging completed when the charging current falls below the termination threshold. Write REG05[6]=1 to enable an early "charge done" indication on STAT pin. The STAT pin will go high when the charge current reduces below 800mA. The charging cycle will be still on-going until the current falls below the termination threshold.

12. Charging Safety Timer

SY6907 has a safety timer to prevent extended charging cycle due to abnormal battery conditions.

In default mode, the device keeps charging the battery with 5-hour fast charging safety timer regardless of REG05[2:1] default value. At the end of the 5 hours, the EN_HIZ (REG00[7]) is set to signal the Buck converter stopping, and the system load will be supplied by the battery. The EN_HIZ bit can be cleared to restart the Buck converter.

In host mode, the device will keep charging the battery until the fast charging safety timer expired. The duration of the safety timer can be set by the REG05[2:1] bits (default = 8 hours). At the end of the safety timer, Q4 is turned off and the Buck converter continues to operate to supply system load, the fault register REG09[5:4] goes to 11 and an INT is asserted to the host. The safety timer is 1 hour when the battery is below BATLOWV threshold.

The safety timer feature can be disabled via the I^2C (REG05[3]).

During the input voltage, the current regulation or the thermal regulation, the safety timer counts at half of the clock rate since the actual charge current is likely to be below the register setting. For example, if the charger is in the input current regulation (IINDPM) throughout the whole charging cycle, and the safety time is set to 5 hours, the safety timer will expire in 10 hours. This feature can be disabled by writing 0 to REG07[6].

13. Host Mode and Default Mode

SY6907 is a host controlled device, but it can operate in default mode without host management. In default mode, SY6907 can be used as an autonomous charger with no host or with host in sleep.

When the charger is in default mode, REG09[7] is HIGH. When the charger is in host mode, REG09[7] is LOW. After power-on-reset, the device will start in watchdog timer expiration state, or default mode. All the registers will be in the default settings.

Any written command to SY6907 transits the device from default mode to host mode. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to REG01[6] before the watchdog timer expiring (REG05[5:4]), or disabling the watchdog timer by setting REG05[5:4]=00.

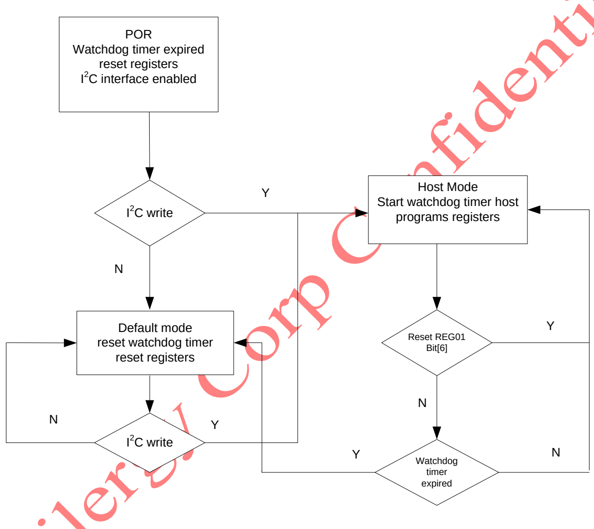


Figure5. Watchdog Timer Flow Chart

14. Status Outputs （/PG, STAT and INT)

Power Good Indicator (/PG)

In SY6907, /PG goes LOW to indicate a good input source.

Charging Status Indicator (STAT)

SY6907 indicates charging state on the open-drain STAT pin. The STAT pin can drive LED as the application diagram shows.

Table 4. STAT Pin State

Charging State	STAT
Charging in progress (including recharge)	LOW
Charging complete	HIGH
Sleep mode, charge disable	HIGH
Charge suspend (input over-voltage, NTC fault, timer fault, input or system over- voltage)	blinking at 1Hz

Interrupt to Host (INT)

In some applications, the host does not always monitor the charger operation. The INT notifies the system on the device operation. The following events will generate 256us INT pulse.

- USB/adapter source identified (through PSEL and OTG pins)
- Good input source detected
- Input removed or ACOV
- Charge Complete
- Any fault event in REG09

When a fault occurs, the charger device will send out INT and latch the fault state in REG09 until the host reads the fault register. Before the host reading REG09, the charger device will not send any INT upon new faults except NTC fault (REG09[2:0]). The NTC fault is not latched and always reports the current thermistor conditions. In order to read the current fault status, the host has to read REG09 two times consecutively. The 1st reads fault register status from the last INT and the 2nd reads the current fault register status.

15. BATFET Control Principle

During the normal mode, the BATFET is always on for the battery charging and discharging. It can be forced off by the host through the I²C REG07[5]. To force off BATFET in OTG mode, OTG mode should be disabled first (by REG01[5:4]). This bit allows the user to turn off the BATFET when the battery condition becomes abnormal during charging. When the BATFET is off, there will be no path to charge or discharge the battery. Besides I²C control, when the switching converter is in HIZ mode, the BATFET will be off if the discharging overload occurs; when the switching converter operates in Buck mode, the BATFET will be latched off if the SYS short is detected or the discharging overload occurs; when the switching converter operates in OTG mode, the BATFET will be latched off if the overload occurs.

Shipping Mode

When the end equipment is assembled, the system is connected to the battery through the BATFET. There will be a small leakage current to discharge the battery even when the system is powered off. In order to extend the battery life during shipping and storage, the device can turn off the BATFET so that the system voltage will be zero to minimize the leakage.

In order to keep the BATFET off during the shipping mode, the host has to disable the watchdog timer (REG05[5:4]=00) and disable the BATFET (REG07[5]=1) at the same time.

Once the BATFET is disabled, the BATFET can be turned on by plugging in the adapter.

16. Protections

Input Current Limit on ILIM

For safe operation, SY6907 has an additional hardware pin on ILIM to limit maximum input current on ILIM pin. The input maximum current is set by a resistor from ILIM pin to the ground as:

$$I_{INMAX} = \frac{1V}{R_{ILIM}} \times 1845 \quad (1)$$

The actual input current limit is the lower value between the ILIM setting and the register setting (REG00[2:0]). For example, if the register setting is 111 for 3A, and the ILIM has a 1230Ω resistor to the ground for 1.5A, the input current limit is 1.5A. The ILIM pin can be used for setting the input current limit rather than the register settings.

The device regulates the ILIM pin at 1V. If the ILIM voltage exceeds 1V, the device will enter the input current regulation .

The voltage on ILIM pin is proportional to the input current. The ILIM pin can be used for monitoring the input current following equation (2):

$$I_{IN} = \frac{V_{ILIM}}{1V} \times I_{INMAX} \quad (2)$$

For example, if the ILIM sets 2A by the ILIM pin, and the ILIM pin voltage is 0.6V, the actual input current is 1.2A. If the ILIM pin is open, the input current will be limited to zero since ILIM voltage floats above 1V. If ILIM pin is short, the input current limit will be set by the register.

Thermal Regulation and Thermal Shutdown

SY6907 monitors the internal junction temperature T_J to avoid overheating the chip and limit the IC surface temperature. When the internal junction temperature exceeds the preset limit (REG06[1:0]), the device will lower down the charge current. The wide thermal regulation which ranges from 60℃ to 120℃ allows the user to optimize the system thermal performance.

During the thermal regulation, the actual charging current is usually below the programmed battery charging current. Therefore, the termination is disabled, the safety timer runs at half of the clock rate, and the status register REG08[1] goes high.

Additionally, the device has a thermal shutdown to turn off the converter. The fault register REG09[5:4] is 10 and an INT is asserted to the host.

Voltage and Current Monitoring in Buck Mode

SY6907 closely monitors the input and system voltage, as well as HSFET and LSFET current for safe Buck mode operation.

Input Over Voltage (ACOV)

The maximum input voltage for Buck mode operation is 6.4V. If VBUS voltage exceeds 6.4V, the device will stop switching immediately. During the input over voltage (ACOV), the fault register REG09[5:4] is set to 01. An INT is asserted to the host.

System Over Voltage Protection (SYSOVP)

The charger device monitors the voltage at SYS. When the system over-voltage is detected, the converter will be stopped to protect components connected to SYS from the high voltage damage.

Voltage and Current Monitoring in Boost Mode

SY6907 closely monitors the VBUS voltage, as well as HSFET and LSFET current to ensure safe Boost mode operation.

VBUS Over Voltage Protection

The Boost mode regulated output is 5V. When an adapter plugs in during the Boost mode, the VBUS voltage will rise above the regulation target. Once the VBUS voltage exceeds 5.3V, SY6907 will stop switching and the device will exit the Boost mode. The fault register REG09[6] will be set high to indicate fault in the Boost operation. An INT will be asserted to the host.

Battery Protection

Battery Over Voltage Protection (BATOVP)

The battery over-voltage limit is clamped at 4% above the battery regulation voltage. When the battery over voltage occurs, the charger device will immediately disable the charge. The fault register REG09[5] will go high and an INT will be asserted to the host.

Charging During Battery Short Protection

If the battery voltage falls below 2V, the charge current is reduced to 100mA for battery safety.

System Over Current Protection

If the system is shorted or exceeds the over current limit, the BATFET will be latched off. The DC source insertion on VBUS is required to reset the latch off condition and turn on the BATFET.

17. Serial Interface

SY6907 uses the I^2C compatible interface for flexible charging parameter programming and instantaneous device status reporting. Only two BUS lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the BUS and generates the clock signals to permit that transfer. At that time, any device addressed is considered as a slave.

The device operates as a slave device with address 6BH, receiving control inputs from the master device like a micro controller or a digital signal processor. The I^2C interface supports both the standard mode (up to 100kbits) and the fast mode (up to 400kbits).

Both SDA and SCL are bi-directional lines, connected to the positive supply voltage via a current source or a pull- up resistor. When the BUS is free, both lines are HIGH. The SDA and SCL pins are open drain.

Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transfer.

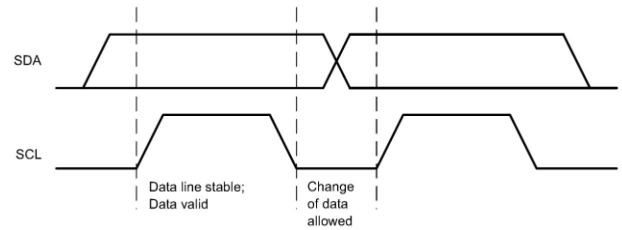


Figure 6. Bit Transfer on the I^2C BUS

START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The BUS is considered busy after the START condition, and free after the STOP condition.

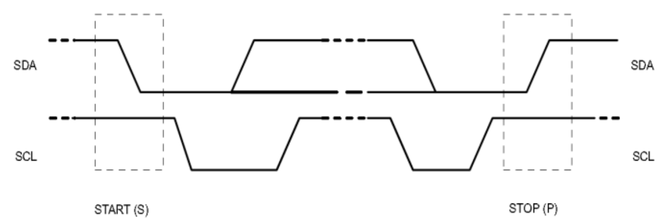


Figure 7. START and STOP conditions

Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. The data is transferred with the most significant bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). The data will transfer then continue when the slave is ready for another byte of data and release the clock line SCL.

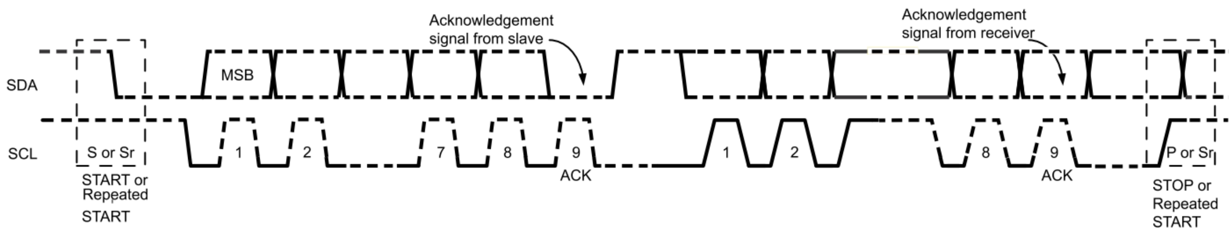


Figure 8. Data Transfer on the I²C BUS

Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the 9th clock pulse, this is the not acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A "0" indicates a transmission (WRITE) and a "1" indicates a request for data (READ).

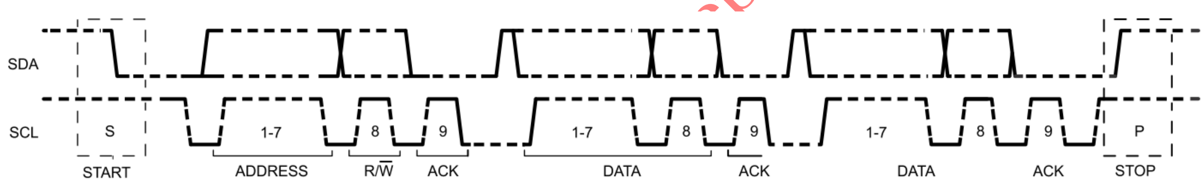


Figure 9. Complete Data Transfer

Single Read and Write

Figure 10. Single Write

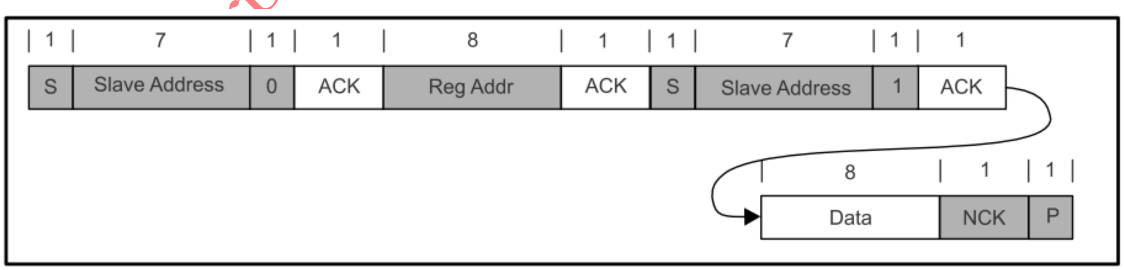


Figure 11. Single Read

If the register address is not defined, the IC sent back NACK and return to the idle state.

Multi-Read and Multi-Write

The charger device supports multi-read and multi-write on REG00 through REG08.

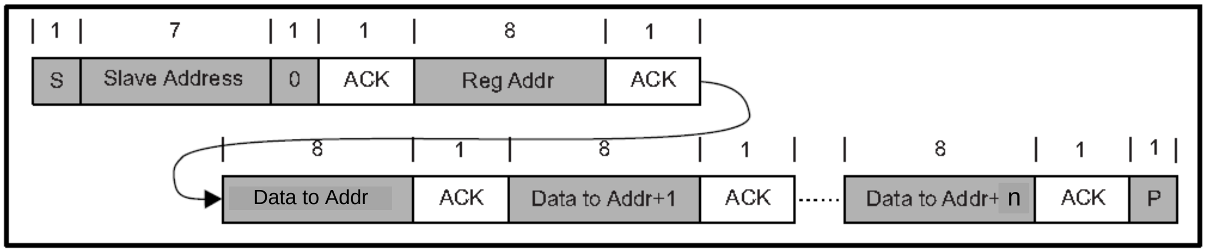


Figure12. Multi-Write

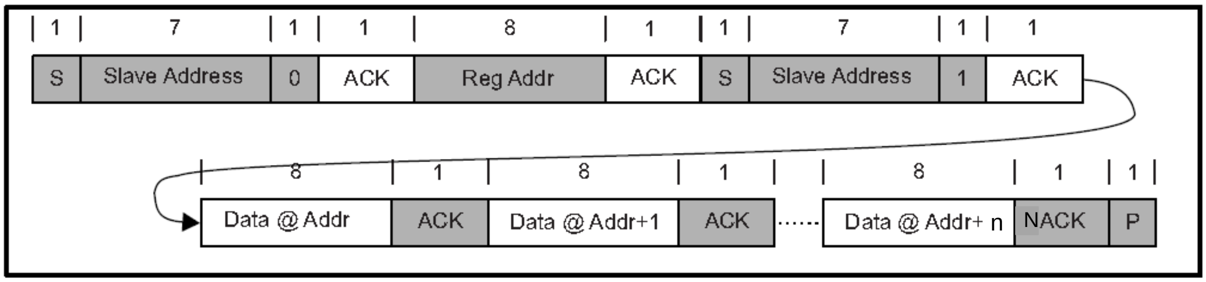


Figure 13. Multi-Read

The fault register REG09 locks the previous fault and only clears it after the register is read. In addition, the fault register REG09 does not support multi-read or multi-write.

Applications Information

The following battery charger design refers to the "Schematic Diagram" (see Figure 1.). This section describes how to select the external components including the inductor, the input and output capacitors, the sense resister.

Inductor Selection

Higher switching frequency allows the using of the smaller inductor and the capacitor values. The inductor saturation current should be higher than the load current (I_{LOAD}) plus half of the ripple current (I_{Ripple}):

$$I_{SAT} \geq I_{LOAD} + \frac{1}{2} \times I_{Ripple}$$

The inductor ripple current depends on the input voltage (V_{IN}), the duty cycle ($D = V_{OUT}/V_{IN}$), the switching frequency (F_{SW}) and the inductance (L):

$$I_{Ripple} = \frac{V_{IN} \times D \times (1-D)}{f_{SW} \times L}$$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. Usually the inductor ripple is designed in the range of (20-40%) maximum charging current as a trade-off between the inductor size and efficiency for a practical design.

Output Capacitor Selection

The output capacitor in parallel with the battery is used for absorbing the high frequency switching ripple current and smoothing the output voltage. The RMS value of the output ripple current I_{RMS} is calculated as follow:

$$I_{RMS} = \frac{V_{IN}}{\sqrt{12}L \times f_{SW}} \times D \times (1-D)$$

Where the duty cycle D is the ratio of the output voltage (battery voltage) over the input voltage for CCM mode which is the typical operation for the battery charger. During the battery charge period, the battery voltage varies from its initial battery voltage to the rated voltage. A typical 60μF ceramic capacitor is a good choice to absorb this current and also has a very small size.

Input Capacitor Selection

The input capacitor absorbs input ripple current from the Buck converter, which is given by the below equation:

$$I_{RMS} = I_{LOAD} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

This RMS ripple current must be smaller than the rated RMS current in the capacitor datasheet.

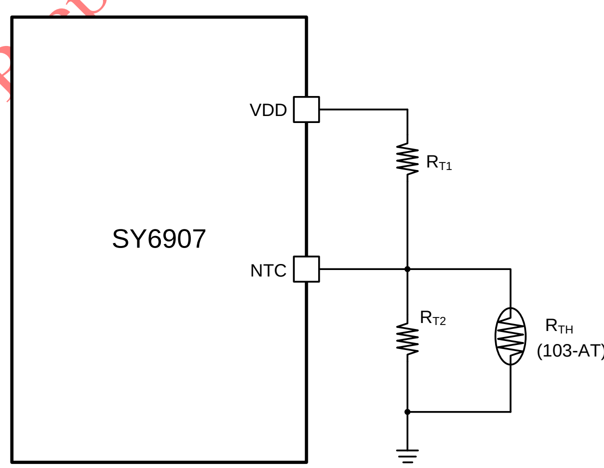
At the same time, the input capacitor is also as the output capacitor when Boost works. At this condition, the input capacitor can be calculated as below:

$$C_{IN} = \frac{I_{BUS} \times (V_{BOOST} - V_{BAT})}{f_{SW} \times V_{BOOST} \times V_{RIPPLE}}$$

Usually V_{RIPPLE} is designed less than 0.5% of the Boost output voltage. A typical 20μF ceramic capacitor is a good choice to absorb this current and also has a very small size.

NTC Resistor Slection

SY6907 continuously monitors the battery temperature by measuring the voltage between the NTC pins and the ground, typically determined by a negative temperature coefficient thermistor and an external voltage divider. The device compares this voltage against its internal thresholds to determine if the charging is allowed. During the charge cycle the battery temperature must be within the V_{LTF} to V_{HTF} thresholds, or else the device will suspend charging.



Assuming a 103AT NTC thermistor is used on the battery pack, the value of RT1 and RT2 can be calculated as below:

$$RT2 = \frac{V_{DD} \times R_{COLD} \times R_{HOT} \times (1/V_{LTF} - 1/V_{HTF})}{R_{HOT} \times (V_{DD}/V_{HTF} - 1) - R_{COLD} \times (V_{DD}/V_{LTF} - 1)}$$

$$RT1 = \frac{V_{DD}/V_{LTF} - 1}{1/RT2 + 1/R_{COLD}}$$

Layout Design:

The layout design of SY6907 regulator is relatively simple. For the best efficiency and to minimize noise problems, we should place the following components close to the IC: C_{PMID}, C_{VDD} and C_{BOOT}.

1) It is desirable to maximize the PCB copper area adjacent to GND pin to achieve the best thermal and noise performance. If the board space allows, a ground plane is highly desirable.

2) C_{PMID}, C_{VDD} and C_{BOOT} must be close to the IC.

3) The loop area formed by C_{PMID} and GND must be minimized. The PCB copper area adjacent to LX pin must be minimized to avoid the potential noise problem. The following picture is the recommended layout design of LX, C_{PMID} and C_{BOOT} .

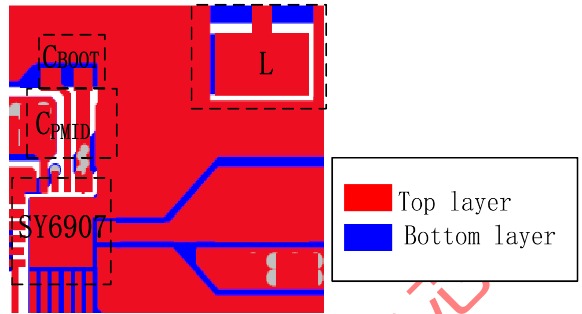
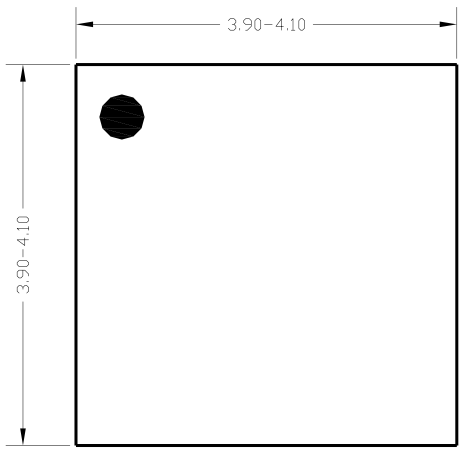
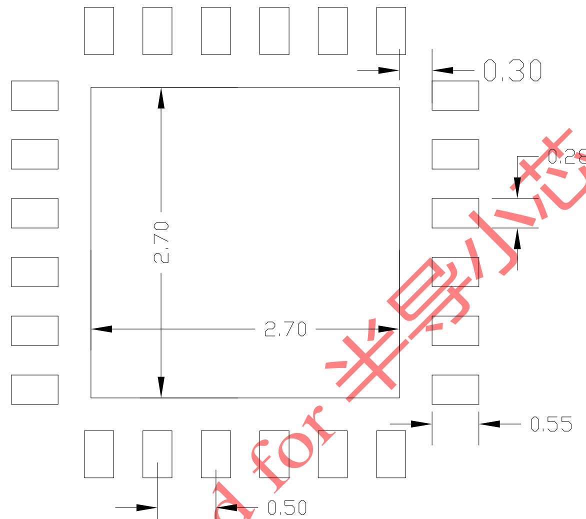


Figure14. PCB Layout Suggestion

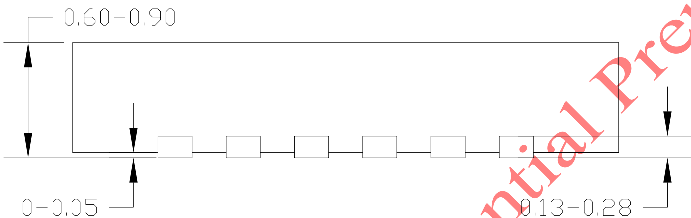
QFN4×4-24 Package Outline & PCB Layout



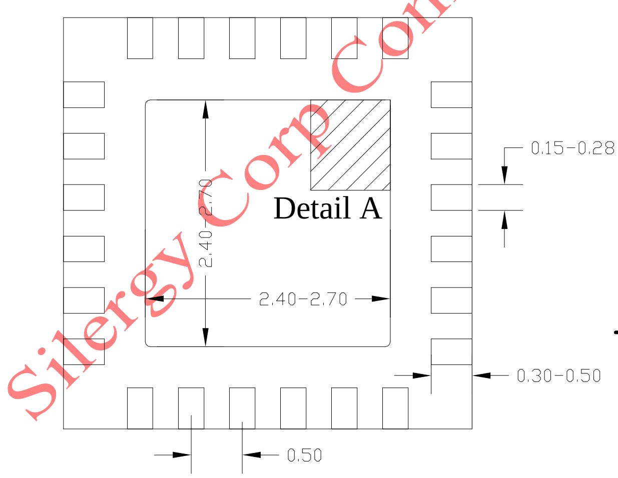
Top View

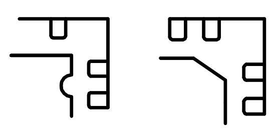


PCB layout (Recommended)



Side View





Detail A
Pin1 identifier: two options

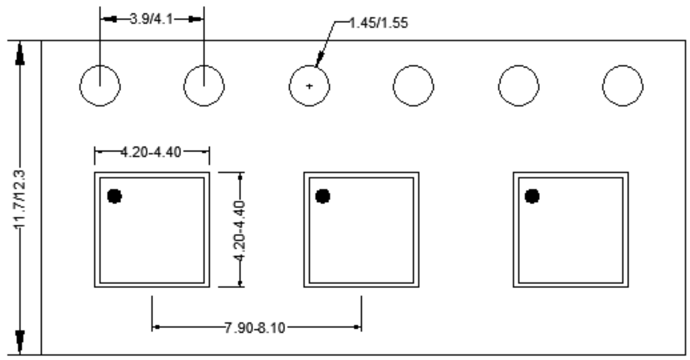
Bottom View

Notes: **All dimension in MM and exclude mold flash & metal burr**

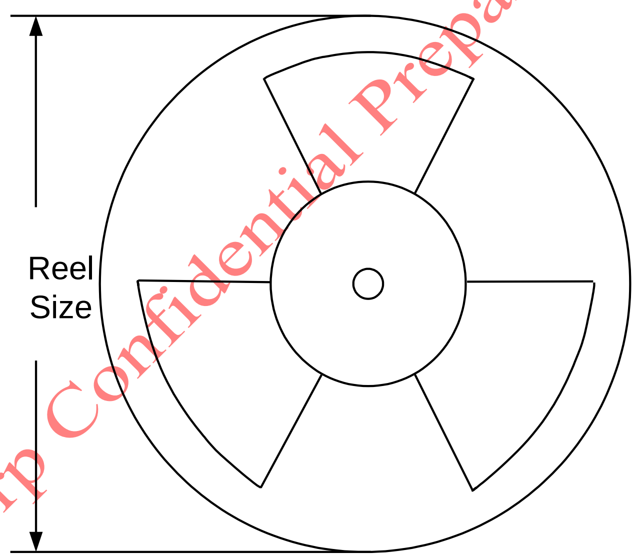
Taping & Reel Specification

1. Taping orientation

QFN4×4



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN4×4	12	8	13"	400	400	5000

3. Others: NA

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