Application Notes: AN_SY6990

Wide Input, High current, Bi-directional Regulator for Single Cell Li-Ion Battery Power Bank Application

Advanced Design Specification

General Description

SY6990 is a 4.0-13.5V input, bi-directional regulator for Li-Ion battery power bank application. Advanced bi-directional energy flow control with automatic input power source detection is adopted to achieve battery charging mode and battery power supply mode alternately. If the external power supply is present, SY6990 runs in battery charging mode with fully protection function. If the external power supply is absent, SY6990 runs in battery power supply mode with output current capability up to 3A.

SY6990 has an integrated reverse blocking switch to prevent from current leaking from the system side or battery side to the input side and an integrated linear switch to achieve over voltage/current protection at the system side. A half bridge with quasi-fixed 0.5MHz switching frequency is integrated to achieve power conversion for battery charging mode and battery power supply mode. All of them adopt N-channel MOSFETs with 16V rating and extremely low $R_{DS(ON)}$ to optimize operation efficiency and extend battery life-time.
SY6990 is available in QFN4x4 package to minimize the PCB layout size for wide portable applications.

Ordering Information

SY6990 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY6990QCC	QFN4x4-24	

Features

- Integrated N-Channel MOSFETs with 16V Voltage Rating and Extremely Low $R_{DS(ON)}$
- High Switching Frequency to Minimize Peripheral Circuit Design
- Trickle Current / Constant Current / Constant Voltage Charging Mode
- Maximum 5A Battery Charging Current
- Maximum 3A System current in Battery power supplement mode
- USB Port Identifier for Various Input Current Limit
- Automatic Input Power Source Detection
- I^2C Controls
  - Selectable Battery Charge Voltage
  - Programmable Constant Current Charging
  - Programmable Over Current Limit for SYS load
  - Programmable Battery Charging Timeout
  - Programmable Input Current DPM
  - Programmable Input Voltage DPM
- Charging Shutdown Control
- Charging Mode CV Tolerance +/-0.5%
- DO+/DO- Divider Mode Compliant
- Host Enable Control for Standby Mode
- Over Temperature Protection
- Charge Status Indication
- Light load Status Indication
- Supply System by both Adapter and Battery in Supplement mode

Applications

- Single cell Li-Ion Power Bank
- Portable device with 1-cell battery pack

Typical Applications

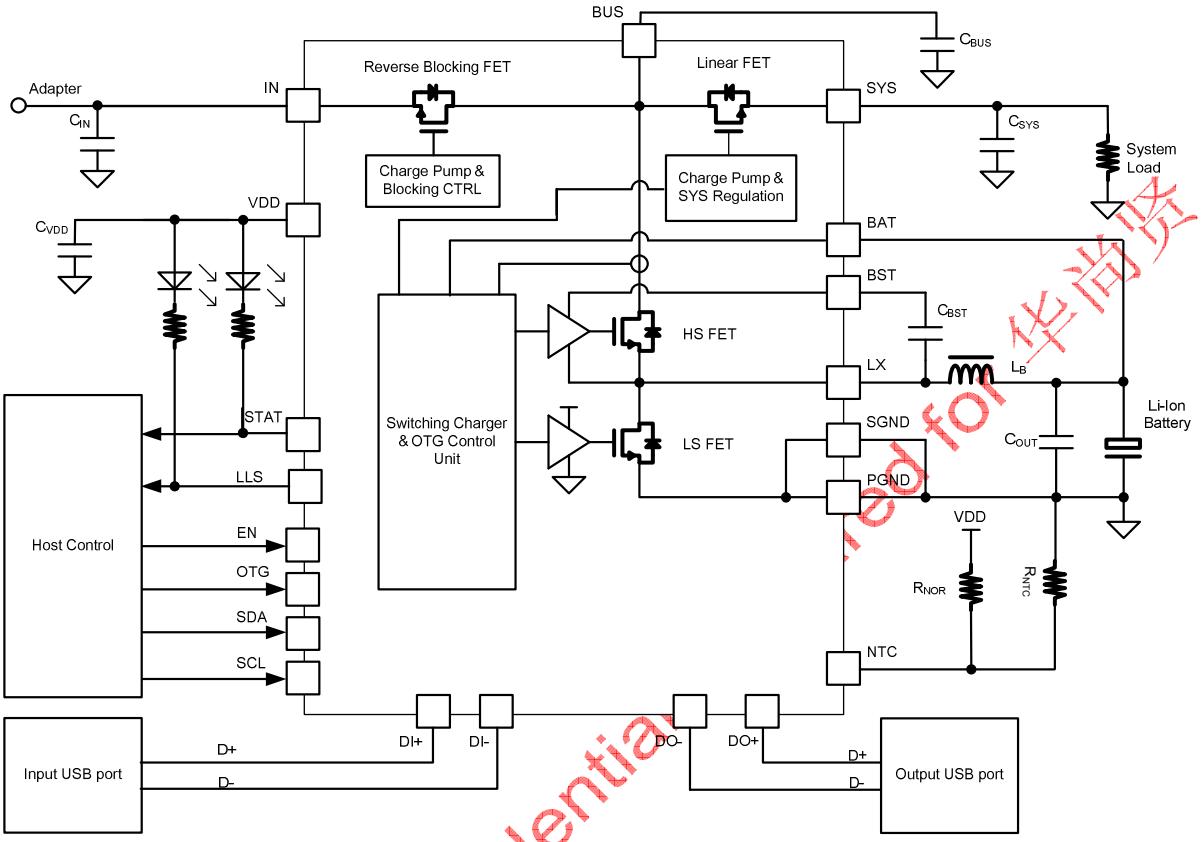
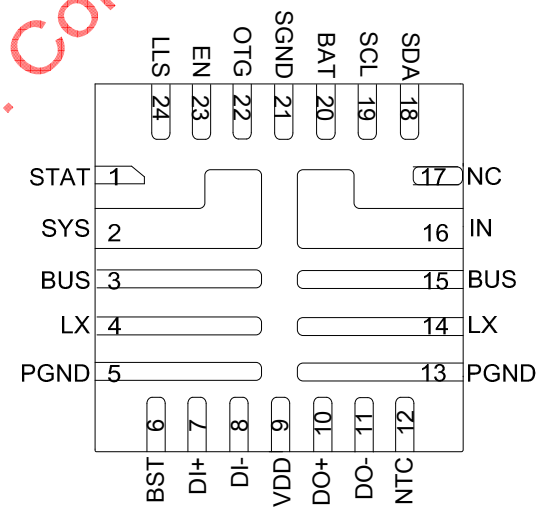


Figure 1. Schematic Diagram

Pinout (Top view)



(QFN4x4-24)

Top Mark: BGW*xyz* (device code: **BGW**, ***x=year code, y=week code, z= lot number code)***

Name	PIN Number	Description
STAT	1	Charging status indication pin. It is open drain output pin and can be used to turn on a LED to indicate the charge in process. When the charge is done, LED is off. STAT pin will be pulled low for about 200uS when DATA pins handshake is done.
SYS	2	System load pin. Connect a MLCC from this pin to ground to decouple the high frequency noise.
BUS	3,15	Connection point for reverse blocking FET and bypass linear switch. Connect a MLCC from this pin to ground to decouple the high frequency noise.
LX	4,14	Switch node pin. Connect an external inductor from this pin to BAT pin.
PGND	5,13	Power ground pin.
BST	6	Boot strap pin. Connect a MLCC from this pin to LX.
DI+	7	Host USB D+ connection. For USB input identification
DI-	8	Host USB D- connection. For USB input identification
VDD	9	Internal Linear regulator output. VDD is the output of 3.3V Linear regulator. The LDO is active when EN is high. Connect a 1uF ceramic capacitor from VDD to GND.
DO+	10	USB D+ for system connection. Support Divider mode and BC1.2 handshake.
DO-	11	USB D- for system connection. Support Divider mode and BC1.2 handshake.
NTC	12	Thermal protection and battery detection pin. In charging mode UTP threshold is about 65% VDD and OTP threshold is about 35% VDD. In discharging mode UTP threshold is about 81% VDD and OTP threshold is about 30% VDD.
IN	16	Positive power supply input pin. VIN ranges from 4V to 13.5V for normal operation and up to 16V surge. Connect a MLCC from this pin to ground to decouple high frequency noise.
NC	17	Not Connect.
SDA	18	I2C Interface data.
SCL	19	I2C Interface clock.
BAT	20	Battery positive sense pin.
SGND	21	Signal ground pin.
OTG	22	Enable control pin for system power supply. If the external power source is present, pull down OTG to shutdown linear FET. If the external power source is absent, pull down OTG to shutdown linear FET and sync-boost converter both to save the leakage power from battery.
EN	23	Whole chip enable pin. EN high to enable IC, low to shutdown IC.
LLS	24	System light load indicate pin, It is an open drain output pin and is used to turn on a LED to indicate the light system load condition lower then 50mA/200mA (set by I2C).

Absolute Maximum Ratings (Note 1)

IN, LX, BUS, BAT, SYS ---------- -0.5- 18V
STAT, SCL, SDA, DI+, DI-, DO+, DO-, NTC, EN, OTG, LLS ---------- -0.5- 18V
VDD, BST-LX ---------- -0.5- 4V
Power Dissipation, PD @ TA = 25°C, ---------- 2.5 W
Package Thermal Resistance (Note 2)
θJA ---------- 40 °C/W
θJC ---------- 20 °C/W
Junction Temperature Range ---------- -40°C to +150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 125°C

Recommended Operating Conditions (Note 3)

IN, LX, BUS, BAT, SYS ---------- 0- 16V
STAT, SCL, SDA, DI+, DI-, DO+, DO-, NTC, EN, OTG, LLS ---------- 0- 16V
VDD, BST-LX ---------- 0- 3.6V
Junction Temperature Range ---------- -20°C to 100°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

T_A=25°C, T_A=T_J, V_{IN}=5V, GND=0V, C_{IN}=20uF, L_B=2.2uH, C_{OUT}=20uF, C_{BUS}=20uF, C_{SYS}=10uF, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Quiescent Current						
I_{BAT}	Battery leakage current	EN and OTG pull down			10	uA
I_{IN}	Input quiescent current	EN=OTG=High, NTC=0V		1.5		mA
I_{BOOST}	Battery discharge current with Boost null-load	V_{BAT}=4.35V,Vsys=5V, I_{SYS}=0V, Converter switching		2		mA
Input Power Supply						
V_{INUVLO}	Input voltage UVLO threshold		4.0	4.2	4.4	V
V_{UVHYS}	Input voltage UVLO hysteresis	Falling edge		100		mV
LDO Output						
V_{VDD}	VDD voltage	V_{BUS}=5V		3.3		V
I_{VDD}	VDD source current	V_{VDD}=3.3V	50			mA
Linear FET						
R_{LNFT}	$R_{DS(ON)}$ of the linear NFET			30		mΩ
I_{SYSMAX}	System current limit tolerance	Reg02[4:2]=100, 2.6 A		2.6		A
V_{SYSMAX}	System clamp voltage tolerance	DCP		5.8		V
		HVDCP		13		V
Blocking FET						
R_{BKFT}	$R_{DS(ON)}$ of reverse blocking NFET			30		mΩ
Half-bridge in Buck Mode						
Voltage and Current Bias						
V_{BUS}	Supply voltage for battery charging		4.5		13.5	V
V_{BOVP_LV}	Bus voltage over voltage protection threshold for 5V adapter.	Rising edge	7			V
V_{BOVP_HV}	Bus voltage over voltage protection threshold for other higher voltage adapters	Rising edge	13.5			V
$V_{BOVPHYS}$	Bus voltage OVP hysteresis	Falling edge		400		mV
Switching Frequency						
f_{SWBK}	Buck Switching frequency			0.5		MHz
$T_{ONMINHS}$	Min on time for charging mode, HS FET			100		ns
$T_{ONMAXHS}$	Max on time for charging mode, HS FET	In low dropout mode		7		us
Battery Charging						
V_{CV}	Battery CV voltage tolerance	0°C <=T_A<=70°C, voltage on BAT pin	-0.5		0.5	%
ΔV_{RCH}	Battery voltage threshold hysteresis for recharge	0°C <=T_A<=70°C, falling edge		100		mV
V_{TRK}	Battery trickle charging mode voltage threshold	0°C <=T_A<=70°C, rising edge	2.7	2.8	2.9	V
I_{CC}	Charging current accuracy for Constant Current Mode	Reg03[2:0]=011		2		A
	Charging current accuracy for Trickle Current Mode	Reg03[2:0]=011		0.2		A
I_{TERM}	Termination current tolerance	Reg03[2:0]=011. reg01[0]=1		200		mA
		Reg03[2:0]=011. reg01[0]=0		120		mA
V_{BTOVP}	Battery voltage OVP threshold		105%	110%	115%	V_{CV}
Battery Short Circuit Protection						

$V_{SHORTBT}$	Battery short circuit protection threshold			2		V
Dynamic Input Power Management						
I_{DPM}	Input current limit tolerance	Reg02[7:5]=011		1.5		A
V_{DPM}	Input Voltage regulation during current limit		-1		1	%
USB Port Identification and Current Limit Reference (Proposal 1)						
I_{SDP}	SDP input current limit			500		mA
$I_{CDP/DCP}$	CDP/DCP input current limit			1500		mA
Half-bridge in Boost Mode						
Voltage and Current Bias						
V_{BATDEP}	Battery depletion voltage tolerance			2.6		V
V_{BOVP}	Bus voltage over voltage protection to shutdown Linear FET	Rising edge	13.5			V
$V_{BOVPHYS}$	Bus voltage OVP hysteresis	Falling edge		400		mV
V_{SYS}	SYS voltage tolerance		-2%		+2%	V_{SYS}
I_{SYS_L}	OTG light load threshold	REG02[1:0]=10		50		mA
		REG02[1:0]=11		200		mA
Switching Frequency						
f_{SWBT}	Boost Switching frequency			0.5		MHz
T_{ONMINL}	Min on time for discharging mode, LS FET			200		ns
Other General Parameters						
Battery Thermal Protection NTC						
Battery Detection	Battery removed	Rising edge	90%			V_{DD}
	Battery inserted hysteresis	Falling edge		1%		
UTP_CHG	Under temperature protection	Rising edge, charging mode	60%	65%	70%	
	Under temperature protection hysteresis	Falling edge, charging mode		5%		
OTP_CHG	Over temperature protection	Falling edge, charging mode	33%	35%	37%	
	Over temperature protection hysteresis	Rising edge, charging mode		2%		
UTP_DCHG	Under temperature protection	Rising edge, Discharging mode	79%	81%	83%	
	Under temperature protection hysteresis	Falling edge, Discharging mode		5%		
OTP_DCHG	Over temperature protection	Falling edge, Discharging mode	28%	30%	32%	
	Over temperature protection hysteresis	Rising edge, Discharging mode		2%		
Power MOSFET						
R_{HSFT}	$R_{DS(ON)}$ of High-Side NFET			20		mΩ
R_{LSFT}	$R_{DS(ON)}$ of Low-Side NFET			18		mΩ
I_{LM}	Half Bridge FET current limit		8			A
Logic Level and Timing						
V_{LOW}	EN, OTG,SCL,SDA low level threshold				0.4	V
V_{HIGH}	EN, OTG,SCL,SDA low level threshold		1.2			V

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

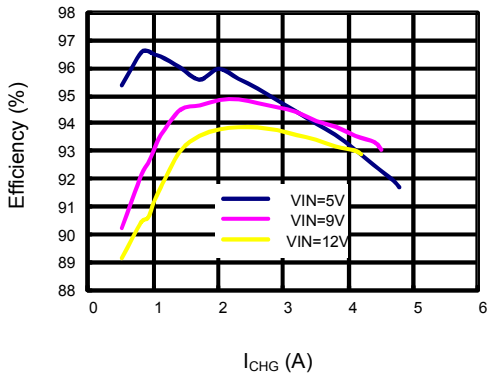
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective four-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions

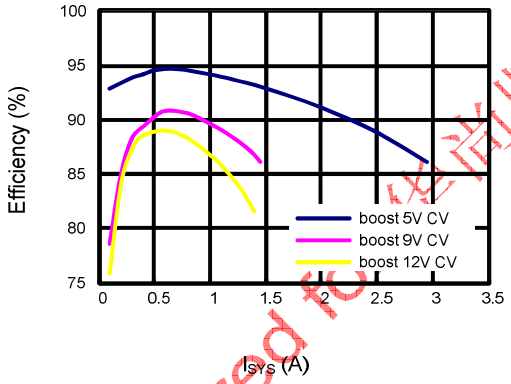
Typical Performance Characteristics

(T_A=25°C, V_{IN}=5V , unless otherwise specified.)

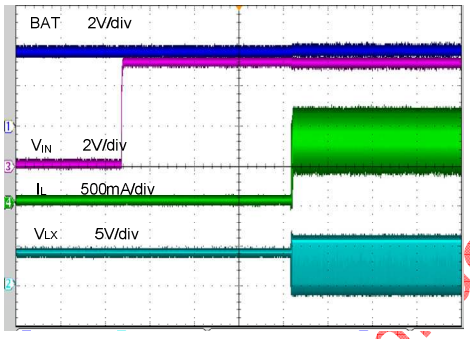
Efficiency vs. Charging current (CV mode)



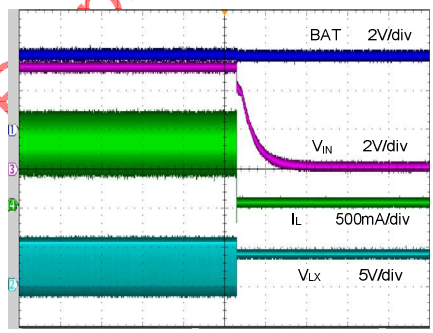
Efficiency vs. I_{SYS} (Boost mode, BAT=2.8V)



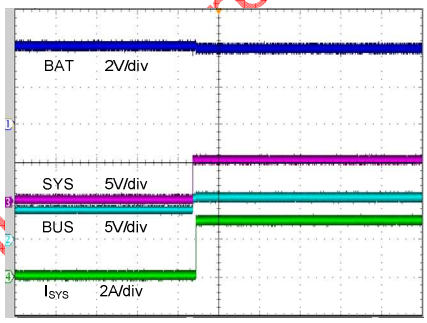
5V VIN Power on(Adapter)



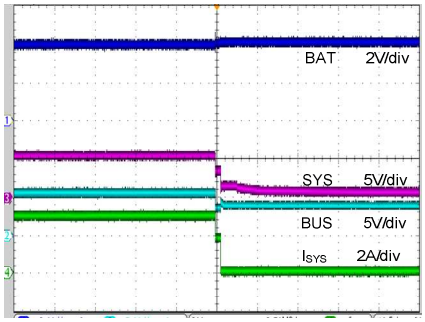
5V VIN Power off(Adapter)



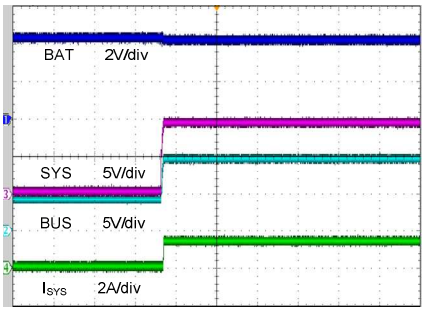
5V Boost mode OTG ON by I2C



5V Boost mode OTG OFF by I2C

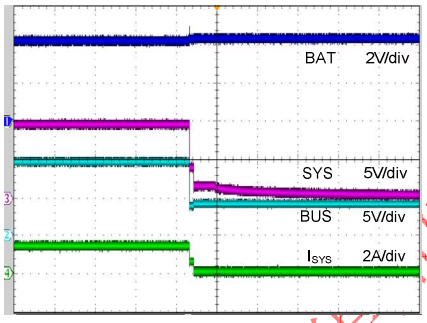


9V Boost mode OTG ON by I2C



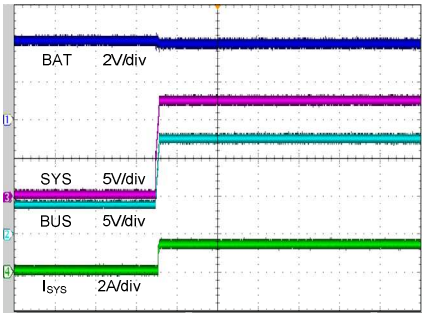
Time (200ms/div)

9V Boost mode OTG OFF by I2C



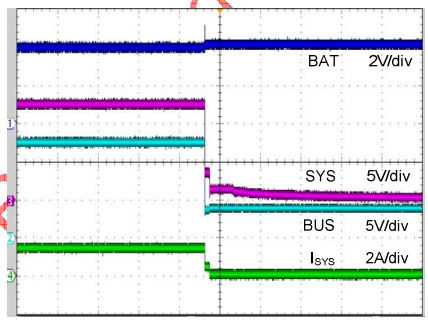
Time (200ms/div)

12V Boost mode OTG ON by I2C



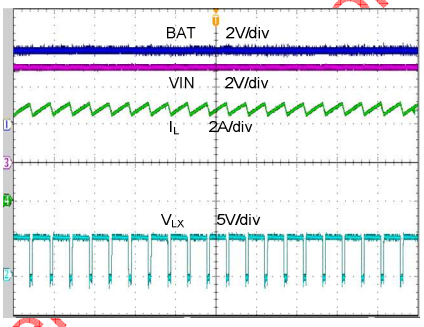
Time (200ms/div)

12V Boost mode OTG OFF by I2C



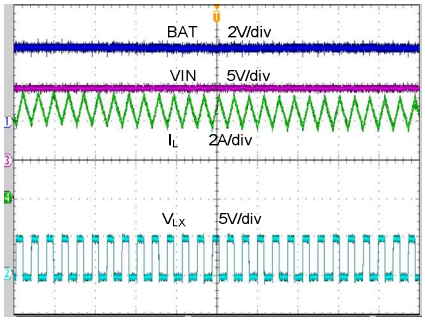
Time (200ms/div)

5V Buck Steady State



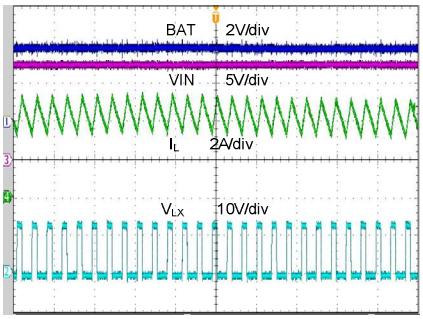
Time (4us/div)

9V Buck Steady State



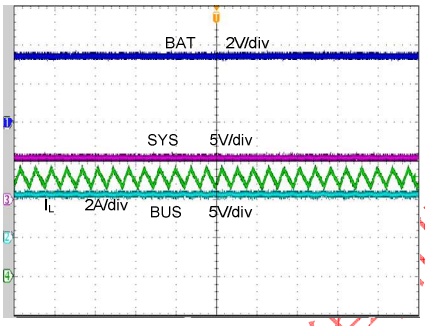
Time (4us/div)

12V Buck Steady State



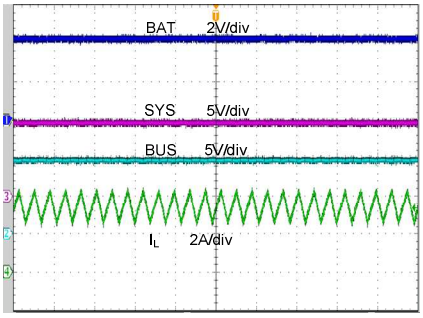
Time (4us/div)

5V Boost Steady State



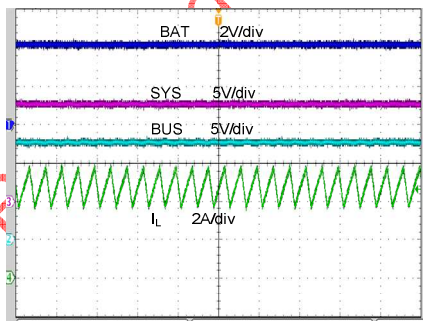
Time (4us/div)

9V Boost Steady State



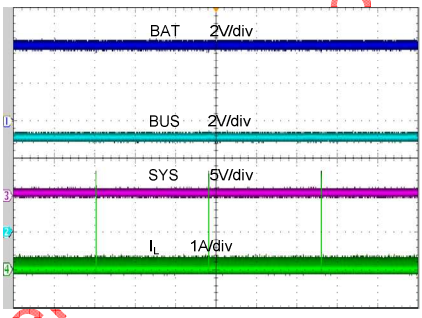
Time (4us/div)

12V Boost Steady State



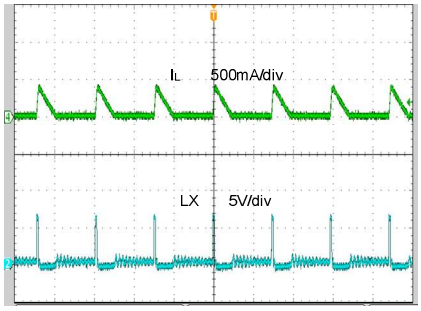
Time (4us/div)

Boost SYS Short



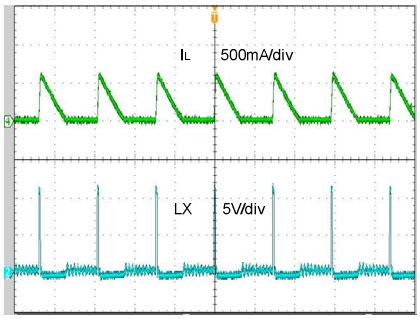
Time (200ms/div)

Battery Short In 5V Charging Mode



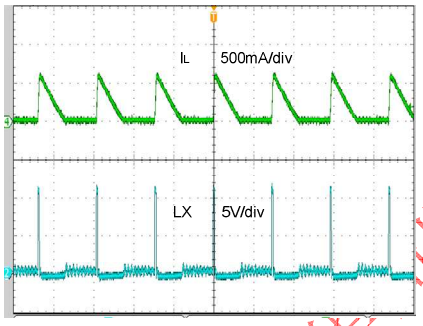
Time (4μs/div)

Battery Short In 9V Charging Mode



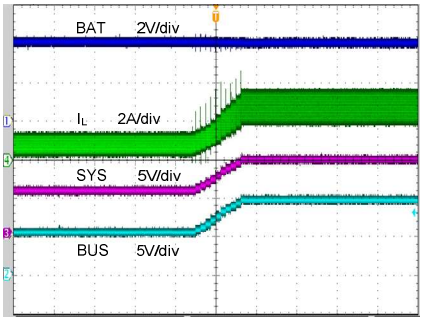
Time (4μs/div)

Battery Short In 12V Charging Mode



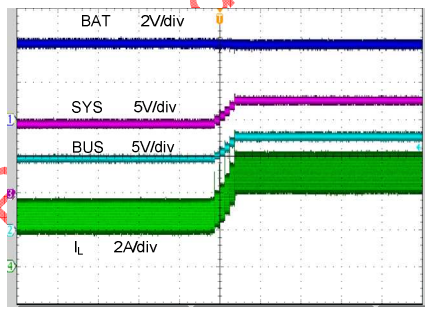
Time (4μs/div)

Boost 5V to 9V



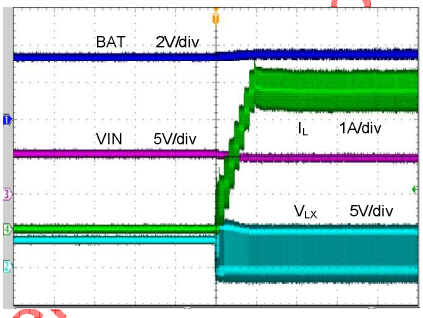
Time (10ms/div)

Boost 9V to 12V



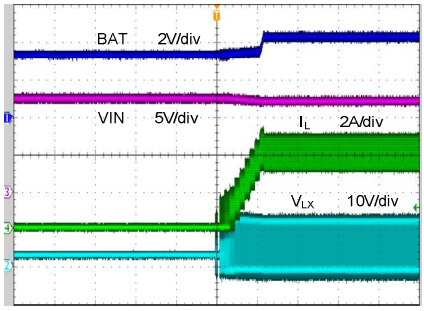
Time (10ms/div)

Inductor current soft start in 5V charging mode



Time (10ms/div)

Inductor current soft start in 12V charging mode



Time (10ms/div)

General Function Description

Working Mode Description

Charging mode. When the input source is present and there is no fault happens, SY6990 works in charging mode to charge the battery. The half bridge works in Buck mode.
If the OTG is enabled, SY6990 supplies the power to the system at the same time.

Discharging mode/Boost mode. When the input source is removed, SY6990 works in discharging mode/boost mode if V_{BAT} is higher than V_{BATDEP} and there is no fault happens.

Automatic Input Power Supply Detection

Automatic input power supply detection in SY6990 adopts an internal current source with 10mA maximum capability to discharge the IN pins for 100ms once V_{SIN} exceeds input UVLO threshold. If the external power supply is present normally, V_{IN} should keep being higher than the input voltage UVLO even after 100ms discharging. While V_{IN} is present REG00[0] will be set to 1.

Input Power Up

After Automatic Input Power Supply Detection is done and V_{IN} is present, SY6990 will enable BC1.2 detection automatically, after BC1.2 detection an INT(200us low pulse) is generated and the input USB type is recorded in REG05[1:0]. The MCU can monitor the USB type to set the appropriate Charging current\Input current limit\Input VDPM. After BC1.2 detection is done SY6990 will start charging if there is no fault happens.

SY6990 can set the DI+/DI- output voltage by REG05[7:4] and monitor the DI- input voltage by REG06[3].

After Input power up the input voltage range should be 4.2V-7V to ensure the SY6990 can work normally. In order to work in higher input voltage REG06[4] HV_VIN_EN should be 1 and REG05[3:2] should be set to 9V or 12V to change the OVP and VDPM point of SY6990.

Charging mode Enable control

When VIN is present, the charger can be controlled by I2C REG01 [7].

INT signal to MCU

SY6990 will generate the INT signal (200uS low pulse) if in below conditions.

1. Upstream D+/D- detection is done
2. Downstream D+/D- detection is done
3. Downstream D+/D- voltage level changes after the detection.

Programmable Input Current Dynamic Power Management

The input current limit is programmable by I2C REG02[7:5]. Once the input current reaches I_{DPM}, it will be limited in I_{DPM} by regulating the duty cycle of Buck converter.

Programmable Input Voltage Dynamic Power Management

The input voltage limit is programmable by REG03[7:5]. Once the input voltage drops to V_{DPM}, it will be limited in V_{DPM} by regulating the duty cycle of Buck converter.

REG00[1] will be set to 1 while SY6990 works in VDPM state.

SYS Current Limit

SYS current limit is programmed by REG02[4:2].
In boost mode, once the SYS current exceeds I_{SYS_Limit}, it is limited to I_{SYS_Limit} by regulating the duty cycle of Boost converter.
In buck mode, once SYS current exceeds I_{SYS_Limit}, the LNFET works in LDO mode to regulate SYS current to I_{SYS_Limit}.

Programmable charging current

Charging current is programmed by REG03[2:0].

Programmable termination current

Termination current can be set to 5%Icc and 10%Icc by REG01[0].

Programmable charging voltage

Charging voltage is programmed by REG03[4:3].

OTG light load indicate

Once the SYS current is lower than 50mA or 200mA set by REG02[1:0], the LLS pin will be pulled down to indicate the OTG light load. OTG light load state can be read in REG00[3].

Supplement mode

The supplement mode is enabled by REG01[6].
In bypass mode the SYS load increases may lead the SY6990 works in IDPM mode to make the buck mode PWM duty cycle decreases. When the PWM duty cycle decrease to zero and the system current goes on increasing, the converter will enter into supplement mode. In supplement mode SY6990 switches from Buck mode to Boost mode and delivers the power from both the input and the battery to SYS.

OTG Function

When VIN is present, both OTG pin and REG01[5] are active can enable OTG function to turn on LNFET.
When VIN is absent, both OTG pin and REG01[5] are active can enable OTG function to turn on the Boost converter and LNFET.

Downstream output voltage control

In default mode, **Reg_State_Con** REG06[5] is 0. In this condition REG06[7:6] is read only. The voltage which downstream requests is recorded in REG06[7:6].
When **Reg_State_Con** REG06[5] is set to 1 REG06[7:6] is readable and writable. The SYS output voltage will change to the set one by REG06[7:6] in boost mode.

OTG RESET condition

REG01[5] will be reset to 0 (OTG is disabled) while one of following faults happens:

1. BAT OVP
2. UTP/OTP
3. Thermal shutdown
4. BAT depletion

Charging Status Indication Description

1. **Charging-In-Process** – Pull and keep STAT pin to Low;
2. **Charging Done** – Pull and keep STAT pin to High;
3. **Fault Mode** – Output high and low voltage alternatively with 10Hz frequency, fault mode includes VIN OVP, BAT OVP, BAT SCP, BAT UTP/OTP, charging time out.

Connect a LED from VDD to STAT pin, **LED ON** indicates **Charging-in-Process**, **LED OFF** indicates **Charging Done**, **LED Flash** indicates **Fault Mode**.
Charging status is recorded in REG00[5:4]

Protection Description

Thermal Protection-Thermal protection for battery is achieved through NTC pin in charging and discharging mode. The basic scheme is shown in application information. Thermal shutdown is active for the device itself. IC recovers to normal work when the temperature returns into normal range again. Charging timer stops and maintains the result without reset.

Short Circuit Protection- There are BAT short circuit protection and SYS short circuit protection in SY6990. When V_{SYS} is lower than $V_{SHORTSYS}$, the linear FET modulates the current to be saw tooth shape from 0A to about 2.5A for short circuit protection recovery. SY6990 tries recovery for 5ms per 0.6s. In charging mode once V_{BAT} is lower than $V_{SHORTBT}$, the inductor current is fold back to a very low value.

Over Voltage Protection- When V_{BUS} or V_{BAT} is higher than the over voltage protection threshold, the half bridge stops Boost operation or Buck operation immediately. It recovers to normal work when the monitored voltage backs to normal level. Input voltage has UVLO and OVP, which would make the device shutdown and recover to normal work when the V_{SIN} backs to normal range.

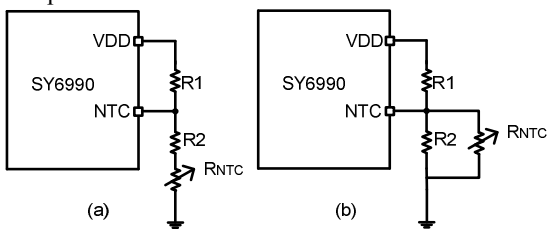
Input Over Current Protection- SY6990 can protect the IC from input over current. Higher than 110%I_{DPM} will trigger the input over current protection and it will recover to normal when the fault is removed.

Battery Over discharge protection- IN OTG mode, once battery voltage is lower than V_{BATDEP}, SY6990 will turn off the Boost and the LNFET.
Timeout Protection- Timeout time is set by REG01[2:1]. Once timeout is active, the device stops the charge operation and latch-off. Only re-plug the input power source can reset the latch logic and restart the normal charging work.

Applications Information

Because of the high integration of SY6990, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, bus capacitor C_{BUS}, battery capacitor C_{BAT}, inductor L, NTC resistors R1, R2, need to be selected for the targeted applications specifications.

NTC resistor:
SY6990 monitors battery temperature by measuring the BUS voltage and NTC voltage. The controller triggers the UTP or OTP when the rate K (K= V_{NTC}/V_{VDD}) reaches the threshold of UTP (K_{UT}) or OTP (K_{OT}). The temperature sensing network is showed as below.
Choose R1 and R2 to program the proper UTP and OTP points.



The calculation steps of Figure (a) are:
1. Define K_{UT}, K_{UT} =65%
2. Define K_{OT}, K_{OT} =35%
3. Assume the resistance of the battery NTC thermistor is R_{UT} at UTP threshold and R_{OT} at OTP threshold.
4. Calculate R2

$$R2 = \frac{K_{OT}(1-K_{UT})R_{UT} - K_{UT}(1-K_{OT})R_{OT}}{K_{UT} - K_{OT}}$$

5. Calculate R1

$$R1 = (1/K_{OT} - 1)(R2 + R_{OT})$$

If choose the typical values K_{UT} =65% and K_{OT}=35%, then

$$R2 = 0.408R_{UT} - 1.408R_{OT}$$
$$R1 = 1.857(R2 + R_{OT})$$

Input capacitor C_{IN}:
Input capacitor reduces the surge current drawn from the input and the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent high-frequency-switching current from passing to the input.

To minimize the potential noise problem, place a typical X7R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins. At least 20uF ceramic capacitor is suggested.

Bus capacitor C_{BUS}:
1. Buck mode
The capacitor acts as the input capacitor of the buck converter. The input current ripple RMS value is larger than:

$$I_{CIN\_MIN} = I_{CHG}\sqrt{D(1-D)}$$

Where I_{CHG} is the charge current.
2. Boost mode
C_{BUS} is the output capacitor of boost converter. C_{BUS} reduces the bus voltage ripple and ensures the stability of boost. The output current ripple RMS value is :

$$I_{CBUS\_RMS} = \frac{\Delta I}{2\sqrt{3}}$$

Where ΔI is the current ripple of inductor.
At least 20uF ceramic capacitor is suggested.

Battery capacitor C_{BAT}:
1. Buck mode
Battery capacitor acts as the output capacitor of Buck converter. C_{BAT} is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X7R or better grade ceramic capacitor. The output voltage ripple is calculated as below:

$$V_{Ripple\_BAT\_Buck} = \frac{(1-D)\times V_{BAT}}{8C_{BAT}F_{SW}{}^2L}$$

Where F_{SW} is the switching frequency.
2. Boost mode
C_{BAT} acts as the input capacitor of Boost converter. The input voltage ripple is calculated as below:

$$V_{Ripple\_BAT\_Boost} = \frac{D\times V_{BAT}}{8C_{BAT}F_{SW}{}^2L}$$

Where F_{SW} is the switching frequency.
At least 20uF ceramic capacitor is suggested.

Inductor L:
Inductor selection trades off between cost, size, and efficiency. A lower inductance value corresponds with smaller size, but results in higher ripple currents, higher magnetic hysteretic losses, and higher output capacitances. However, a higher inductance value benefits from lower ripple current and smaller output filter capacitors, but results in higher inductor DC

resistance (DCR) loss. An inductor must not saturate under the worst-case condition.

1. Buck mode

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the average input current. The inductance is calculated as:

$$L = \frac{V_{BAT}(1 - V_{BAT}/V_{IN,MAX})}{F_{SW} \times I_{CHG,MAX} \times 40\%}$$

Where F_{SW} is the switching frequency and $I_{CHG,MAX}$ is the maximum charge current.

SY6990 is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{CHG,MAX} + \frac{V_{BAT}(1 - V_{BAT}/V_{IN\ MAX})}{2 \times F_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement.

2. Boost mode

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the average input current. The inductance is calculated as:

$$L = \frac{V_{BAT}(1 - V_{BAT}/V_{BUS\_MAX})}{F_{SW} \times I_{DIS,MAX} \times 40\%}$$

Where F_{SW} is the switching frequency and $I_{DIS,MAX}$ is the maximum discharge current.

SY6990 is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{DIS,MAX} + \frac{V_{BAT}(1 - V_{BAT}/V_{BUS\_MAX})}{2 \times F_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement.

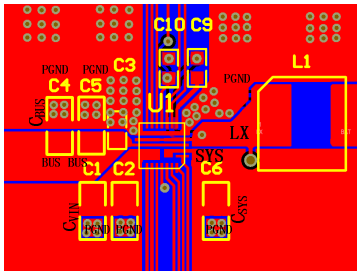
SY6990 is a high integrated IC and the internal compensation circuits also limit the inductor choice. Out of the range from 0.68uH to 3.3uH is not suggested.

Layout Design:

The layout design of SY6990 regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{IN}, C_{BUS}, C_{SYS}, L_B.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2) C_{IN} must be close to Pins IN and GND, C_{BUS} must get close to Pins BUS and GND. The loop area formed by C_{IN} and GND, C_{BUS} and GND must be minimized. Following figure is the recommended layout design.



3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

4) The capacitor C_{TIM} and the trace connecting to the TIM pin must not be adjacent to the LX net on the PCB layout to avoid the noise problem. It should be better to ground C_{TIM} to the output capacitor's ground.

5) In high current applications, a RC snubber circuit should be placed between LX and GND for better EMI.

Register Description

Battery Charger Registers

The SY6990 supports 7 battery-charger registers that use either Write-Word or Read-Word protocols, as summarized in Table 1. 04H are "read only" registers and can be used to identify the SY6990.

Table 1. Battery Charger Registor Summary

Register Address	Register Name	Read/Write	Default
00H	Status/Control Register	Read or Write	00H
01H	Control Register	Read or Write	84H
02H	Current Register	Read or Write	FBH
03H	Charge Register	Read or Write	89H
04H	Vendor/PN/Rev Register	Read	BxH
05H	Upstream USB type Register	Read or Write	xxH
06H	Downstream USB type Register	Read or Write	xxH

Table 2. Status/Control Register (00H)

Bit	Bit Name	R/W	Description
7	Reset	R/W	Write 1 to reset all the parameters, auto clear.
6	Boost	R	1: In boost mode 0: Not in boost mode
5:4	Status	R	00: Ready 01: Charge in progress 10: Charge done 11: Fault
3	BST_LLOAD	R	0:I_{SYS}> I_{SYS_L} 1: I_{SYS}< I_{SYS_L} ,Boost mode light load
2	BAT_DPL	R	0: V_{BAT}> V_{BATDEP} 1: V_{BAT}< V_{BATDEP}
1	VDPM_STATE	R	1: In VDPM state; 0: Not in VDPM state.
0	VIN_PRES	R	1: Vin present; 0: Vin absent.

Table 3. Control Register (01H)

Bit	Bit Name	R/W	Description
7	Charge_Enable	R/W	0: Disable charger 1: Enable charger (default)
6	Supplement_Enable	R/w	0: Disable charge Supplement mode (default) 1: Enable charge Supplement mode
5	OTG_Enable	R/W	0: Disable OTG mode(default) 1: Enable OTG mode Both OTG and the register are available can enable OTG function.
4	Reserved	NA	

3	V_{SYS} comp	R/W	System output voltage compensation in 5V mode. 1: 5.525V; 0: 5.125V (default).
2:1	Timer	R/W	Charge timeout protection. 00: 5h 01: 10h 10: 20h (default) 11: Disable timer
0	ITERM_Current	R/W	0: 5%*ICC (default) 1:10%*ICC

Table 4. Current Register (02H)

Bit	Bit Name	R/W	Description
7:5	IDPM	R/W	Input current limit for 5/9/12V source. 001: 500/400/400mA current limit 010: 1000/800/800mA current limit 011: 1500/1200/1200mA current limit 100: 2000/1600/1600mA current limit 101: 2500/2000/2000mA current limit 110: 3000/2400/2400mA current limit 111: Disable input current limit (default)
4:2	ISYS_Limit	R/W	SYS current limit for 5/9/12V SYS voltage. 000: 1/0.5/0.5A 001: 1.4/0.7/0.7A 010: 1.8/0.9/0.9A 011: 2.2/1.1/1.1A 100: 2.6/1.3/1.3A 101: 3/1.5/1.5A 110: 3.4/1.7/1.7A (default) 111: 3.4/1.7/1.7A
1	OTG_Lightload_EN	R/W	0:Disable OTG_Lightload detection 1:Enable OTG_Lightload detection (default)
0	OTG_Lightload	R/W	0:50mA 1:200mA (default)

Table 5. Voltage Register (03H)

Bit	Bit Name	R/W	Description
7:5	VDPM	R/W	V_{IN} threshold for input current limit. The offset is -0.3V based on 5V,-0.35V based on 9V or 12V. For example, V_{DPM}=5*(1-bit[7:5])-0.3 for 5V_{IN}. The VDPM need be clamped upon UVLO threshold. 000: 0 001: -1% 010: -2% 011: -3% 100: -4% (default) 101: -5% 110: -6% 111: Disable VDPM
4:3	Charge_Voltage	R/W	1-cell charge voltage. 00: 4.10V charge voltage 01: 4.20V charge voltage (default) 10: 4.35V charge voltage 11: 4.4V charge voltage
2:0	Charge_Current	R/W	000: 0.5A charge current 001: 1A charge current (default)

			010: 1.5A charge current 011: 2A charge current 100: 2.5A charge current 101: 3A charge current 110: 4A charge current 111: 5A charge current

Table 7. Vendor/PN/Rev Register (04H)

Bit	Bit Name	R/W	Description
7:5	Vendor_Code	R	101: Identify the supplied
4:3	PN	R	11: SY6990
2:0	Revision	R	001: Revision 1.0 010: Revision 1.1 011: Revision 1.2 ……

Table 8. Upstream USB type Register (05H)

Bit	Bit Name	R/W	Description
7:6	DI+_Output_Voltage	R/W	11: Floating 10: High 01: Low 00: 0V(default)
5:4	DI-_Output_Voltage	R/W	11: Floating 10: High 01: Low 00: 0V(default)
3:2	Input_Voltage_Set	R/W	11:12V 10: 9V 0x: 5V(Default)
1:0	Upstream USB type	R	11: Nonstandard adapter 10: DCP 01: CDP 00: SDP

Table 9. Downstream USB type Register (06H)

Bit	Bit Name	R/W	Description
7:6	Downstream_Voltage	R/W	11: 12V 10: 9V 0x: 5V(Default)
5	Reg_State_Con	R/W	0: REG06[7:6] read only, only indicate the voltage that downstream requests(default). 1: REG06[7:6] both read and write, output voltage is the same with REG06[7:6]
4	High_VIN_EN	R/W	0 :Don't accept high input voltage(default) 1: Accept high input voltage
3	DIM_STAT	R	0:DIM>0.325V; 1:DIM<0.325V.
2:0	Reserved	NA	

I2C Interface

SY6990 uses I2C compatible interface for flexible charging parameter programming and instantaneous device status reporting. Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address 6AH, receiving control inputs from the master device like micro controller or a digital signal processor. The I2C interface supports both standard mode (up to 100kbits), and fast mode (up to 400kbits).

Both SDA and SCL are bi-directional lines, connecting to the positive supply voltage via a current source or pull- up resistor. When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain.

Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

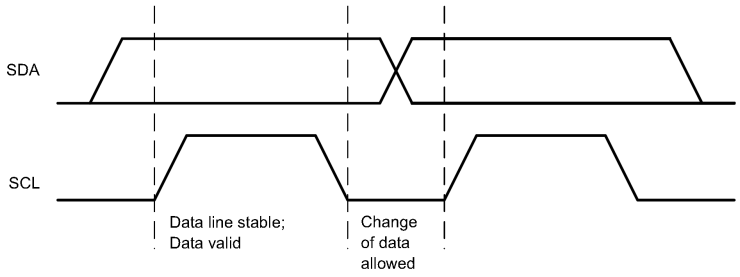


Figure 1. Bit Transfer on the I2C Bus

START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCl is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

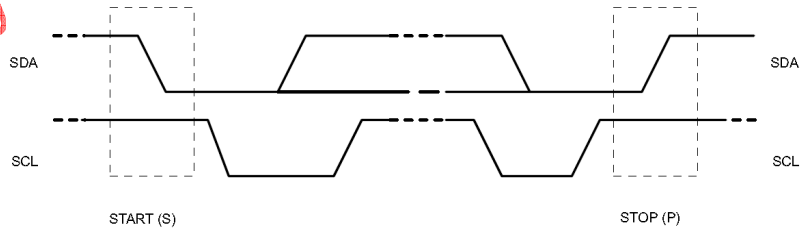


Figure 2. START and STOP conditions

Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.

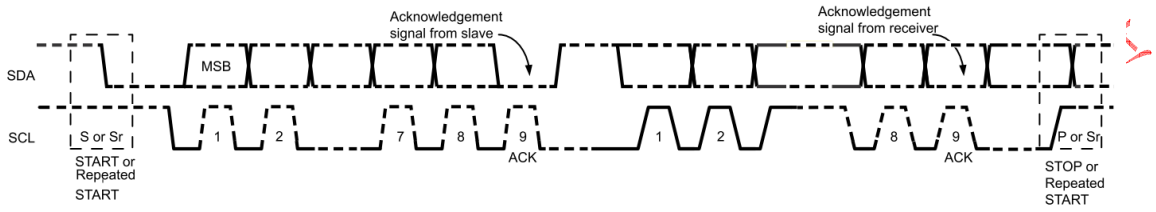


Figure 3. Data Transfer on the I2C Bus

Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the 9th clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

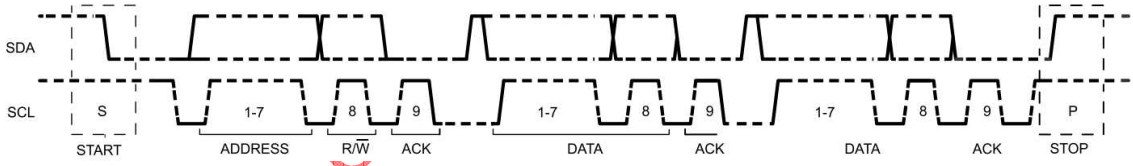


Figure 4. Complete Data Transfer

Single Read and Write

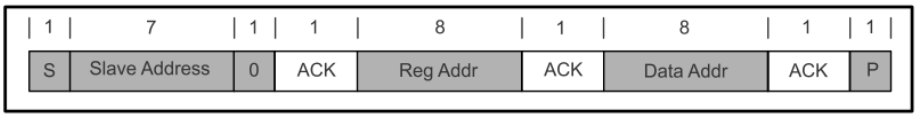


Figure 5. Single Write

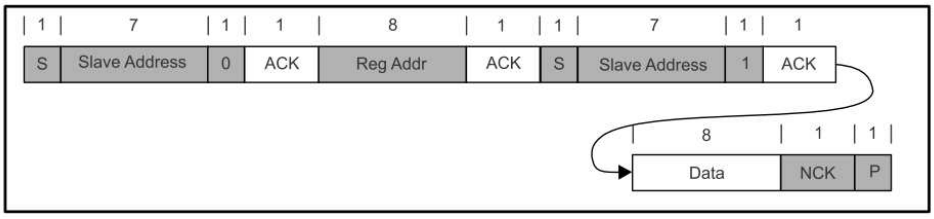
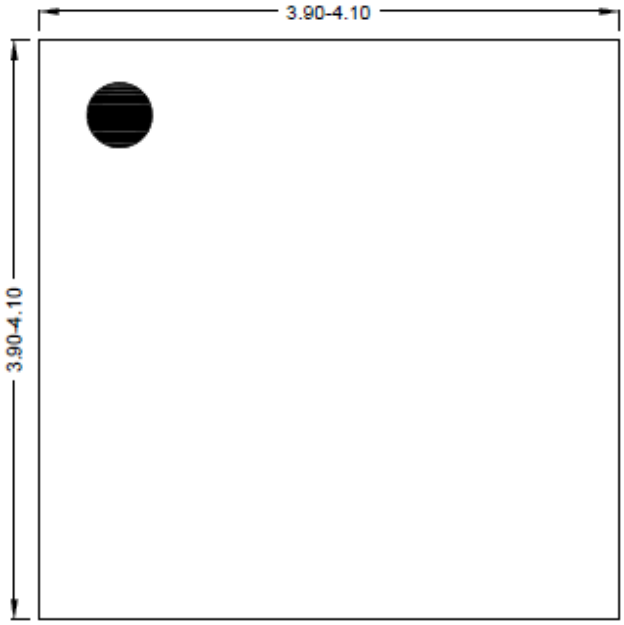


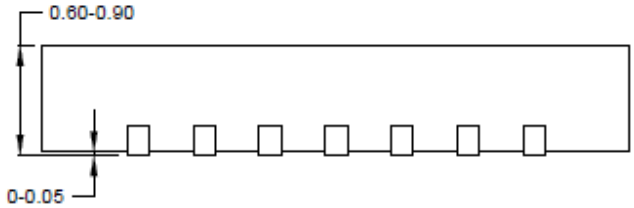
Figure 6. Single Read

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

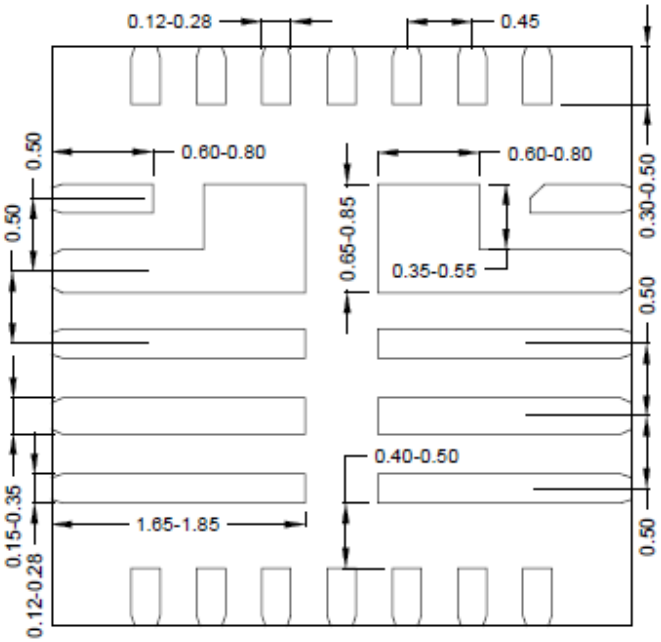
QFN4X4-24 Package Outline Drawing



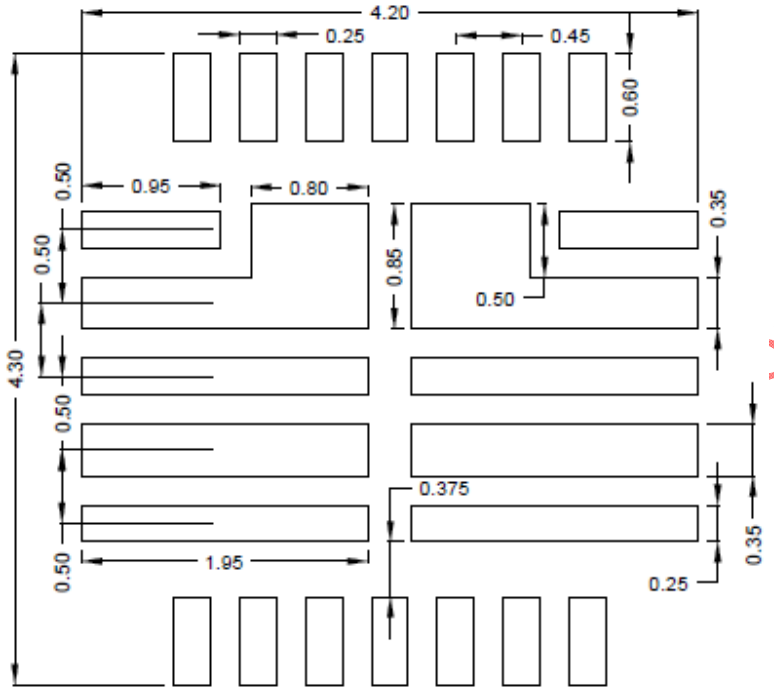
Top view



Side view



Bottom view



Recommended PCB layout
(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**