Application Notes: AN_SY7120

High Efficiency, 16V, 10A
Synchronous Step Up Regulator
Preliminary Specification

General Description

SY7120 develops a high efficiency, high power density synchronous Boost regulator. The device adopts adaptive constant off time and current mode control. The integrated low $R_{DS(ON)}$ switches minimize the conduction loss.

SY7120 provides selectable PFM/PWM light load operation mode. The device features cycle by cycle peak current limit. Low output voltage ripple and small external inductor and capacitor size are achieved with programmable pseudo-constant frequency.

Features

- Input Range: 2.8-16V
- Programmable Pseudo-constant Frequency: 300kHz-2MHz
- Low $R_{DS(ON)}$ for Internal Switch
  Main FET: 10mΩ
  Rectifier FET: 20mΩ
- PFM/PWM Selectable Light Load Operation Mode
- Internal Loop Compensation
- Programmable Peak Current Limit
- Internal Soft-start Time Limit the Inrush Current
- Input Voltage UVLO
- Over Temperature Protection
- Over Voltage Protection
- RoHS Compliant and Halogen Free
- Compact Package:QFN3×3-20

Ordering Information

SY7120 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY7120RAC	QFN3×3-20	--

Applications

- Power Bank
- High Power AP
- E-Cigarette
- Bluetooth Speaker

Typical Applications

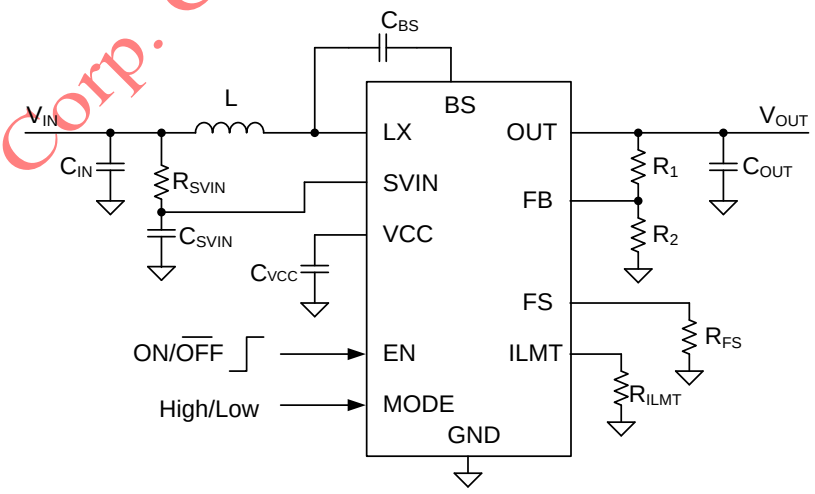
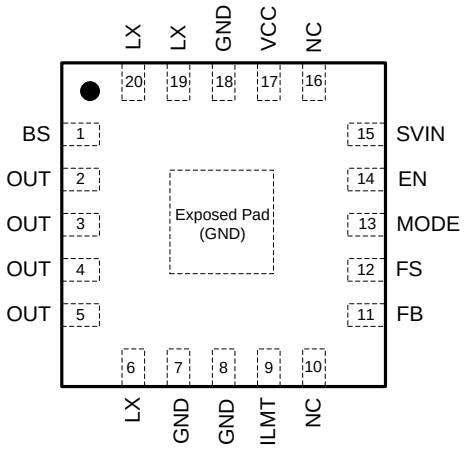


Figure1. Schematic Diagram

Pinout (top view)



(QFN3×3-20**)**

Top Mark: **BMF*xyz* for SY7120RAC (**device code: BMF, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
BS	1	Boost-strap pin. Supply Rectifier FET's gate driver. Decouple this pin to the LX pin with a 0.1μF ceramic capacitor
OUT	2,3,4,5	The Boost converter output pin.
LX	6,19,20	Inductor node. Connect an inductor from power input to the LX pin.
GND	7,8,18, EP	Ground pin of the IC.
ILMT	9	Switch peak current limit setting. Connect a resistor from this pin to GND. $I_{LMT}(A)=1200/R_{ILMT}(k\Omega)-2$
NC	10,16	Not connected.
FB	11	Feedback pin. Connected to the center of resistor voltage divider to program the output voltage: $V_{OUT}=1V\times(R_1/R_2+1)$
FS	12	Switching frequency setting pin. Connect a resistor from this pin to ground to program the switching frequency. $f_S(kHz) = 73565/R_{FS}(k\Omega)+300$
MODE	13	Operating mode selection under light load. Pull this pin low for PFM operation, and pull this pin high or leave it floating for PWM operation.
EN	14	Enable control. Pull high to turn on the IC. Do not leave it floating.
SVIN	15	IC power supply input pin. Decouple this pin to the GND pin with a 1μF ceramic capacitor.
VCC	17	Output of the internal regulator. Decouple this pin to the GND pin with a 1μF ceramic capacitor.

Block Diagram

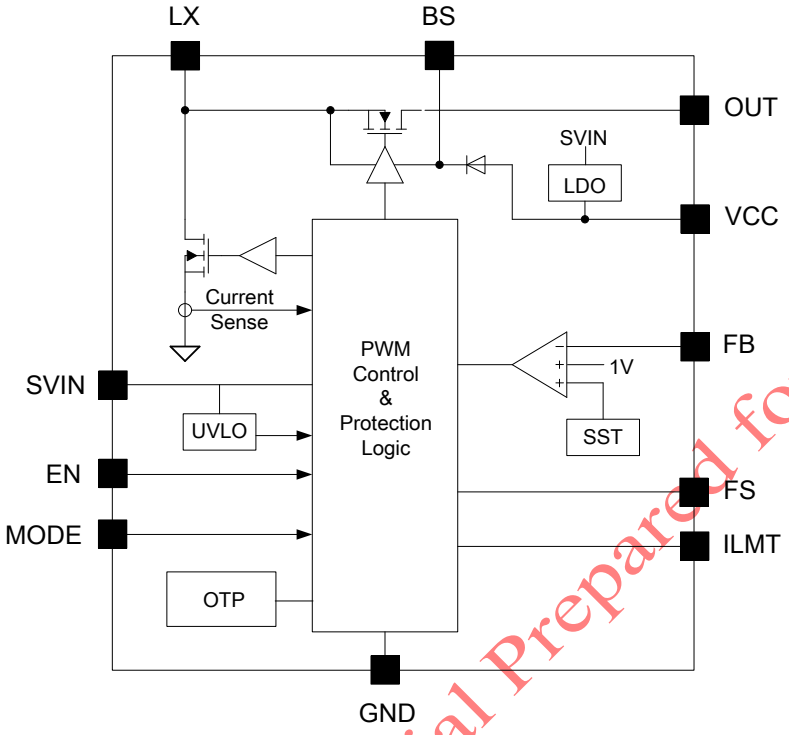


Figure2. Block Diagram

Absolute Maximum Ratings (Note 1)

SVIN, LX, OUT, ILMT, FS, MODE, EN ---------- 0.3V to 18V
FB, VCC ---------- 4V
BS-LX ---------- 4V
Power Dissipation, P_D @ T_A = 25℃ QFN3x3-20 ---------- TBD
Package Thermal Resistance (Note 2)
θ_{JA} ---------- TBD
θ_{JC} ---------- TBD
Junction Temperature Range ---------- -40℃ to 150℃
Lead Temperature (Soldering, 10 sec.) ---------- 260℃
Storage Temperature Range ---------- -65℃ to 150℃

Recommended Operating Conditions (Note 3)

SVIN ---------- 2.8V to 16V
Junction Temperature Range ---------- -40℃ to 125℃
Ambient Temperature Range ---------- -40℃ to 85℃

Electrical Characteristics

(V_{IN} =5V, V_{OUT}=12V, I_{OUT}=100mA, T_A = 25 ℃, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{SVIN}		2.8		16	V
Quiescent Current	I_Q	FB=1.1 V		200		μA
Shutdown Current	I_{SHDN}	EN=0			3.5	μA
FB Leakage Current	I_{FB}	V_{FB}=3.3V	-50		50	nA
Main N-FET RON	$R_{DS(ON)\_M}$			10		mΩ
Rectifier N-FET RON	$R_{DS(ON)\_R}$			20		mΩ
Feedback Reference Voltage	V_{REF}		0.99	1	1.01	V
SVIN UVLO Rising Threshold	$V_{SVIN,UVLO}$				2.8	V
SVIN UVLO Hysteresis	$V_{SVIN,HYS}$			0.2		V
Output OVP Threshold	$V_{OUT,OVP}$		16	17	18	V
Main N-FET Current Limit	I_{LMT}	R_{ILMT}=100kΩ	10			A
Main N-FET Current Limit Program Range	$I_{LMT,RNG}$		2		10	A
ILMT Reference Voltage	V_{ILMT}			0.6		V
EN/MODE Rising Threshold	$V_{EN/MODE,H}$				1.2	V
EN/MODE Falling Threshold	$V_{EN/MODE,L}$		0.4			V
Switching Frequency Program Range	$f_{SW,RNG}$		300		2000	kHz
Switching Frequency Accuracy	f_{SW}	R_{FS}=340kΩ	400	500	600	kHz
Minimum ON Time	$t_{ON,MIN}$			130		ns
Minimum OFF Time	$t_{OFF,MIN}$			80		ns
Thermal Shutdown Temperature	T_{SD}			150		℃
Thermal Shutdown Hysteresis	T_{HYS}			15		℃

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

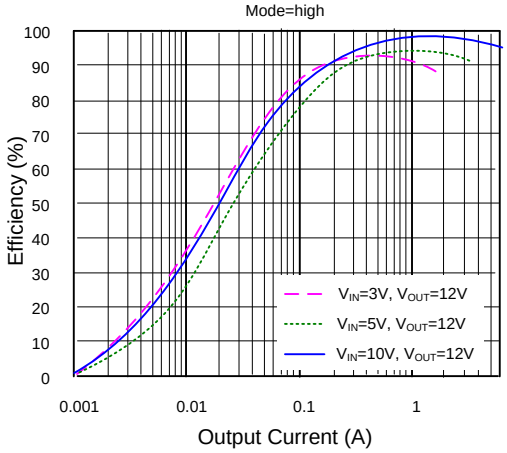
Note 2: θ_{JA} is measured in the natural convection at T_A = 25 ℃ on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Paddle of QFN3x3-20 package is the case position for θ_{JC} measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

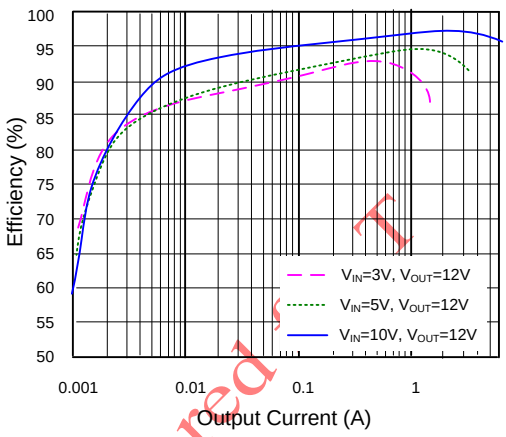
Efficiency vs. Load Current

Mode=high



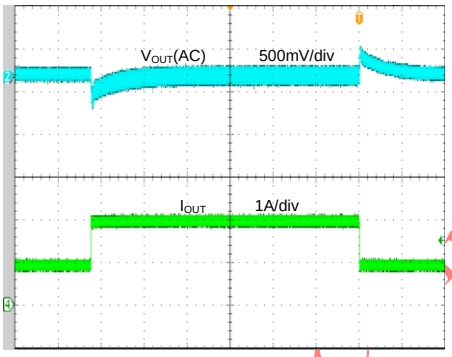
Efficiency vs. Load Current

Mode=low



Load Transient

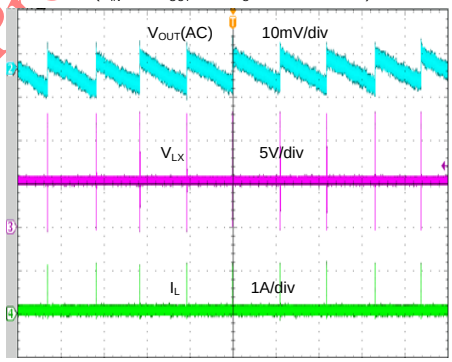
(V_{IN}=5V, V_{OUT}=12V, I_O=1 ~ 2A)



Time (200μs/div)

Output Ripple

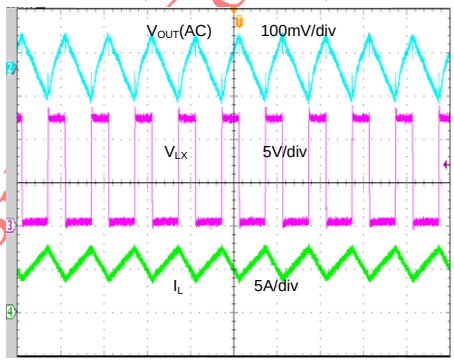
(V_{IN}=5V, V_{OUT}=12V, I_O=0A, Mode=Low)



Time (800μs/div)

Output Ripple

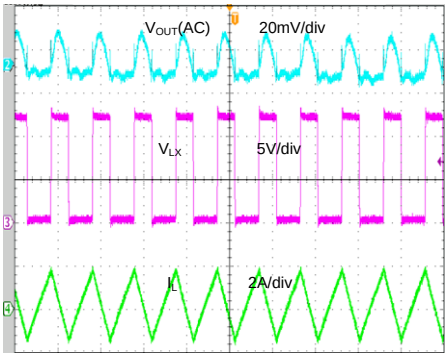
(V_{IN}=5V, V_{OUT}=12V, I_O=2A)



Time (2μs/div)

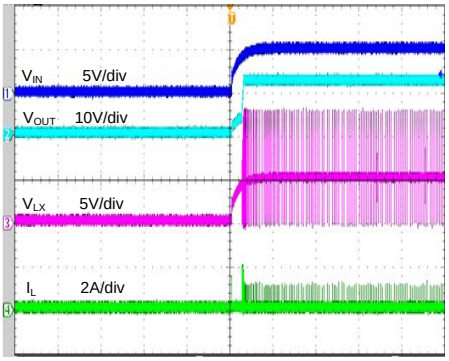
Output Ripple

(V_{IN}=5V, V_{OUT}=12V, I_O=0A, Mode=High)



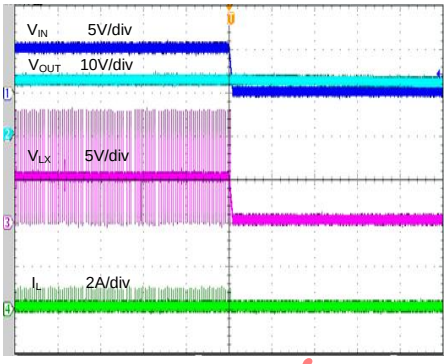
Time (2μs/div)

Startup from V_{IN}
(V_{IN}=5V, V_{OUT}=12V, I_O=0A, Mode=Low)



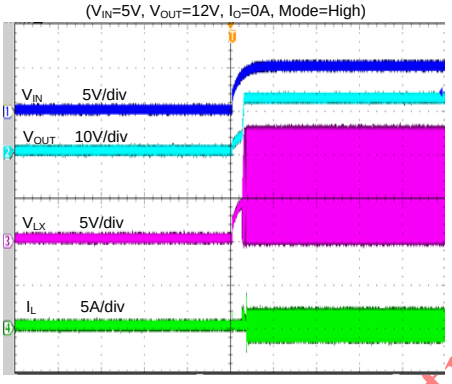
Time (20ms/div)

Shutdown from V_{IN}
(V_{IN}=5V, V_{OUT}=12V, I_O=0A, Mode=Low)



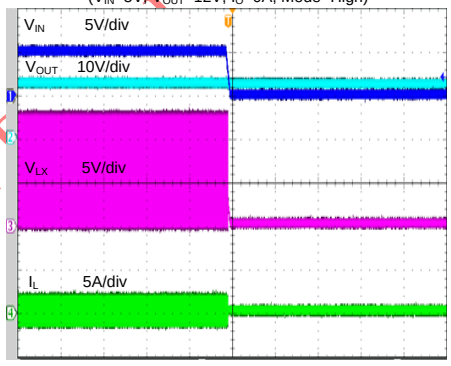
Time (20ms/div)

Startup from V_{IN}
(V_{IN}=5V, V_{OUT}=12V, I_O=0A, Mode=High)



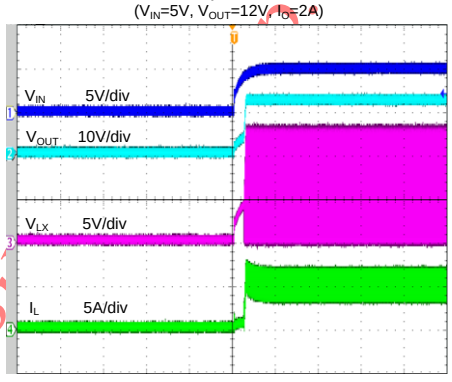
Time (20ms/div)

Shutdown from V_{IN}
(V_{IN}=5V, V_{OUT}=12V, I_O=0A, Mode=High)



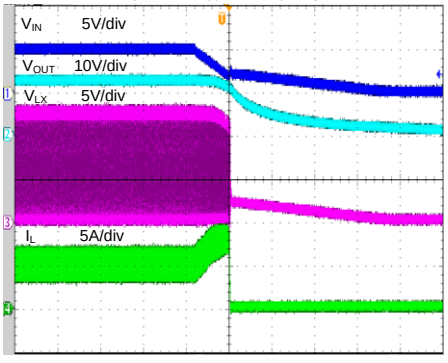
Time (10ms/div)

Startup from V_{IN}
(V_{IN}=5V, V_{OUT}=12V, I_O=2A)



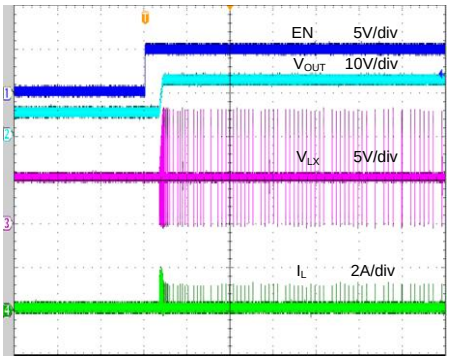
Time (20ms/div)

Shutdown from V_{IN}
(V_{IN}=5V, V_{OUT}=12V, I_O=2A)



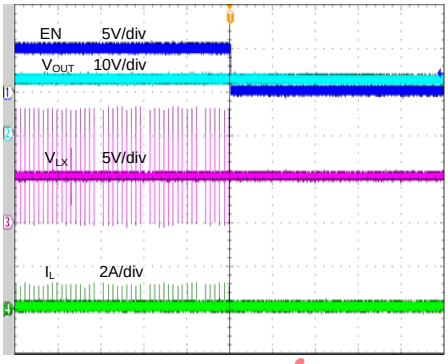
Time (200μs/div)

Startup from Enable
(V_{IN}=5V, V_{OUT}=12V, I_O=0A, Mode=Low)



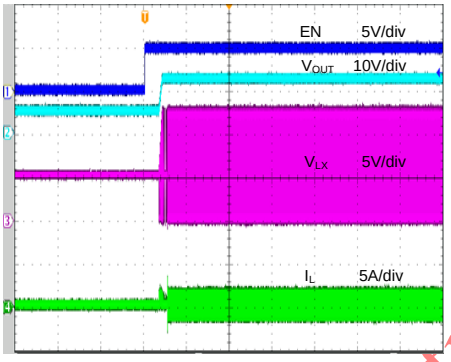
Time (10ms/div)

Shutdown from Enable
(V_{IN}=5V, V_{OUT}=12V, I_O=0A, Mode=Low)



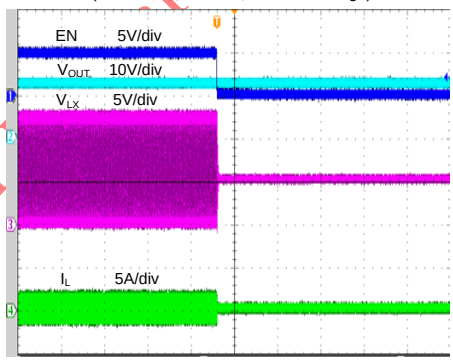
Time (10ms/div)

Startup from Enable
(V_{IN}=5V, V_{OUT}=12V, I_O=0A, Mode=High)



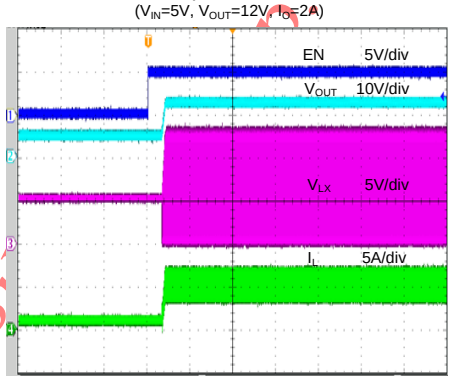
Time (10ms/div)

Shutdown from Enable
(V_{IN}=5V, V_{OUT}=12V, I_O=0A, Mode=High)



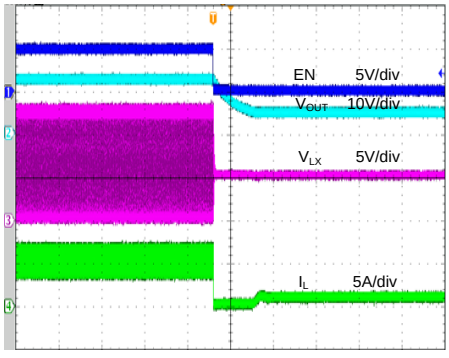
Time (10ms/div)

Startup from Enable
(V_{IN}=5V, V_{OUT}=12V, I_O=2A)



Time (10ms/div)

Shutdown from Enable
(V_{IN}=5V, V_{OUT}=12V, I_O=2A)



Time (200μs/div)

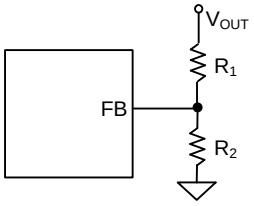
Applications Information

Because of the high integration in SY7120, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, output current limit resistor R_{LIM}, switching frequency program resistor R_{FS}, inductor L and feedback resistors (R_1 and R_2) need to be selected for the targeted applications.

Feedback Resistor Divider R_1 and R_2

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light load, it is desirable to choose large resistance values for both R_1 and R_2. A value between 10k and 1M is recommended for both resistors. If R_1=200k is chosen, then R_2 can be calculated to be:

$$R_2 = \frac{R_1}{V_{OUT} - 1}(\Omega)$$



Input Capacitor C_{IN}

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = \frac{V_{IN} \cdot (V_{OUT} - V_{IN})}{2\sqrt{3} \cdot L \cdot F_{SW} \cdot V_{OUT}}(A)$$

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the VIN and PGND pin. Care should be taken to minimize the loop area formed by C_{IN}, VIN, and PGND pin. In this case, a 10μF low ESR ceramic capacitor is recommended.

The SVIN capacitor must be close to the SVIN and SGND pins to minimize the potential noise problem. Care should be taken to minimize the loop area formed by C_{SVIN}, and SVIN/GND pins. In this case a 1uF low ESR ceramic is recommended.

Output Capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into account when selecting these capacitors. For the best performance, it is recommended to use X5R or better grade ceramic capacitor with 25V rating and more than 44μF capacitors.

Boost Lnductor L

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum average input current. The inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{(V_{OUT} - V_{IN})}{F_{SW} \times I_{OUT\_MAX} \times 40\%}(H)$$

Where F_{SW} is the switching frequency and I_{OUT_MAX} is the maximum load current.

SY7120 is less sensitive to the ripple current variations. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of an inductor must be selected to guarantee an adequate margin to the peak inductor current under full load conditions.

$$I_{SAT\_MIN} > \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT\_MAX} + \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{(V_{OUT} - V_{IN})}{2 \times F_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<10mohm to achieve a good overall efficiency.

Switching Frequency

The switching frequency of SY7120 in CCM can be programmed by adjusting external resistor R_{FS} connected to FS pin:

F_{SW} (kHz)= 73565/R_{FS}(kohm) +300

Under PFM light load condition, SY7120 linearly fold back the frequency, thus minimize the output ripple.

Enable Operation

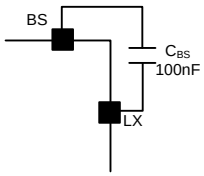
Pulling the EN pin low (<0.4V) will shut down the device. Driving the EN pin high (>1.2V) will turn on the IC again.

Light Load Operation Mode Selection

PFM or PWM light load operation is selected by MODE pin. Pull MODE pin low (<0.4V) for PFM operation, and pull this pin high (>1.2V) for PWM operation.

External Bootstrap Capacitor

This capacitor provides the gate driver voltage for internal rectifier. A 100nF low ESR ceramic capacitor connected between BS pin and LX pin is recommended.



Peak Current Limit Setting

The peak current limit can be programmed with a resistor R_{ILMT} connecting from ILMT pin to ground: $I_{LIM}(A)=1200/R_{LIM}(Kohm)-2$

Layout Design

The layout design of SY7120 is highly simplified. To achieve a higher efficiency and better noise immunity, following components should be placed close to the IC: C_{IN}, C_{SVIN}, C_{OUT}, L, R_1 and R_2.

1) It is desirable to maximize the PCB copper area connected to GND pin to achieve a better thermal performance and noise immunity. If the board space allowed, a designated ground plane layer is highly recommended.

2) C_{SVIN} must be close to SVIN and GND pins. The loop area formed by C_{OUT}, LX and GND pins must be minimized.

3) C_{OUT} must be close to OUT and GND pins. The loop area formed by C_{OUT}, LX and GND pins must be minimized.

4) The PCB copper area associated with LX pin must be minimized to improve the noise immunity.

5) The components R_1 and R_2 and the trace connecting to the FB pin must NOT be adjacent to the LX node on the PCB layout to minimize the noise coupling to FB pin.

6) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the SVIN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1MΩ resistor across the EN and SGND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

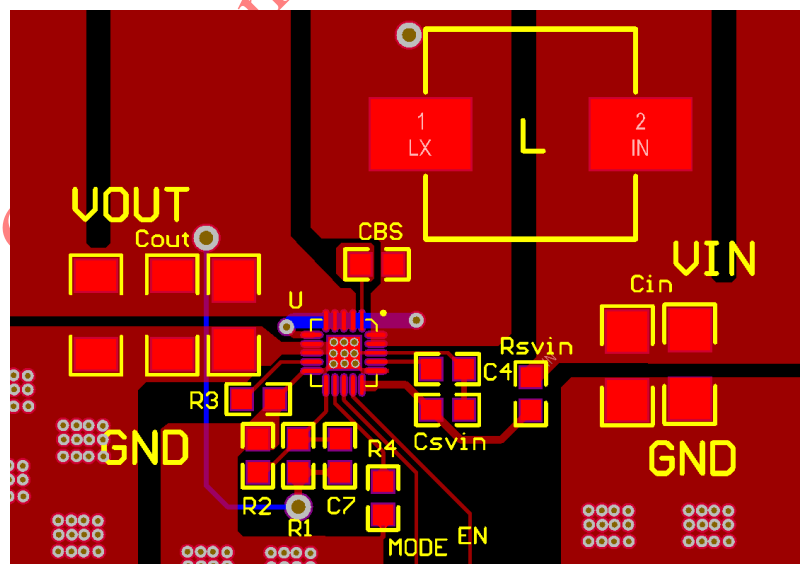
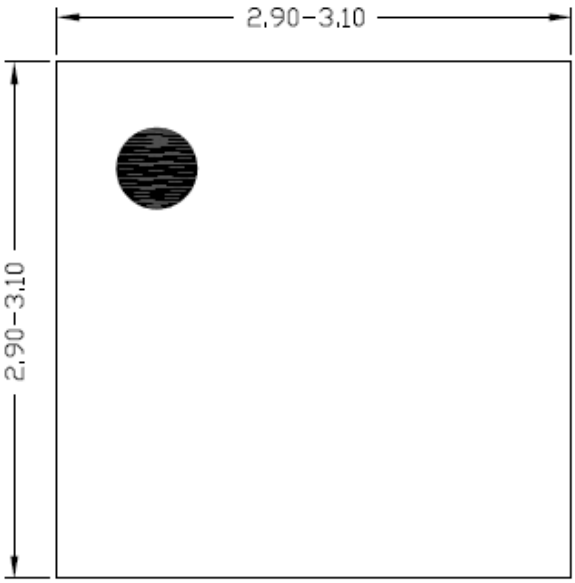
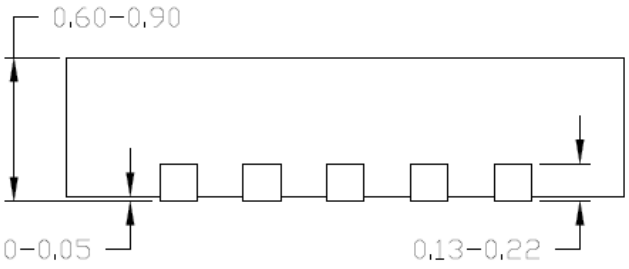


Figure3. PCB Layout Suggestion

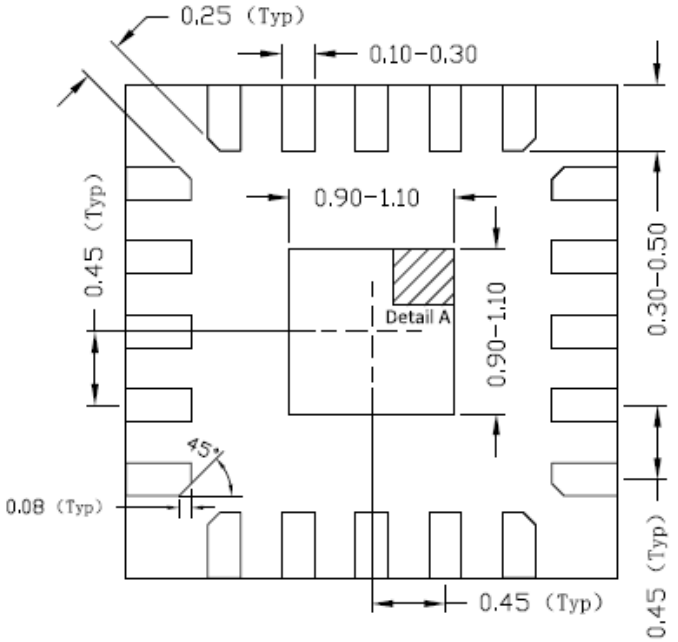
QFN3×3-20 Package Outline

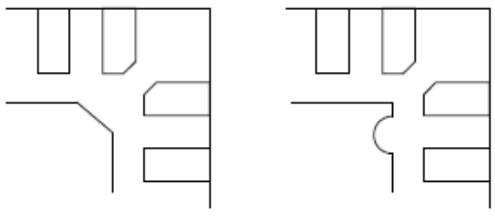


Top view



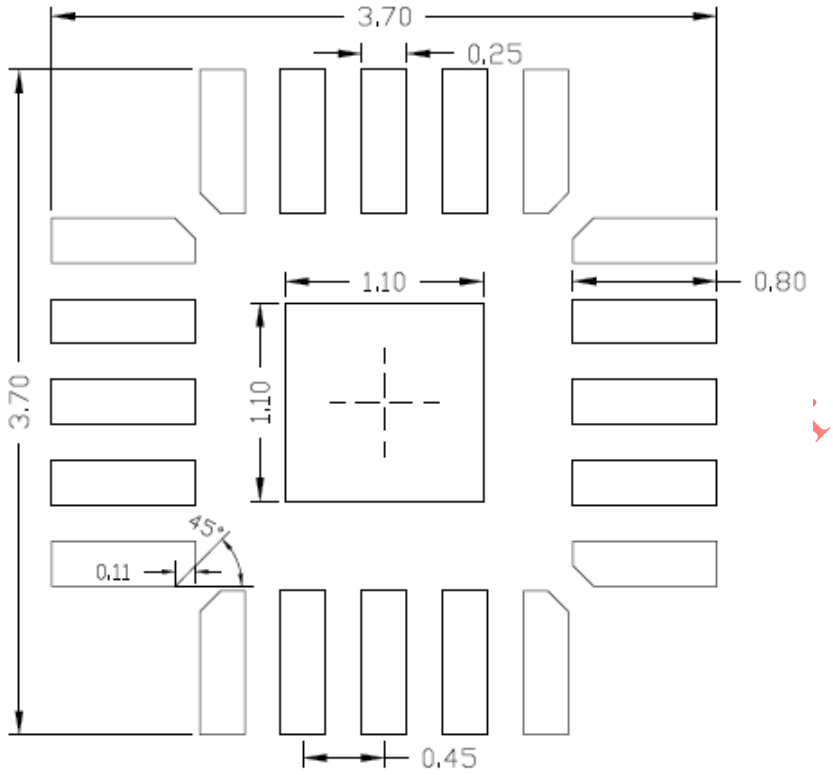
Side view





Detail A
Pin1 Identifier: two options

Bottom view



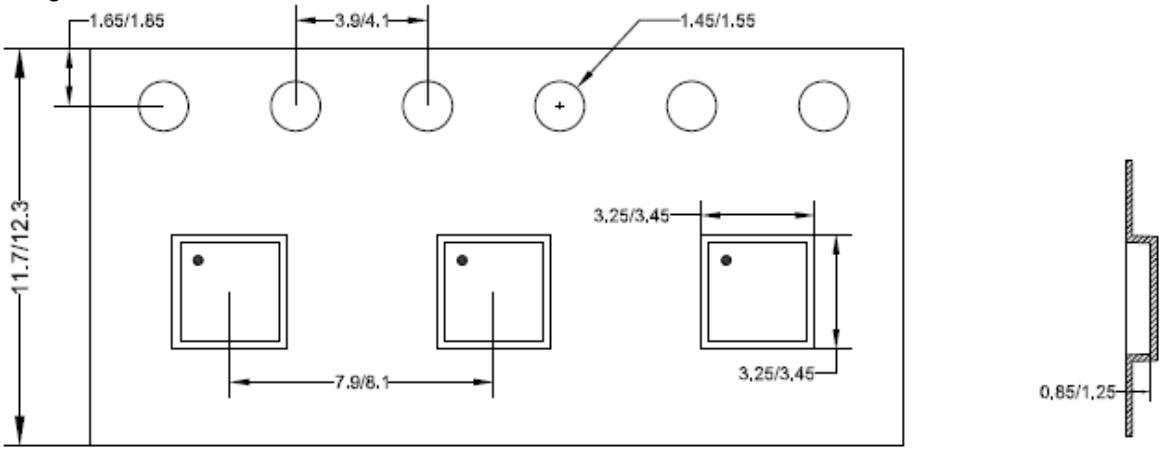
Recommended PCB layout
(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

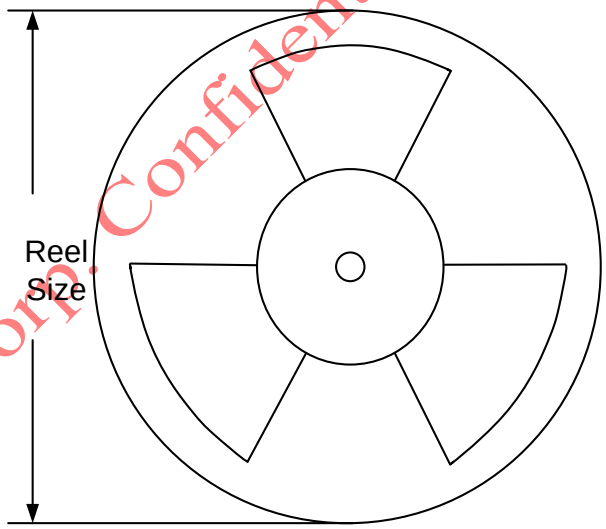
1. Taping orientation

QFN3×3



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3x3	12	8	13"	400	400	5000

3. Others: NA