



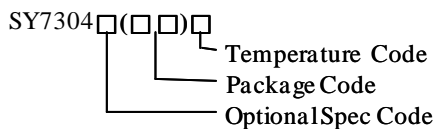
# Applications Note:SY7304

## High Efficiency 33V, 4A, 1MHz Step Up Regulator

### General Description

The SY7304 is a high efficiency, current-mode control Boost regulator. The device integrates a 120mΩ low  $R_{DS(ON)}$  N-channel MOSFET for high efficiency. The fixed 1MHz switching frequency and internal compensation reduce external components size and count. The build-in internal soft start circuitry minimizes the inrush current at start-up. The SY7304 is available in compact DFN3×3-10 package.

### Ordering Information



Ordering Number	Package type	Note
SY7304DBC	DFN3×3-10	4A

### Features

- Wide input range: 3-33V
- Maximum output voltage: 33V
- 1MHz switching frequency
- Integrated 120 mΩ  $R_{DS(ON)}$  switch with 4A peak current capability
- Internal soft-start
- 0.6V ±2% reference voltage
- Cycle by cycle peak current limit
- Over temperature protection
- RoHS Compliant and Halogen Free
- Compact package: DFN3×3-10

### Applications

- Portable Device
- Battery Powered System
- Networking cards powered from PCI or PCI-express slots

### Typical Applications

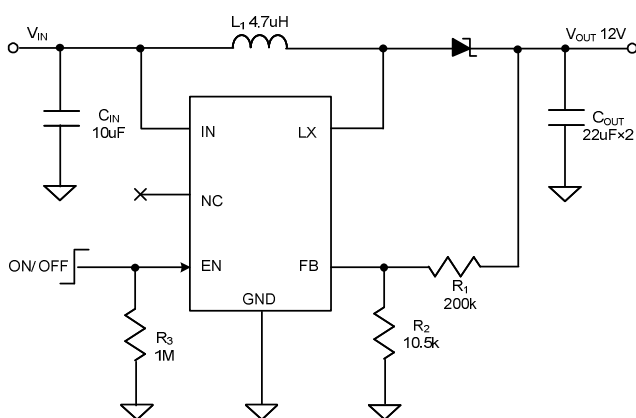


Figure 1. Schematic Diagram

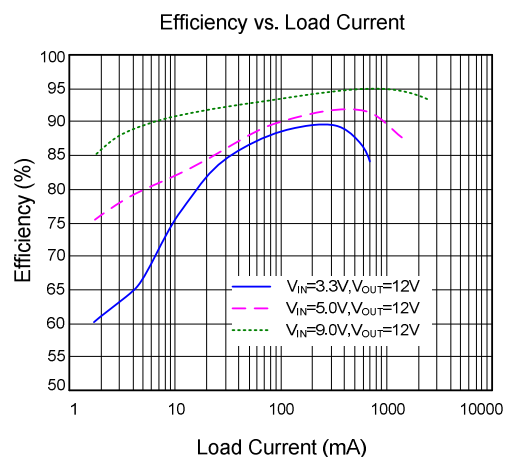
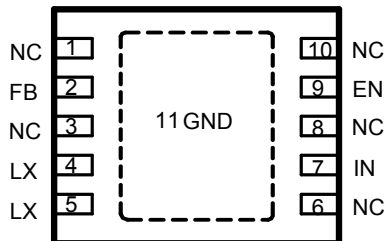


Figure 2. Efficiency vs. Load Current



**Pinout (top view)**



(DFN3×3-10)

**Top Mark:** VLxyz (Device code: VI, x=year code, y=week code, z= lot number code)

Pin Name	Pin Number	Pin Description
IN	7	Input pin. Decouple this pin to GND pin with 1uF ceramic cap.
GND	11	Ground pin
LX	4,5	Inductor node. Connect an inductor between IN pin and LX pin.
FB	2	Feedback pin. Connect a resistor R1 between V <sub>OUT</sub> and FB, and a resistor R2 between FB and GND to program the output voltage: V <sub>OUT</sub> =0.6V*(R1/R2+1).
EN	9	Enable control. High to turn on the part. Don't leave it floated.
NC	1,3,6,8,10	No connection.

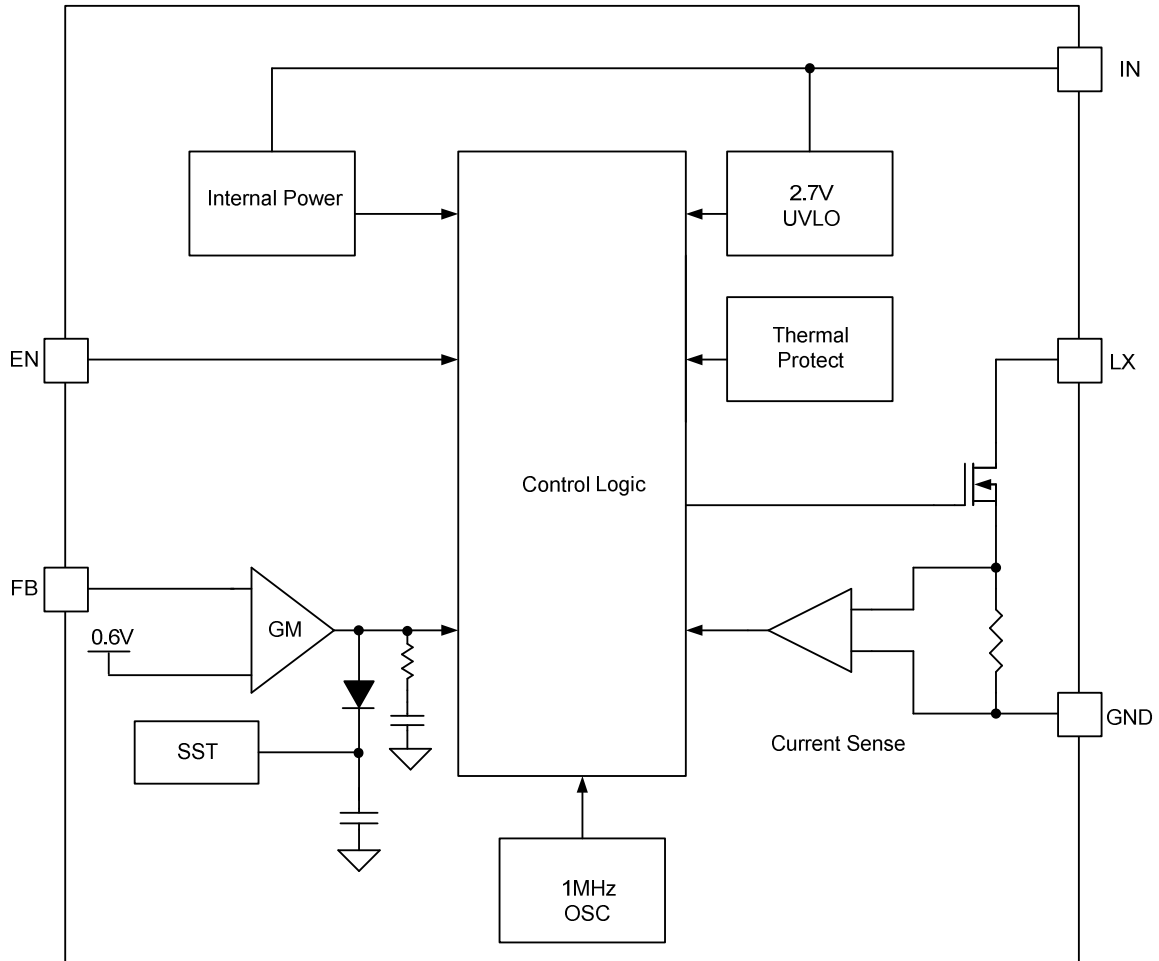
**Absolute Maximum Ratings** (Note 1)

LX, IN, EN	-----	-0.3V to 36V
FB	-----	-0.3V to 4V
Power Dissipation, P <sub>D</sub> @ T <sub>A</sub> = 25°C DFN3×3-10	-----	2.6W
Package Thermal Resistance (Note 2)		
θ <sub>JA</sub>	-----	38°C/W
θ <sub>JC</sub>	-----	8°C/W
Junction Temperature Range	-----	-40 to 150°C
Lead Temperature (Soldering, 10 sec.)	-----	260°C
Storage Temperature Range	-----	-65°C to 150°C
Dynamic LX voltage in 50ns duration	-----	IN+3V to GND-4V

**Recommended Operating Conditions** (Note 3)

IN	-----	3V to 33V
Junction Temperature Range	-----	-40°C to 125°C
Ambient Temperature Range	-----	-40°C to 85°C

## Block Diagram





## Electrical Characteristics

( $V_{IN} = 5V$ ,  $V_{OUT} = 12V$ ,  $I_{OUT} = 100mA$ ,  $T_A = 25^\circ C$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	$V_{IN}$		3		33	V
Quiescent Current	$I_Q$	$V_{FB} = 0.66V$		100		$\mu A$
Shutdown Current	$I_{SHDN}$	EN=0			15	$\mu A$
Low Side Main FET $R_{ON}$	$R_{DS(ON)}$			120		m $\Omega$
Main FET Current Limit	$I_{LIM}$	Duty cycle=80%	4		6	A
Switching Frequency	F <sub>SW</sub>		0.8	1	1.2	MHz
Feedback Reference Voltage	$V_{REF}$		0.588	0.6	0.612	V
FB Pin Input Current	$I_{FB}$		-50		50	nA
IN UVLO Rising Threshold	$V_{IN,UVLO}$				2.7	V
UVLO Hysteresis	$U_{VLO,HYS}$			0.1		V
EN Rising Threshold	$V_{ENH}$		2			V
EN Falling Threshold	$V_{ENL}$				0.4	V
Max Duty Cycle	D <sub>max</sub>			90		%
Thermal Shutdown Temperature	$T_{SD}$			150		$^\circ C$
Thermal Recovery Hysteresis	$T_{HYS}$			15		$^\circ C$

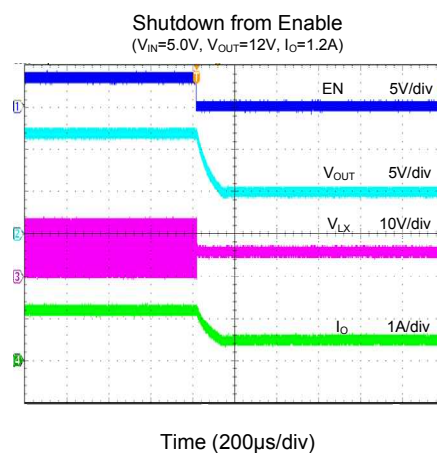
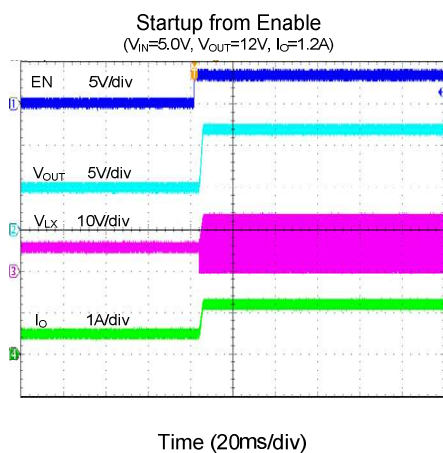
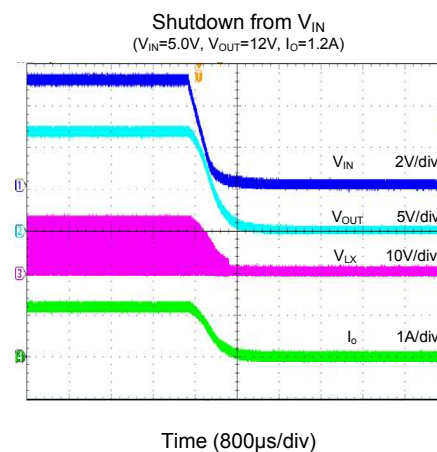
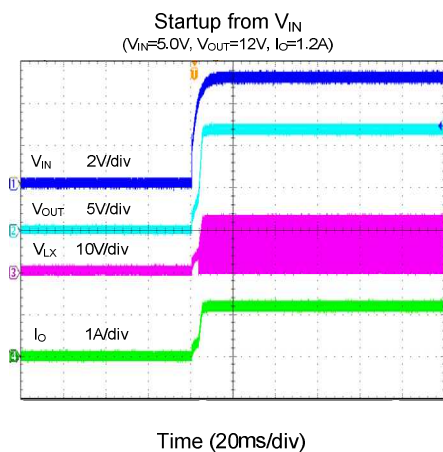
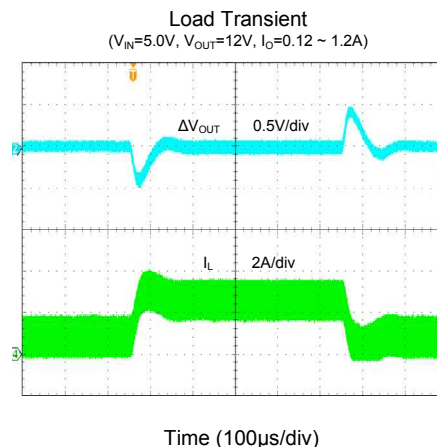
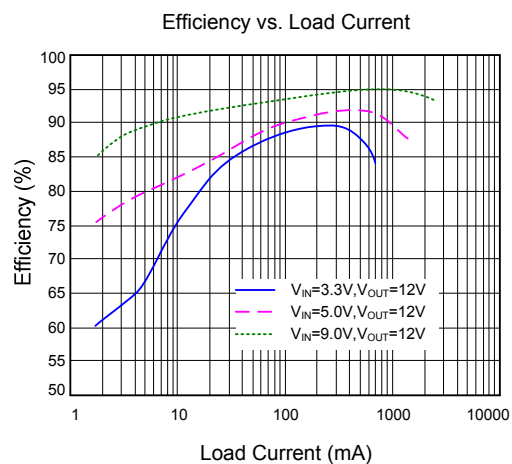
**Note 1:** Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

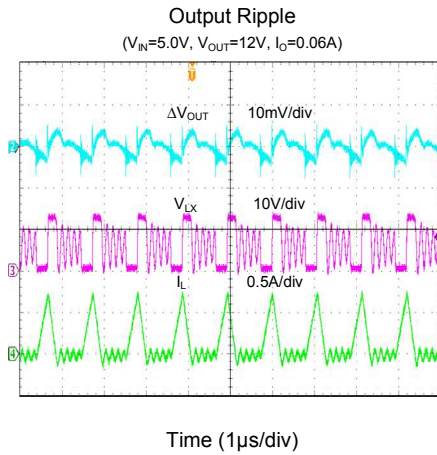
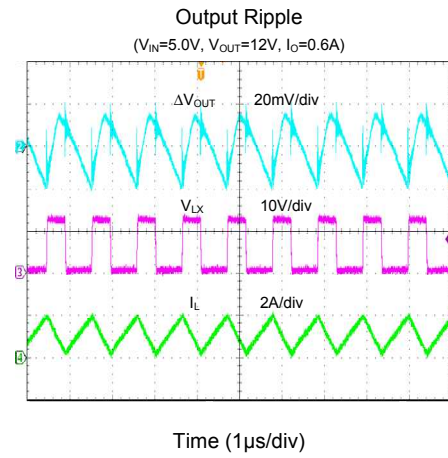
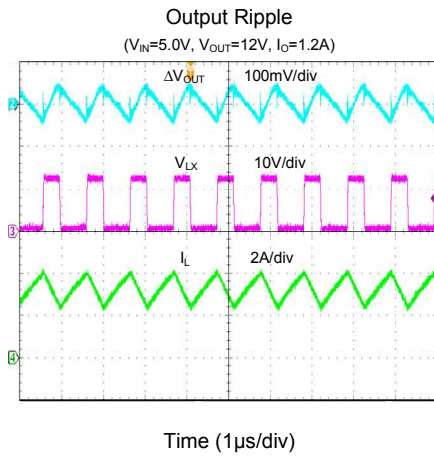
**Note 2:**  $\theta_{JA}$  is measured in the natural convection at  $T_A = 25^\circ C$  on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2” x 2” FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

**Note 3:** The device is not guaranteed to function outside its operating conditions.



## Typical Performance Characteristics







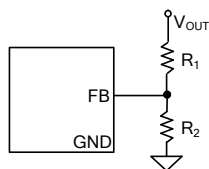
## Applications Information

Because of the high integration in SY7304, the application circuit based on this regulator IC is rather simple. Only input capacitor  $C_{IN}$ , output capacitor  $C_{OUT}$ , inductor  $L$  and feedback resistors ( $R_1$  and  $R_2$ ) need to be selected for the targeted applications.

### Feedback resistor divider $R_1$ and $R_2$

Choose  $R_1$  and  $R_2$  to program the proper output voltage. To minimize the power consumption under light load, it is desirable to choose large resistance values for both  $R_1$  and  $R_2$ . A value between 10k and 1M is recommended for both resistors. If  $R_1=200k$  is chosen, then  $R_2$  can be calculated to be:

$$R_2 = \frac{0.6R_1}{V_{OUT} - 0.6} (\Omega)$$



### Input capacitor $C_{IN}$

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = \frac{V_{IN} \cdot (V_{OUT} - V_{IN})}{2\sqrt{3} \cdot L \cdot F_{SW} \cdot V_{OUT}} (A)$$

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by  $C_{IN}$ , and IN/GND pins. A low ESR ceramic capacitor with greater than 10uF capacitance is recommended.

### Output capacitor $C_{OUT}$

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into account when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor with greater than 22uF capacitance.

### Boost inductor $L$

There are several considerations in choosing this inductor.

- 1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum average input current. The inductance is calculated as:

$$L = \left( \frac{V_{IN}}{V_{OUT}} \right)^2 \frac{(V_{OUT} - V_{IN})}{F_{SW} \times I_{OUT\_MAX} \times 40\%} (H)$$

where  $F_{SW}$  is the switching frequency and  $I_{OUT\_MAX}$  is the maximum load current.

SY7304 regulator IC is less sensitive to the ripple current variations. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

- 2) The saturation current rating of an inductor must be selected to guarantee an adequate margin to the peak inductor current under full load conditions.

$$I_{SAT\_MIN} > \left( \frac{V_{OUT}}{V_{IN}} \right) \times I_{OUT\_MAX} + \left( \frac{V_{IN}}{V_{OUT}} \right)^2 \frac{(V_{OUT} - V_{IN})}{2 \times F_{SW} \times L}$$

- 3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with  $DCR < 10m\Omega$  to achieve a good overall efficiency.

### Enable Operation

Pulling the EN pin low (<0.4V) will shut down the device. During the shut down mode, the SY7304 shut down current drops to lower than 15uA. Driving the EN pin high (>2V) will turn on the IC again.

### Rectifier Diode Selection

Schottky diode is a good choice for high efficiency operation because of its low forward voltage drop and fast reverse recovery. The maximum current rating of the diode must be higher than maximum input current. And the average current rating of the diode must be higher than the output current.

### Layout Design

The layout design of SY7304 regulator is highly simplified. To achieve a higher efficiency and better noise immunity, following components should be placed close to the IC:  $C_{IN}$ ,  $L$ ,  $R_1$  and  $R_2$ .

- 1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve better thermal



performance and noise immunity. If the board space allowed, a designated ground plane layer is highly recommended.

2)  $C_{IN}$  must be close to IN and GND pins. The loop area formed by  $C_{OUT}$ , LX and GND pins must be minimized.

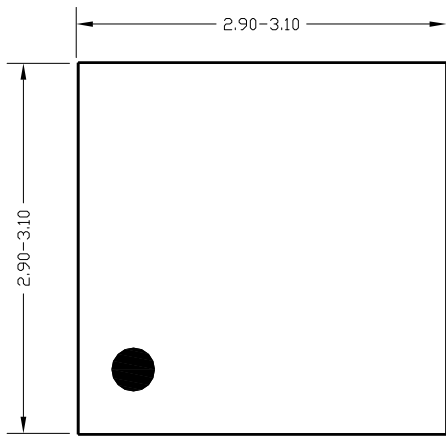
3) The PCB copper area associated with LX pin must be minimized to improve the noise immunity.

4) The components  $R_1$  and  $R_2$ , and the trace connecting to the FB pin must NOT be adjacent to the LX node on the PCB layout to minimize the noise coupling to FB pin.

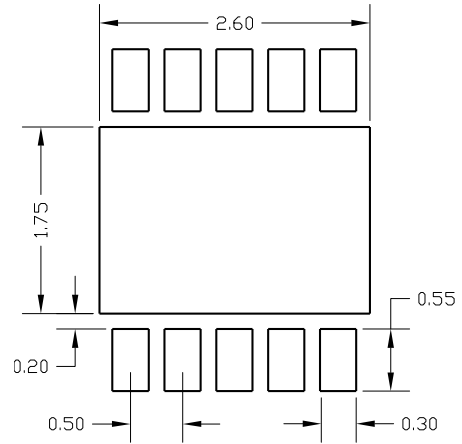
5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down  $1M\Omega$  resistor across the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.



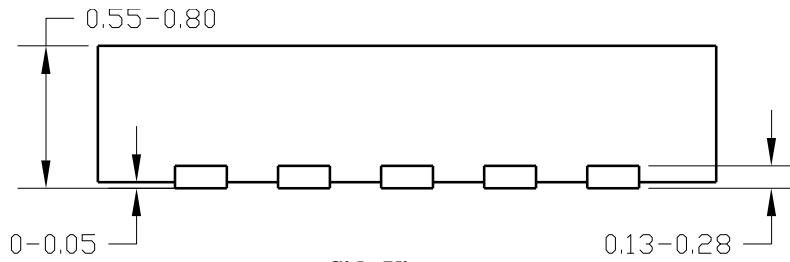
**DFN3x3-10 Package outline**



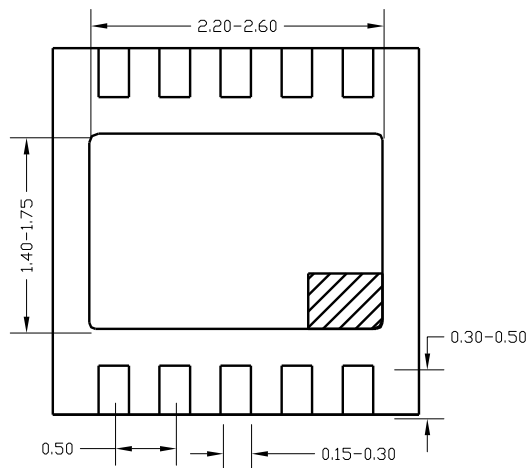
**Top View**



**PCB layout (recommended)**



**Side View**



**Bottom View**

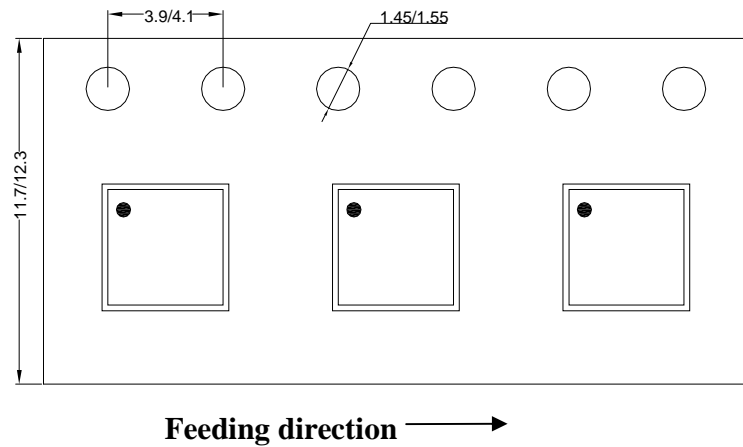


**Detail A**  
 Pin1 identifier: two options

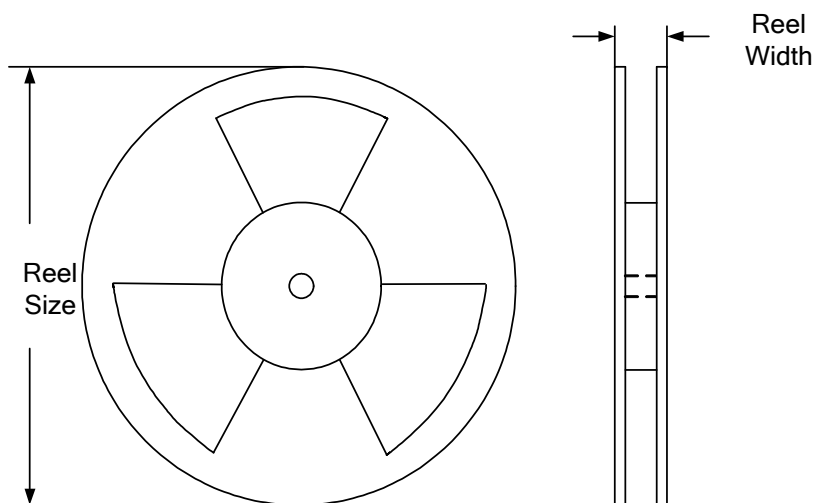
**Notes: All dimensions are in millimeters and exclude mold flash & metal burr.**

## Taping & Reel Specification

### 1. DFN3x3-10 taping orientation



### 2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Reel width(mm)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN3x3	10	8	13"	12.4	400	400	5000

### 3. Others: NA