SY7636A

PMIC for Electronic Paper Display

General Description

The SY7636A is a single-chip power management IC (PMIC) designed for electronic paper display (EPD) applications, and the device supports panel sizes up to 9.7 inches and greater. The device integrates two high efficiency DC/DC Boost converters that are boosted to 25V and –20V by two charge pumps to provide the gate driver supply for panels. Two tracking LDOs create ±15V source driver supplies that support up to 200mA of output current. SY7636A also provides an I²C interface control for specific panel requirements.

Ordering Information

SY7636 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package Type	Note
SY7636ARMC	QFN6×6-48	----

Key Features

- 2.9V to 5.5V Input Voltage Range
- Boost Converter VP for the Power Input of Positive Rails
- Inverting Buck-Boost converter VN for the Power Input of Negative Rails
- Two Adjustable LDOs for Source Driver Supply
  - VPOS: 15 V, 200mA
  - VNEG: –15 V, 200mA
  - Accurate Output Voltage Tracking: VPOS+VNEG = ±50 mV
- Two Charge Pumps for Gate Driver Supply
  - VDDH: 25 V, 10mA (Up to 29V)
  - VEE: –20 V, 15mA (Down to -25V)
- Adjustable VCOM Driver for Accurate Panel-Backplane Biasing
  - 0 V to –5V
  - ± 1.5% Accuracy (±10 mV)
  - 9-Bit Control (10-mV Nominal Step Size)
- Internal Active Discharge for VPOS, VNEG, VDDH, and VCOM
- Differential Temperature Sense Input and Digital Temperature Reporting
- I²C Compatible Interface
- Protection: UVLO, OTP, OCP, SCP, UVP
- RoHS Compliant and Halogen Free
- Compact package: QFN6×6-48

Applications

- Power Supply for Active Matrix Panels
- EPD Power Supplies
- E-Book Readers

Typical Applications

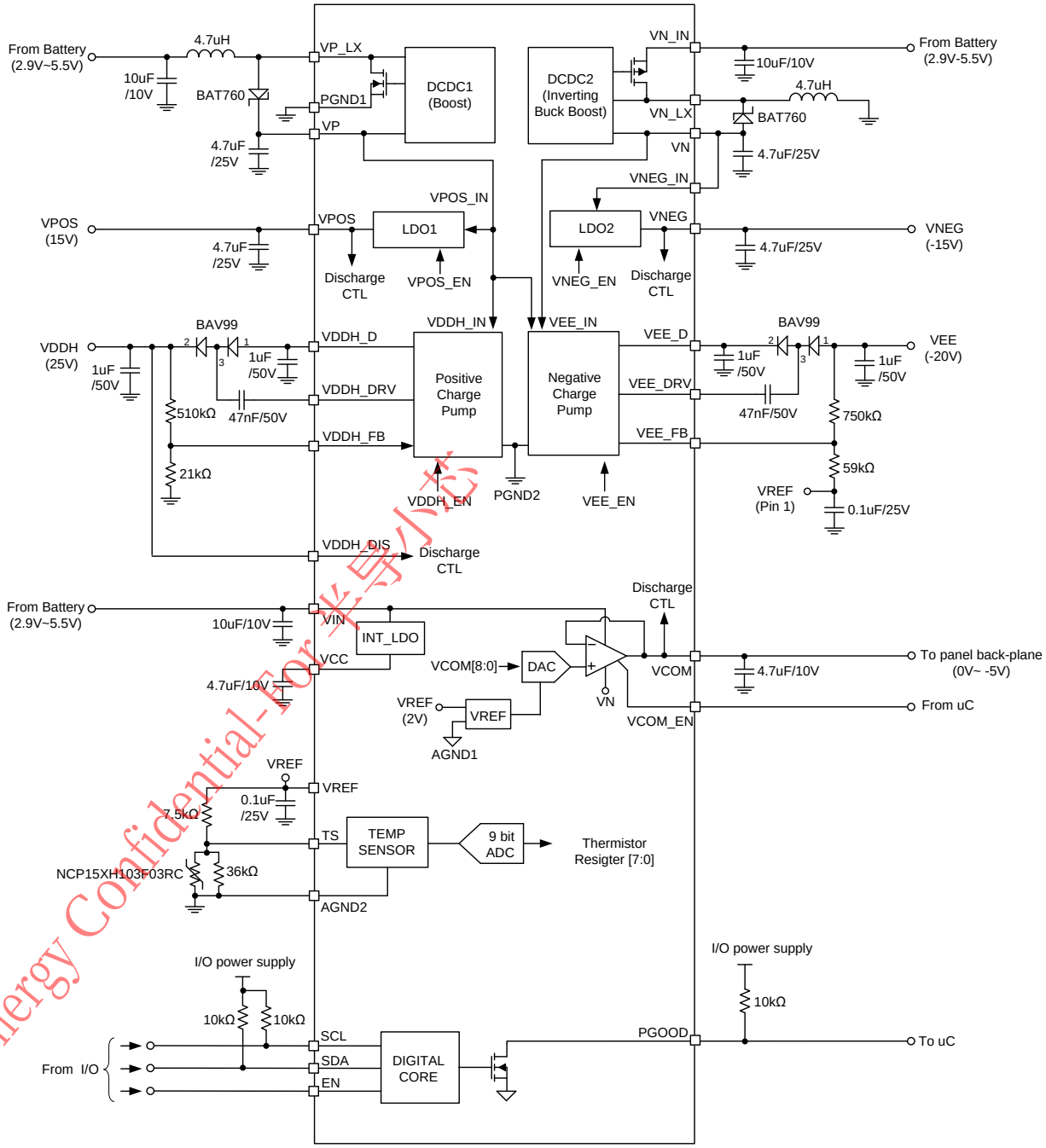
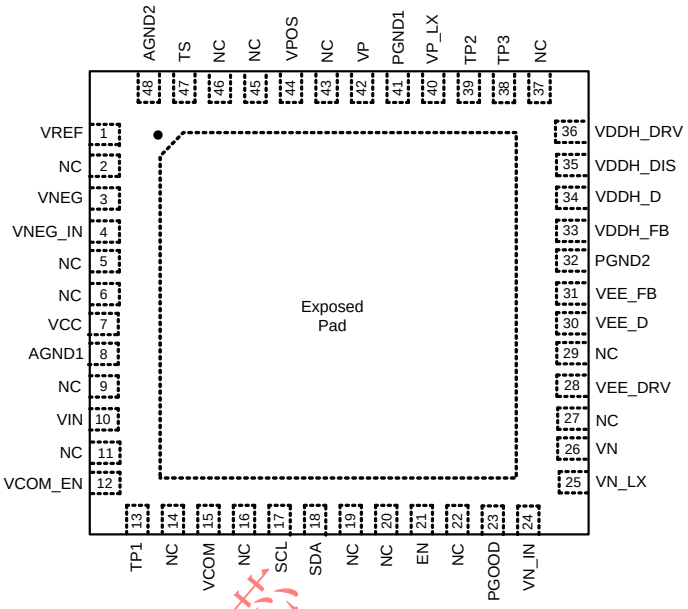


Figure 1. Typical Application Circuit & Function Block Diagram.

Pinout (top view)



(QFN 6×6-48)

Top Mark: BWN*xyz* (device code: BWN, ***x=year code, y=week code, z=lot number code***)

Pin Name	Pin Number	Pin Description
VREF	1	Filter pin for 2V internal reference for temperature sense pull-high voltage. The filter capacitor on this pin is limited to 0.1uF.
NC	2	Not internally connected.
VNEG	3	Negative supply output pin for panel source drivers. Discharge VNEG to ground whenever the rail is disabled.
VNEG_IN	4	Input power supply to VNEG rail.
NC	5	Not internally connected.
NC	6	Not internally connected.
VCC	7	Filter pin for 3.3V internal supply.
AGND1	8	Analog ground for general analog circuitry.
NC	9	Not internally connected.
VIN	10	Input power supply to general circuitry.
NC	11	Not internally connected.
VCOM_EN	12	VCOM enable pin when VCOMCTL[0]=1. Pull this pin high to enable the VCOM amplifier. When pin is pulled low and VN is enabled, VCOM discharge is enabled.
TP1	13	This pin is no application definition. This pin needs to set floating.
NC	14	Not internally connected.
VCOM	15	Filter pin for panel common-voltage driver. Discharge VCOM to ground whenever the rail is disabled.
NC	16	Not internally connected.
SCL	17	Serial interface (I^2C) clock input.
SDA	18	Serial interface (I^2C) data input/output.

NC	19	Not internally connected.
NC	20	Not internally connected.
EN	21	Power-up pin with internal pull low resistor (200kΩ). Pull this pin high to power up all output rails. Moreover, after power off controlled by I^2C , pull this pin being low can reset register being default value and clear reporting register (including fault register and thermistor register).
NC	22	Not internally connected.
PGOOD	23	Open-drain power good output pin. Pin is pulled low when one or more rails are disabled or not in regulation. VCOM have no effect on this pin.
VN_IN	24	Input power supply to inverting buck-boost converter (VN).
VN_LX	25	Switch out of inverting buck-boost converter (VN).
VN	26	Feedback pin for inverting buck-boost converter (VN) and supply for VNEG rail and VEE rail.
NC	27	Not internally connected.
VEE_DRV	28	Driver output pin for negative charge pump (VEE).
NC	29	Not internally connected.
VEE_D	30	Base voltage output pin for negative charge pump (VEE).
VEE_FB	31	Feedback pin for negative charge pump (VEE). The lower divider resistor is connected to VREF(2V). The filter capacitor on VREF is limited to 0.1uF.
PGND2	32	Power ground for VDDH and VEE charge pumps.
VDDH_FB	33	Feedback pin for positive charge pump (VDDH).
VDDH_D	34	Base voltage output pin for positive charge pump (VDDH).
VDDH_DIS	35	Discharge pin for VDDH. Connect to VDDH to discharge VDDH to ground whenever the rail is disabled. Leave floating if discharge function is not desired.
VDDH_DRV	36	Driver output pin for positive charge pump (VDDH).
NC	37	Not internally connected.
TP3	38	Reserved pin for function extension.
TP2	39	This pin is no application definition. This pin needs to set floating.
VP_LX	40	Switch out of boost converter (VP).
PGND1	41	Power ground for boost converter (VP).
VP	42	Feedback pin for boost converter (VP) and supply for VPOS rail and VDDH rail.
NC	43	Not internally connected.
VPOS	44	Positive supply output pin for panel source drivers. Discharge VPOS to ground whenever the rail is disabled.
NC	45	Not internally connected.
NC	46	Not internally connected.
TS	47	Thermistor input pin. Connect a 10-kΩ NTC thermistor and a 36kΩ linearization resistor between this pin and AGND2.
AGND2	48	Reference point to external thermistor and linearization resistor.
Exposed Pad	N/A	Reference for negative voltage. This pin needs to set floating and must not be connected to ground.

Block Diagram

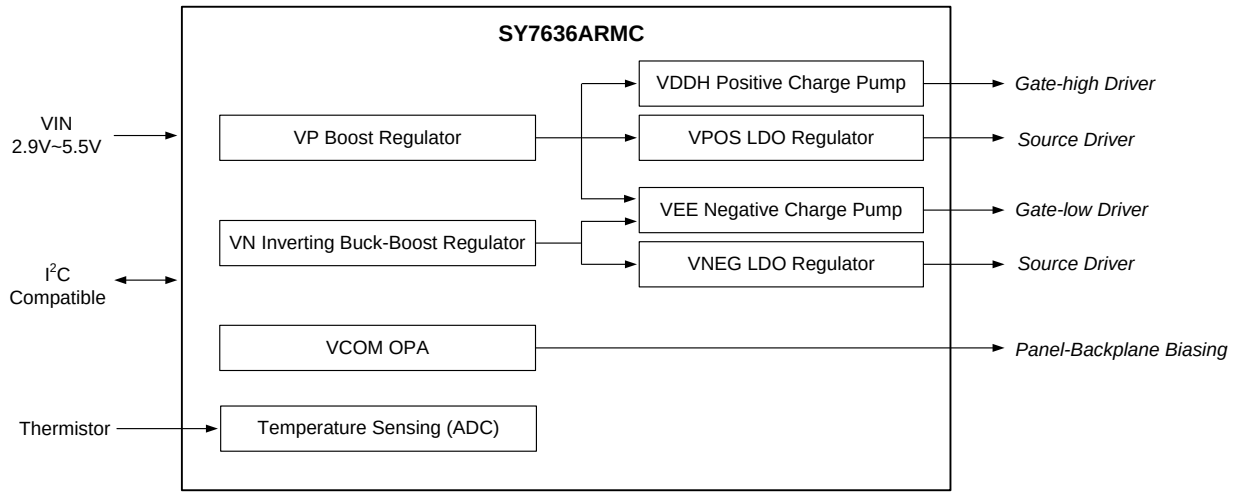


Figure 3. General system block diagram

Absolute Maximum Ratings (Note 1)

- VIN, VN_IN to GND ---------- (-0.3V) ~ 7V
- SDA, SCL, EN, VCOM_EN, VDDH_FB, VEE_FB, PGOOD, TS, VREF to GND ---------- (-0.3V) ~ 3.6V
- VCC, TP1, TP2 to GND ---------- (-0.3V) ~ 4V
- VP, VP_LX, VPOS, VDDH_DRV, VEE_DRV to GND ---------- (-0.3V) ~ 20V
- VDDH_D to GND----------(-0.3V) ~ 18V
- VDDH_DIS, TP3 to GND ---------- (-0.3V) ~ 33V
- VN, VNEG_IN, VNEG, VEE_D, to GND ---------- (-20V) ~ (-0.3V)
- VN_IN to VN_LX ---------- (-0.3V) ~ 30V
- VCOM to GND ---------- (-7V) ~ 0.3V
- Power Dissipation, P_D @ T_A = 25℃
  QFN6×6-48----------5W
- Package Thermal Resistance (Note 2)
  θ_{JA} ---------- 19.88°C/W
  θ_{JC} ---------- 11.72°C/W
- Junction Temperature ---------- 150℃
- Lead Temperature (Soldering, 10 sec.) ---------- 260℃
- Storage Temperature Range ---------- -65℃ to 150℃

Recommended Operating Conditions (Note 3)

- VIN---------- 2.9V ~ 5.5V
- Junction Temperature Range---------- (-10℃) ~ 125℃
- Ambient Temperature Range---------- (-10℃) ~ 85℃

Electrical Characteristics

(VIN = 3.8 V, VP=16V, VN=-16V, VPOS=15V, VNEG=-15V, VDDH=25V, VEE=-20V, Typical values are at T_A = 25 ℃, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
General Supply						
Supply Voltage	VIN		2.9	3.8	5.5	V
VIN UVLO	$V_{IN,RISING}$	VIN Rising		2.7		V
VIN UVLO	$V_{IN,FALING}$	VIN Falling		2.5		
Quiescent Current in Normal Mode	I_{IN}	EN high, ON/OFF bit="ON"		1.5		mA
Quiescent Current in Standby Mode	I_{STD}	EN high, ON/OFF bit="OFF"			100	uA
Quiescent Current in Shutdown Mode	I_{SD}	EN low		3	5	uA
Regulated Voltage for Internal Circuit	V_{CC}	Bypass cap. is 4.7uF		3.3		V
Regulated Voltage for ADC Reference	V_{REF}	Bypass cap. is 100nF		2		V
Thermal Shutdown Trip Point	T_{SD}			150		℃
Thermal Shutdown Hysteresis	T_{HYS}			20		℃
VP (Positive Boost Regulator)						
Output Voltage Range	VP	Fixed voltage		16		V
Output Accuracy			-4.5		4.5	%
Output Current	I_{OUT}			250		mA
MOSFET On Resistance	$R_{DS(ON)}$	VIN = 3.8 V		350		mΩ
Switch Current Limit	I_{LIMIT}		2.1	3	3.9	A
Switch Current Limit Accuracy			–30		30	%
Switching Leakage Current	I_{Lk}			0.1		uA
Switching Frequency	F_{SW}			1000		kHz
VN (Inverting Buck Boost Regulator)						
Output Voltage Range	VN	Fixed voltage		-16		V
Output Accuracy			-4.5		4.5	%
Output Current	I_{OUT}			250		mA
MOSFET On Resistance	$R_{DS(ON)}$	VIN = 3.8 V		350		mΩ
Switch Current Limit	I_{LIMIT}		2.1	3	3.9	A
Switch Current Limit Accuracy			–30		30	%
Switching Leakage Current	I_{Lk}			0.1		uA
Maximum Duty	D_{max}			84		%
Switching Frequency	F_{SW}			1000		kHz
VPOS (Positive LDO)						
Power Good Threshold		Fraction of nominal output voltage		90		%
Power Good Time-out				50		ms
Output Voltage Range	VPOS	Fixed voltage	14.85	15	15.15	V
Output Accuracy		VPOS= 15 V, I_{LOAD} = 20 mA	–1		1	%
Dropout Voltage	$V_{DROPOUT}$	I_{LOAD} = 200 mA			250	mV
Load Regulation – DC	$V_{LOADREG}$	I_{LOAD} = 10% to 90%			1	%
Load Current Range	I_{LOAD}	2.9V ≤ VIN < 3.6V @ VPOS=15V			150	mA
		VIN ≥ 3.6V @ VPOS=15V			200	mA
Output Current Limit	I_{LIMIT}	2.9V ⩽ VIN < 3.6V @ VPOS=15V	150			mA
		VIN ⩾ 3.6V @ VPOS=15V	200			mA
Discharge Impedance to Ground	R_{DIS}	Enabled when rail is disabled		550		Ω
VNEG (Negative LDO)						
Power Good Threshold		Fraction of nominal output voltage		90		%
Power Good Time-out				50		ms

Output Voltage Range	VNEG	Fixed voltage	-15.15	-15	-14.85	V
Output Accuracy		VNEG = -15 V, I_{LOAD} = 20 mA	–1		1	%
Dropout Voltage	$V_{DROPOUT}$	I_{LOAD} = 200 mA			250	mV
Load Regulation – DC	$V_{LOADREG}$	I_{LOAD} = 10% to 90%			1	%
Load Current Range	I_{LOAD}	2.9V ≤ VIN < 3.6V @ VNEG=-15V			110	mA
		VIN ≥ 3.6V @ VNEG=-15V			200	
Output Current Limit	I_{LIMIT}	2.9V ≤ VIN < 3.6V @ VNEG=-15V	110			mA
		VIN ≥ 3.6V @ VNEG=-15V	200			
Discharge Impedance to Ground	R_{DIS}	Enabled when rail is disabled		300		Ω
UVP Fault with Over Loading Capability(Note 4)						
VPOS and VNEG output loading	I_{LOAD}	VPOS=15V	250			mA
		VNEG=-15V	250			
Positive LDO (VPOS) and Negative LDO (VNEG) Tracking						
Difference between VPOS and VNEG	V_{DIFF}	VPOS=15V@20mA VNEG=-15V@20mA 0 ℃ to 60 ℃	–50		50	mV
VCOM Driver						
Drive Current	I_{VCOM}			0	10	mA
Allowed Operating Range	VCOM		–5	-1.25	0	V
Accuracy		VCOM= -1.25 V, VIN = 3.4 V to 4.2 V, no load	–0.8		0.8	%
		VCOM= -1.25 V, VIN = 2.9 V to 5.5 V, no load	–1.5		1.5	%
Resolution		1 LSB		10		mV
Output Current Limit	I_{LIMIT}			40		mA
Discharge Impedance to Ground	R_{DIS}	VCOM_CTRL = low, Hi-Z = 0		550		Ω
VDDH (Positive Charge Pump)						
Power Good Threshold		Fraction of nominal output voltage		90		%
Power Good Time-out				50		ms
Output Voltage Range	VDDH		18	25	29	V
Output Accuracy		I_{LOAD} = 2 mA	–2		2	%
Feedback Voltage	V_{FB_VDDH}			1		V
Load Current Range	I_{LOAD}			1.5	10	mA
Switching Frequency	F_{SW}			1000		kHz
Discharge Impedance to Ground	R_{DIS}	Enabled when rail is disabled		1050		Ω
VEE (Negative Charge Pump)						
Power Good Threshold		Fraction of nominal output voltage		90		%
Power Good Time-out				50		ms
Output Voltage Range	VEE		–25	–20	–18	V
Output Accuracy		I_{LOAD} = 2 mA	–2		2	%
Feedback Voltage	V_{FB_VEE}			0.4		V
Load Current Range	I_{LOAD}			1.5	15	mA
Switching Frequency	F_{SW}			1000		kHz
Thermistor Monitor						
Temperature to Voltage Ratio	A_{TMS}			–0.014		V/ ℃
Offset	$Offset_{TMS}$	Temperature = 0 ℃		1.365		V
Maximum Input Level	V_{TMS_MAX}			2		V
External Pullup Resistor	R_{NTC_PU}			7.5		kΩ

External Linearization Resistor	R_{LINEAR}			36		kΩ
ADC Resolution	ADC_{RES}			14		mV
ADC Sampling Time	ADC_{SPL}			40		us
ADC Conversion Time	ADC_{DEL}			480		us
Accuracy	TMS_{ACC}		–1		1	LSB
Logic Levels and Timing Characteristics (SCL, SDA, PGOOD, EN)						
Output Low Threshold Level	V_{OL}	I_O = 3 mA, sink current (SDA, PGOOD)			0.4	V
Input Low Threshold Level	V_{IL}				0.4	V
Input High Threshold Level	V_{IH}		1.2			V
Deglitch Time, EN Pin	$t_{deglitch}$			100		us
EN pin pull-low Resistor	R_{EN}			200		kΩ
SCL Clock Frequency	F_{SCL}				400	kHz
I^2C Slave Address		7-bit address		0 x 62h		
Oscillator						
Oscillator Frequency	F_{OSC}			1000		kHz

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25℃ on a high effective 4-layer thermal conductivity test board of JEDEC 51-7 thermal measurement standard. Paddle of QFN 6x6 packages is the case position for θ_{JC} measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: UVP fault behavior is measured at T_A=25℃ on a four-layer Silergy evaluation board.

Power-up and Power-down Sequence

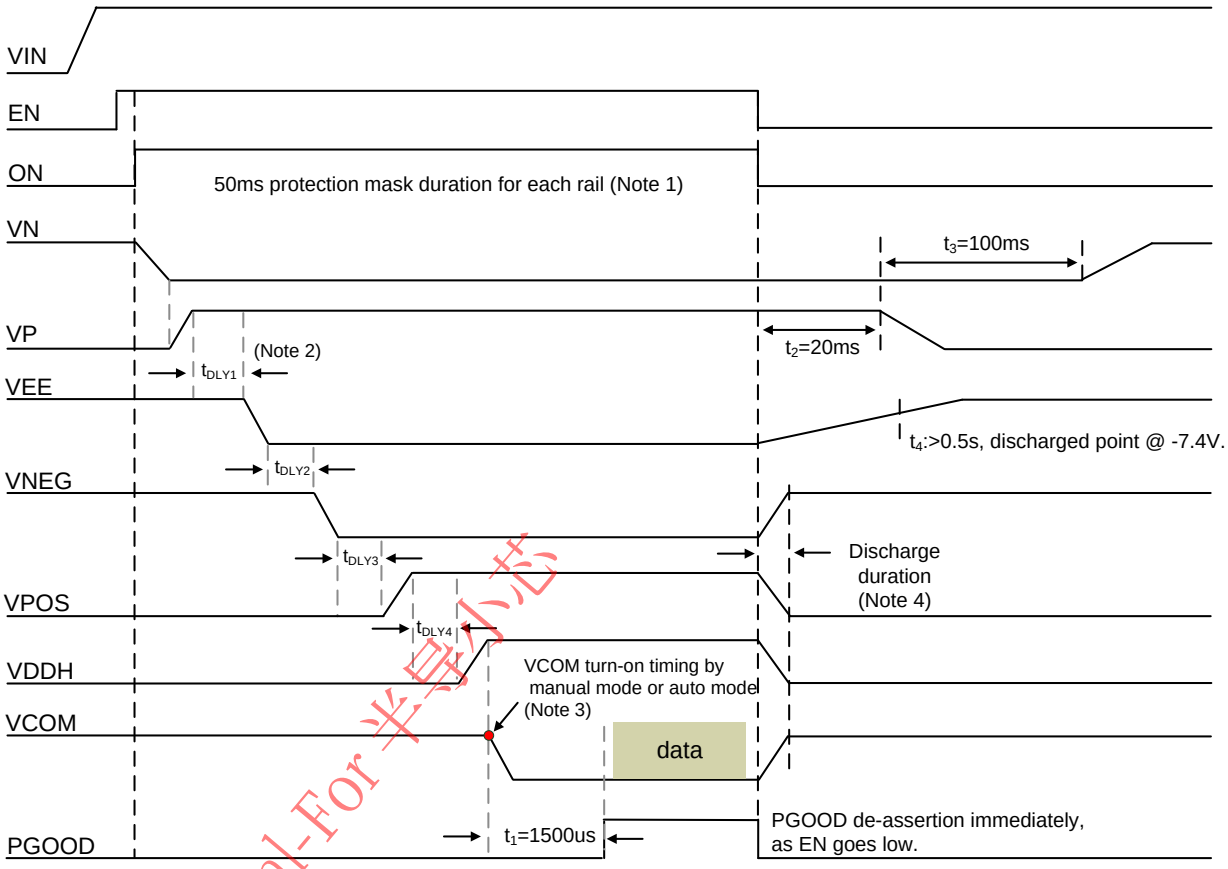


Figure4. Power-up and power-down sequence.

Notes:

1. For each rail, VN, VP, VPOS, VNEG, VDDH & VEE, during soft start, there is 50ms protection mask time.
2. t_{DLYx} is programmable by 2 bits for each delay time. 0ms/1ms/2ms/4ms.
3. VCOM turn-on timing (>UVLO & EN high)
   a. For auto-mode set by I^2C, VCOM timing follows the default sequence, and it is independent with external VCOM_EN pin.
   b. For manual mode set by I^2C, after the last rail power-on (VDDH), VCOM starts ramping as VCOM_EN pull-high. As VCOM_EN pull-low & VN power ready, VCOM is shutdown. VCOM_EN is only dependent with VCOM rail.
4. Discharge function only for VNEG, VPOS, VDDH & VCOM. VN, VP & VEE are no discharge function.

Timing Requirements: Data Transmission

VIN = 3.8 V ±5%, T_A = 25℃, C_L = 100 pF

Parameter	Symbol	Test Conditions	MIN	NOM	MAX	UNIT
Serial Clock Frequency	$f_{(SCL)}$		100		400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{HD;STA}$	SCL = 100 kHz	4			us
		SCL = 400 kHz	600			ns
Low Period of the SCL Clock	t_{LOW}	SCL = 100 kHz	4.7			us
		SCL = 400 kHz	1.3			
High Period of the SCL Clock	t_{HIGH}	SCL = 100 kHz	4			us
		SCL = 400 kHz	600			ns
Set-up Time for a Repeated START Condition	$t_{SU;DAT}$	SCL = 100 kHz	4.7			us
		SCL = 400 kHz	600			ns
Data Hold Time	$t_{HD;DAT}$	SCL = 100 kHz	0		3.45	us
		SCL = 400 kHz	0		900	ns
Data Set-up Time	$t_{SU;DAT}$	SCL = 100 kHz	250			ns
		SCL = 400 kHz	100			
Rise Time of Both SDA and SCL Signals	t_r	SCL = 100 kHz			1000	ns
		SCL = 400 kHz			300	
Fall Time of Both SDA and SCL Signals	t_f	SCL = 100 kHz			300	ns
		SCL = 400 kHz			300	
Set-up Time for STOP Condition	$t_{SU;STO}$	SCL = 100 kHz	4			us
		SCL = 400 kHz	600			ns
Bus Free Time Between Stop and Start Condition	t_{BUF}	SCL = 100 kHz	4.7			us
		SCL = 400 kHz	1.3			
Pulse Width of Spikes that must be Suppressed By the Input Filter	t_{SP}	SCL = 100 kHz	n/a		n/a	ns
		SCL = 400 kHz	0		50	
Capacitive Load for Each Bus Line	C_b	SCL = 100 kHz			400	pF
		SCL = 400 kHz			400	

I²C Compatible Interface

SY7636A integrates an I²C compatible interface. To ensure compatibility with a wide range of system processors, the I²C interface supports clock speeds of up to 400kHz (“Fast-Mode”) and uses standard I²C commands. SY7636A always operates as a slave device, and is addressed using a 7-bit slave address followed by an 8th bit, which indicates whether the transaction is a read-operation or a write-operation.

The I²C interface is fully functional after VIN is above UVLO threshold and EN pin is high.

I²C Interface Timing Diagram:

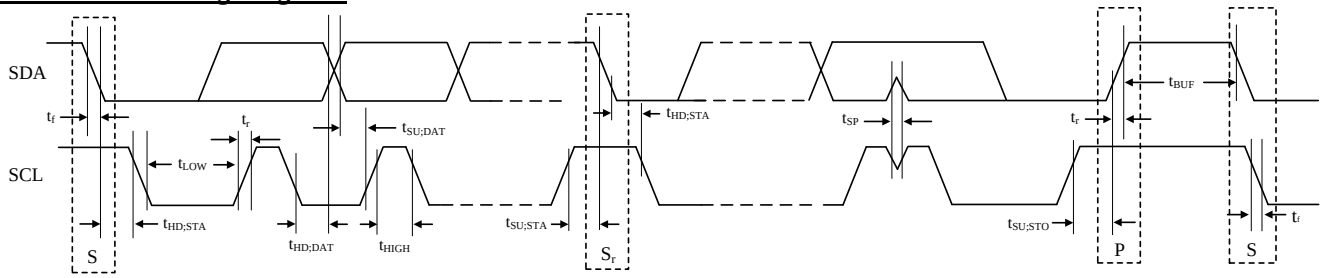


Figure 5. I²C Data Transmission Timing.

I²C Device Address

When communicating with multiple devices using the I²C interface, each device must have its own unique address. That is, the host can distinguish between the devices. SY7636A has a device address.

START and STOP Conditions

The START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition. The I²C master always generates the START and STOP conditions.

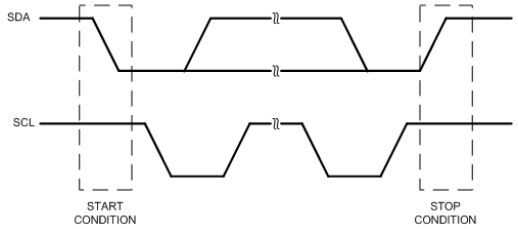


Figure6. Start and stop conditions for I²C.

Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.

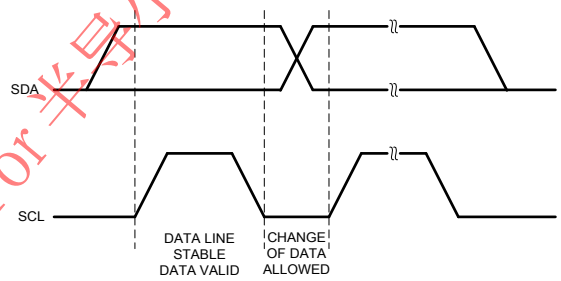


Figure 7. Data validity.

Acknowledge

Each address and data transmission uses 9-clock pulses. The ninth pulse is the acknowledge bit (ACK). After the START condition, the master sends 7-slave address bits and an R/$\overline{W}$ bit during the next 8-clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge. The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data.

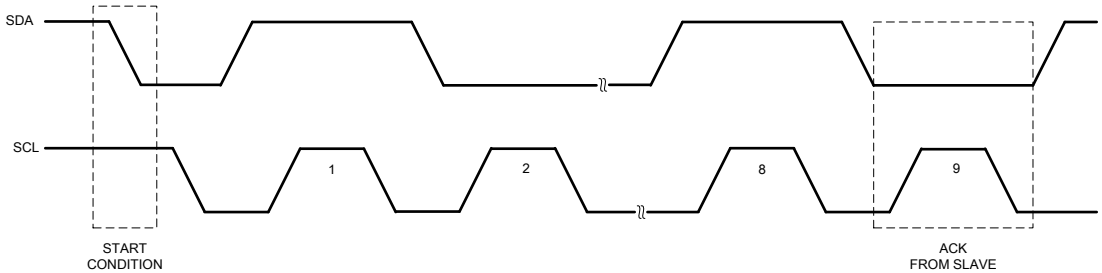


Figure 8. I²C acknowledge.

Register Address Map

REGISTER	ADDRESS (HEX)	NAME	DEFAULT VALUE	DESCRIPTION
0	0x00	Operation Mode Control	00h	Turning on/off power rails, VCOM control, and discharge on/off control
1	0x01	VCOM Adjustment Control 1	7Dh	Voltage settings for VCOM(bits 0~7)
2	0x02	VCOM Adjustment Control 2	14h	Voltage settings for VCOM (bit 8)
3	0x03	VLDO Voltage Adjustment Control	66h	LDO setting
4	0x04	NA	07h	No function definition
5	0x05	NA	26h	No function definition
6	0x06	Power On Delay Time	AAh	Power on delay time set for VEE, VNEG, VPOS & VDDH
7	0x07	Fault Flag	00h	Show error code and PG signal
8	0x08	Thermistor Readout	00h	Thermistor value read by ADC

Operation Mode Control (Address: 0x00h)

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	ON_OFF	VCOMCTL	Reserved	DISCHG				
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	0	0	0	0	0

FIELD NAME	BIT DEFINITION
ON_OFF [7]	Turning on/off power rails 1 -Turn on all of power rails (2 switching regulators, 2 charge pumps, and 2 LDOs), when EN pin being high. 0 -Turn off all of power rails (2 switching regulators, 2 charge pumps, and 2 LDOs), when EN pin being high.
VCOMCTL [6]	VCOM on auto mode or manual mode via VCOM_EN pin 1 – VCOM on/off is controlled by external VCOM_EN pin 0 – VCOM on/off will follow the default sequence
Reserved [5]	Reserved for internal use ONLY. Read only for application.
DISCHG [4:0]	Active discharge settings Bit 4: 0 – enable discharge function for VDDH ; 1 – disable discharge function for VDDH Bit 3: 0 – reserved bit, not support VEE internal discharge function Bit 2: 0 – enable discharge function for VPOS ; 1 – disable discharge function for VPOS Bit 1: 0 – enable discharge function for VNEG ; 1 – disable discharge function for VNEG Bit 0: 0 – enable discharge function for VCOM ; 1 – disable discharge function for VCOM Notes: These control bits is defined during VN rail operating. As VN rail shutdown, these control bits is independent with discharge function control.

VCOM Adjustment Control 1 (Address: 0x01h)

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	VCOM [7:0]							
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	1	1	1	1	1	0	1

FIELD NAME	BIT DEFINITION
VCOM [7:0]	VCOM voltage, least significant byte. See 0x02h register for details. Default value is 0x7Dh (-1.25V)

VCOM Adjustment Control 2 (Address: 0x02h)

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	VCOM[8]	Reserved						
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	1	0	1	0	0

FIELD NAME	BIT DEFINITION
VCOM [8]	VCOM voltage adjustment with 9 bits VCOM = VCOM[8:0] x -10mV in the range from 0 V to -5 V 0x000h = 0 0000 0000 = 0 mV 0x001h = 0 0000 0001 = -10 mV 0x002h = 0 0000 0002 = -20 mV … 0x07Dh = 0 0111 1101 = -1250 mV (default) … 0x1F4h = 1 1111 0100 = -5000 mV 0x1F5h = 1 1111 0101 = -5000 mV … 0x1FEh = 1 1111 1110 = -5000 mV 0x1FFh = 1 1111 1111 = -5000 mV
Reserved [6:0]	Reserved bits

VLDO Voltage Adjustment Control (Address: 0x03h)

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	VLDO			Reserved				
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	1	1	0	0	1	1	0

FIELD NAME	BIT DEFINITION
VLDO [7:5]	VPOS & VNEG voltage adjustment 0x0h = 000 = reserved, limited to R/W 0x1h = 001 = reserved, limited to R/W 0x2h = 010 = +/-15.25V 0x3h = 011 = +/-15.00V (default) 0x4h = 100 = +/-14.75V 0x5h = 101 = +/-14.50V 0x6h = 110 = +/-14.25V 0x7h = 111 = reserved, limited to R/W
Reserved [4:0]	Reserved bits

Power On Delay Time (Address: 0x06h)

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	t_{DYL4}		t_{DYL3}		t_{DYL2}		t_{DYL1}	
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	1	0	1	0	1	0	1	0

FIELD NAME	BIT DEFINITION
t_{DYL4} [7:6]	t_{DYL4} delay time set; defines the delay time from VPOS to VDDH 00 = 0ms 01 = 1ms 10 = 2ms (default) 11 = 4ms
t_{DYL3} [5:4]	t_{DYL3} delay time set; defines the delay time from VNEG to VPOS 00 = 0ms 01 = 1ms 10 = 2ms (default) 11 = 4ms
t_{DYL2} [3:2]	t_{DYL2} delay time set; defines the delay time from VEE to VNEG 00 = 0ms 01 = 1ms 10 = 2ms (default) 11 = 4ms
t_{DYL1} [1:0]	t_{DYL1} delay time set; defines the delay time from VP to VEE 00 = 0ms 01 = 1ms 10 = 2ms (default) 11 = 4ms

Fault Flag (Address: 0x07h)

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	Reserved			Fault				PG
READ/WRITE	R	R	R	R	R	R	R	R
RESET VALUE	0	0	0	0	0	0	0	0

FIELD NAME	BIT DEFINITION
Reserved [7:5]	Reserved bits
Fault [4:1]	Fault flag to show the fault event, and related rail. When power off controlled by I2C, and then re-toggle EN pin can reset fault register value being 0x00h before next power on. 0x0h: no fault event (default) 0x1h: UVP at VP rail 0x2h: UVP at VN rail 0x3h: UVP at VPOS rail 0x4h: UVP at VNEG rail 0x5h: UVP at VDDH rail 0x6h: UVP at VEE rail 0x7h: SCP at VP rail 0x8h: SCP at VN rail 0x9h: SCP at VPOS rail 0xAh: SCP at VNEG rail 0xBh: SCP at VDDH rail 0xCh: SCP at VEE rail 0xDh: SCP at VCOM rail 0xEh: Reserved 0xFh: Thermal shutdown
PG	Power good flag 1 – VDDH, VEE, VPOS & VNEG are in regulation 0 – VDDH, VEE, VPOS & VNEG are not in regulation or turned off (default)

Thermistor Readout (Address: 0x08h)

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	TMST_VALUE							
READ/WRITE	R	R	R	R	R	R	R	R
RESET VALUE	0	0	0	0	0	0	0	0

FIELD NAME	BIT DEFINITION
TMST_VALUE [7:0]	Temperature read-out 1111 0110 = -10℃ 1111 0111 = -9℃ … 1111 1110 = -2℃ 1111 1111 = -1℃ 0000 0000 = 0℃ 0000 0001 = 1℃ 0000 0010 = 2℃ … 0001 1001 = 25℃ … 0101 0101 = 85℃ Note: 1. As reported code from 0x56h to 0x61h, the accuracy of thermal reporting is not guarantee, and clamping being 0x61h. 2. As reported code from 0xF7h to 0xEFh, the accuracy of thermal reporting is not guarantee, and clamping being 0xEFh.

Layout Consideration

Layout is very important in high frequency switching converter design. The PCB can radiate excessive noise and contribute to converter instability with improper layout.

1. Power components should be placed on the same side of board, with power traces routed on the same layer. If it is necessary to route a power trace to another layer, choose a trace in low di/dt paths and use multiple vias for interconnection. When vias are used to connect PCB layers in the high current loop, multiple vias should be used to minimize via impedance. Certain points must be considered before starting a layout.
2. Exposed pad need to put more via to improve heat dissipation. And, optional to connect exposed pad to VN(-16V) through PIN 22 with wide trace to enhance heat dissipation.
3. Exposed pad is internally connected to VN rail and must NOT be connected to ground.
4. Place the bypass capacitor & output capacitors close to IC, such as VREF pin, VNEG pin, VNEG_IN pin, VCC pin, VIN pin, VCOM pin, VN_IN pin, VN pin, VEE_D pin, VDDH_D pin, VP pin, and VPOS pin.
5. For feedback signals at VP pin & VN pin, the sensing point which detects the output voltage must be connected after output capacitor and keep the trace far away from the switching node or inductor.
6. Feedback traces at VEE_FB pin & VDDH_FB pin must be routed away from any potential noise source to avoid coupling. Moreover, the voltage divider network is as close to IC as possible.
7. A conceptual of PCB layout guide is shown in Figure 9 for reference.

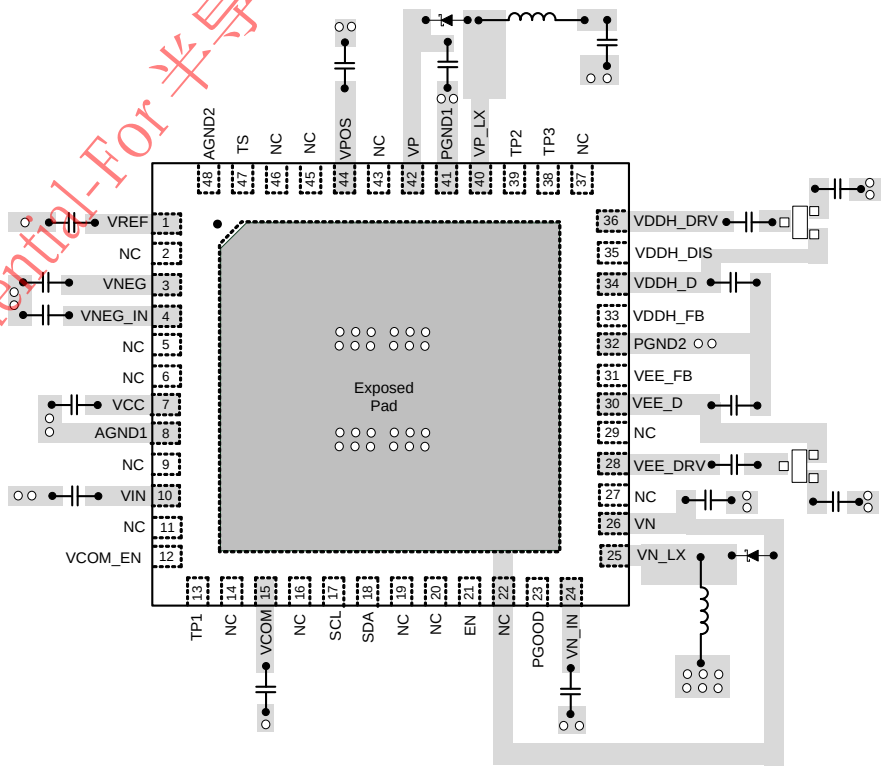
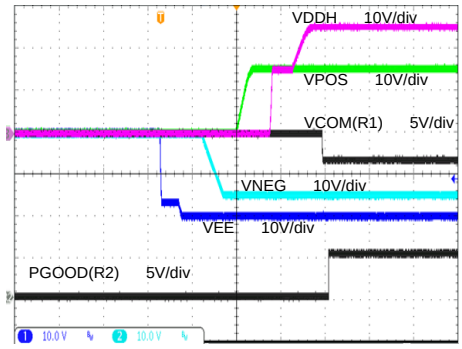


Figure 9. Conceptual PCB Layout Guide

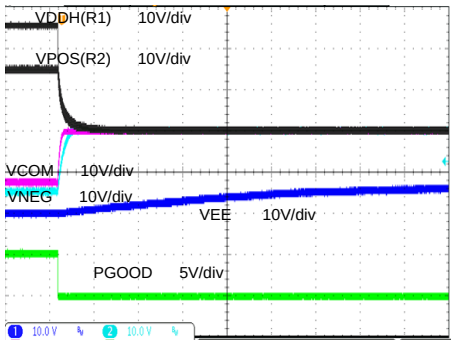
Typical Performance Characteristics

Default Power-up Sequence



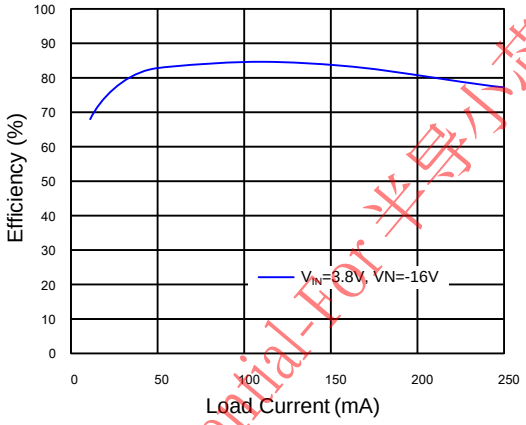
Time (10ms/div)

Default Power-off Sequence

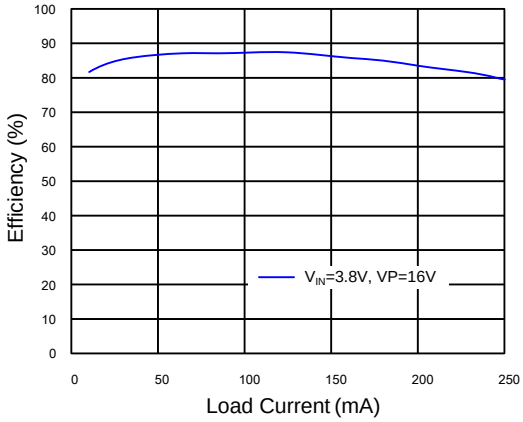


Time (10ms/div)

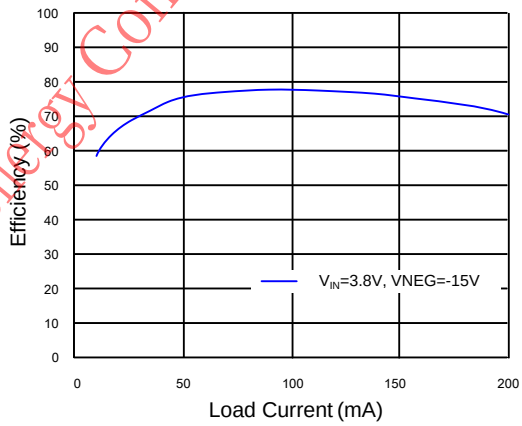
VN DCDC Efficiency



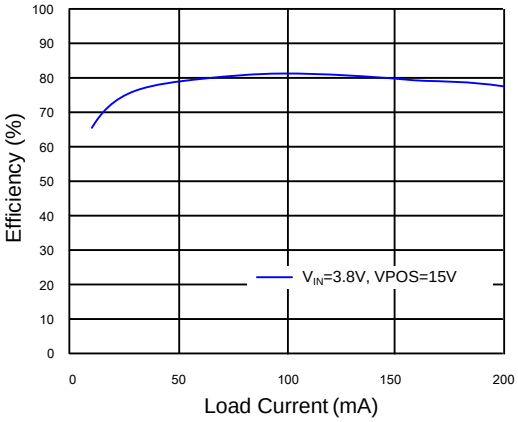
VP DCDC Efficiency



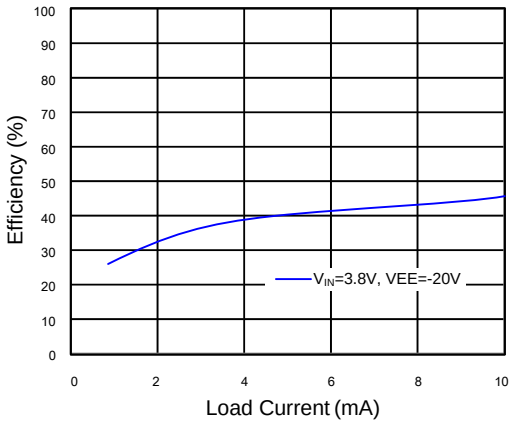
VNEG Negative LDO Efficiency



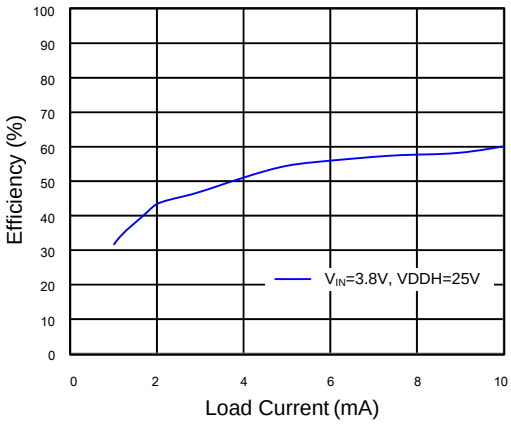
VPOS Positive LDO Efficiency



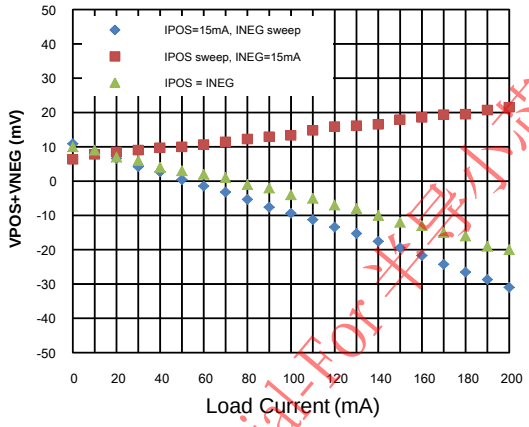
VEE Charge Pump Efficiency



VDDH Charge Pump Efficiency



Source Driver Supply Tracking



Applications Information

The SY7636A provides two adjustable LDOs(VNEG & VPOS) that support up to 200mA of output current for source driver and two charge pumps (VEE & VDDH) to provide the gate driver supply. VEE rail can supply 15mA, and VDDH rail can supply 10mA. An adjustable VCOM voltage is generated by a linear amplifier for accurate back-plane biasing. The device supports a temperature measurement function with an external NTC network to monitor the display panel temperature in a range from -10℃ to 85℃ and accuracy of ±1℃ from 0℃ to 50℃. SY7636A also provides an I²C interface control for specific parameter programmable.

Device Functional Modes

As shown in Figure 10, SY7636A supports three operation modes, which are SLEEP, STANDBY, and ACTIVE. SLEEP mode is a lowest power mode for battery saving. In STANDBY mode, the device is ready to accept commands through the I²C interface. In ACTIVE, all rails are power up successfully.

SLEEP MODE

As VIN achieving UVLO rising threshold and EN pin being low level, SY7636A enters SLEEP MODE to turn off all internal circuitry to save the power. In this operation mode, all of registers are reset to default values, and I²C communications is invalid.

STANDBY MODE

As EN pin pull high to enter STANDBY MODE, SY7636A is ready to receive I²C command to power up VEE, VNEG, VPOS, VDDH and VCOM rail, sequentially. Before set bit[7] at 0x00h being 1, all of power rails are in power off state, and keep in STANDBY MODE.

ACTIVE MODE

For entering ACTIV MODE, EN pin is pulled high at first.And then, after 2.5ms delay time, set bit[7] at 0x00h being 1, all of power rails will be turned on sequentially. After all of rails power up successfully without protection event occurring, the PGOOD pin is pulled high.

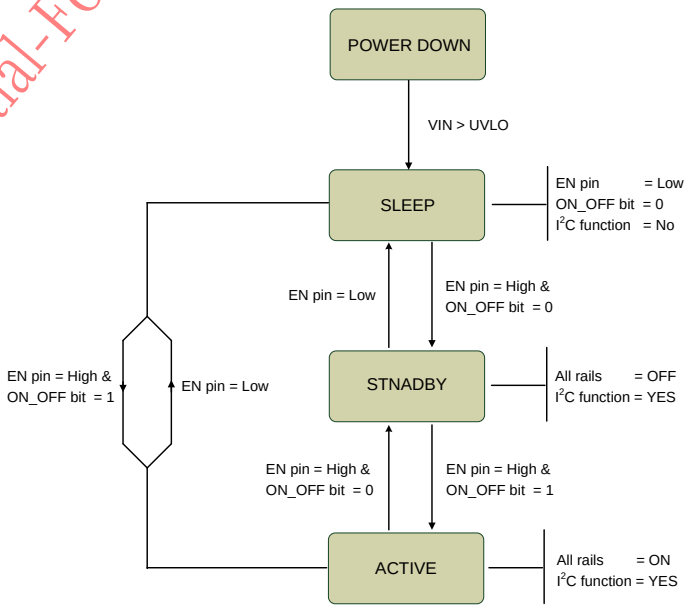


Figure 10. Operation Mode Diagram.

Power-ON and Power-OFF Sequencing

For power-on control, VEE, VNEG, VPOS and VDDH rails are turned on sequentially with programmable delay time by bits[7:0] at register 0x06h. For power-off control, all of power rails will be turned off simultaneously.

Power-On Sequencing

To pull high EN pin and then set ON_OFF bit[7] at 0x00h being 1 to enable all of power rails with specific power-up sequence, as shown in Figure 11. During power on period, negative buck-boost (VN) start-up at first, and then the positive boost (VP) ramps up as VN settling. After delay time t_{DELY1}, negative charge pump (VEE) is start-up. As VEE rail settling, negative LDO rail (VNEG) will ramp up after delay time t_{DELY2}. As VNEG rail settling, positive LDO rail (VPOS) will ramp up, after delay time t_{DELY3}. Finally, positive charge pump (VDDH) is power-up after delay time t_{DELY4}.

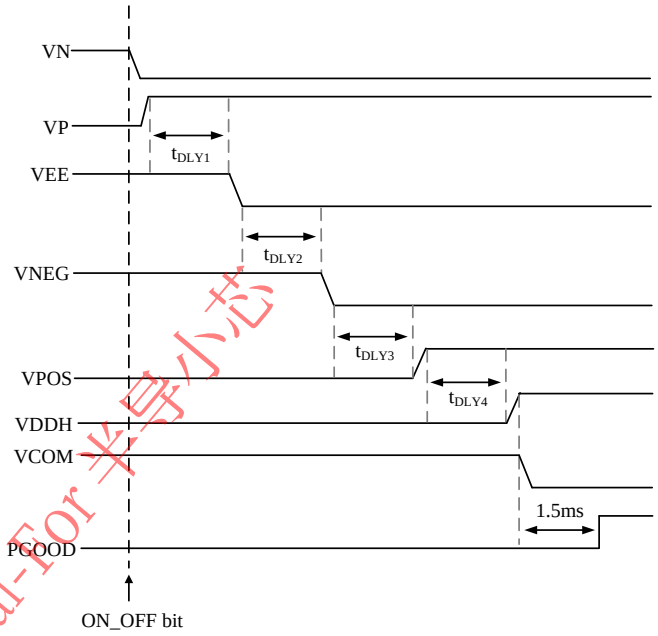


Figure 11. Power-on sequence Timing: VCOM set being auto mode.

VCOM Control

SY7636A provides VCOM auto mode or manual mode, controlled by bit[6] at 0x00h.

- Auto Mode: VCOM turn-on timing follows the default sequence, and it is independent with external VCOM_EN pin, as shown in Figure 11.
- Manual Mode: VCOM power-on timing is after the last rail power-on (VDDH) done. To pull-high external VCOM_EN pin to enable VCOM rail. The VCOM_EN pin is only dependent with VCOM rail.

POWER GOOD

The power good pin (PGOOD) is an open-drain output that needs to be pulled high by an external pullup resistor. The PGOOD pin is pulled high after VDDH soft-start finished 1.5ms when VEE, VNEG, VPOS and VDDH are successful power-on. The PGOOD pin behavior is independent with VCOM rail operation. If any of VEE, VNEG, VPOS and VDDH encounters a fault to cause the rail shutdown, the PGOOD pin is pulled low immediately.

Soft Start

SY7636A supports soft start for all rails to limit inrush current during power-up. If VN or VP is unable to reach specific voltage level within 50ms, the device is shutdown and enters latch-off state. The protection can be released by re-toggling the EN pin or ON/OFF bit[7] at 0x00h. VPOS, VNEG, VEE and VDDH rail also had a 50ms time-

out constraint during power-on period. If either rail is unable to power up within 50ms after it has been enabled, the corresponding rail is shutdown and remains cycling hiccup until fault release.

Power-Off Sequencing

In general, SY7636A can set ON_OFF bit being 0 to power off the device at first. And then, waiting for output voltage discharge completion, system can pull EN pin being low to reset all of register and save the power. As set ON_OFF bit being 0, VEE, VNEG, VPOS, VDDH, and VCOM are shutdown simultaneously. At this timing, the PGOOD pin is pulled low at first. After 20ms delay, the positive boost (VP) is shutdown and then after 100ms delay, the negative boost (VN) is powered off.

Active Discharge

SY7636A provides internal discharge paths for VNEG, VPOS, VDDH and VCOM rails, for which the discharge function control bit by I^2C register are independent. Active discharge function remains enabled before VIN lower than UVLO. After the negative boost converter (VN) power-off, the device enters STANDBY or SLEEP mode, depending on the state of the EN pin.

VPOS/VNEG Supply Tracking

Positive LDO(VPOS) and negative LDO(VNEG) track each other in a way that they are of opposite sign but same magnitude. The different voltage value between VPOS and VNEG is guaranteed to be less than 50 mV.

Temperature Monitoring

The SY7636A provides circuitry to bias and measure an external Negative Temperature Coefficient Resistor (NTC) to monitor the ambient temperature in a range from –10 ℃ to 85 ℃ with accuracy of ±1 ℃ from 0 ℃ to 50 ℃. As set ON/OFF bit[7] being 1 at 0x00h, temperature measurement is working continuously and the last temperature reading is always stored in the Thermistor Readout register(0x08h).

NTC Bias Circuit

Figure 12 shows the block diagram of the NTC bias and sensing network. The NTC is biased from VREF pin (2V) through a resistor 7.5kΩ bias resistor. A 36kΩ resistor is connected in parallel with the NTC to linearize the temperature response curve. For achieving an accurate thermal sense network, GND plane of NTC network should connect directly to PIN48(AGND2) by a trace to implement remote sense. The circuit is designed to work with a nominal 10kΩ NTC and achieves accuracy of ±1°C from 0°C to 50°C.

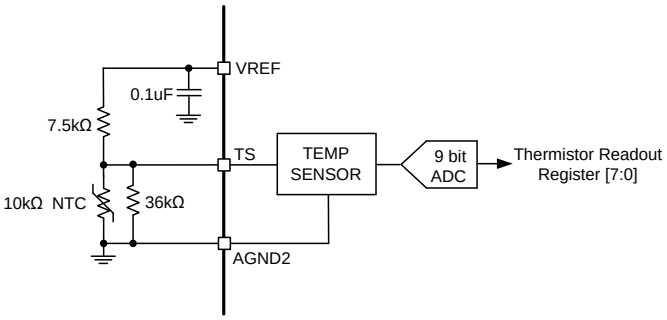


Figure 12.Temperature Monitoring Network.

The temperature sensing voltage across the NTC is digitized by a 9-bit ADC and translated into an 8-bit thermistor readout register. The ADC output versus temperature is shown in Table 1.

Table 1. ADC Output Value vs Temperature

TEMPERATURE	TMST_VALUE[7:0]
–10 ℃	1111 0110
–9 ℃	1111 0111
... ...	... ...
–2 ℃	1111 1110

–1 ℃	1111 1111
0 ℃	0000 0000
1 ℃	0000 0001
2 ℃	0000 0010
... ...	... ...
25 ℃	0001 1001
...	...
85 ℃	0101 0101

Under-Voltage Lockout (UVLO)

SY7636A provides an UVLO detection function to monitor the VIN voltage. If the voltage at VIN pin exceeds $V_{IN,RISING}$ voltage(typ.=2.7V), SY7636A enters SLEEP MODE. Then, to pull-high EN pin at first and set bit[7] at 0x00h being 1 to power up all rails. If VIN pin voltage is lower than $V_{IN,FALLING}$ voltage(typ.=2.5V) when the device is operating, all rails are shutdown together. The UVLO hysteresis (typ.=0.2V) is designed to prevent shutdown caused by supply transients.

Under Voltage Protection(UVP)

SY7636A supports output under-voltage protection mechanism. For VN and VP, if the output voltage of either rail is below 80% of set voltage, the VN, VP, VNEG, VPOS, VEE and VDDH are shutdown. After all rails shutdown, the device enters latch-off state. The latch-off state can be released by re-toggling the EN pin. For VNEG, VPOS, VEE and VDDH, if the output voltage of either rail is below 80% of set voltage, the VNEG, VPOS, VEE and VDDH are shutdown together. And then the fault rail remains cycling hiccup until fault release. As fault occurring, the PGOOD pin is pull-low.

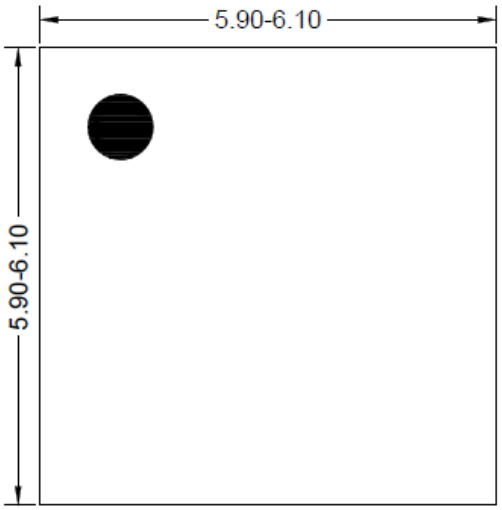
Short Current Protection (SCP)

SY7636A integrates output short-current protection mechanism to prevent the device damage when the output short to GND. For VN and VP, if the output voltage of either rail is falling below the SCP threshold 2V, the VN, VP, VNEG, VPOS, VEE and VDDH are shutdown together. And then the device enters latch-off state. The latch-off state can be released by re-toggling the EN pin. For VNEG, VPOS, VEE and VDDH, if the output voltage of either rail is falling below the SCP threshold 2V, the VNEG, VPOS, VEE and VDDH are shutdown together. And then the fault rail remains cycling hiccup until fault release. As fault occurring, the PGOOD pin is pull-low.

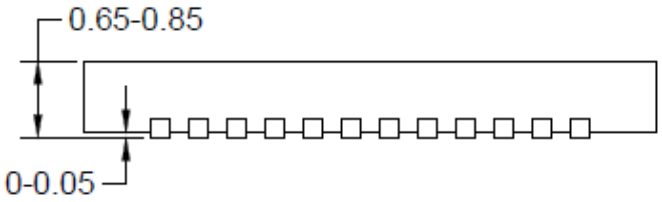
Over Temperature Protection (OTP)

When the junction temperature exceeds OTP threshold(150 ℃), the SY7636A will shut down all the rails in latch off state and pull low PGOOD pin immediately to prevent overheating due to excessive power dissipation. The latch-off state can be released by re-toggling the EN pin. After re-toggling the EN pin and the junction temperature cools down by the OTP hysteresis(20 ℃), the SY7636A can be back to SLEEP MODE or STANDBY MODE depend on EN pin.

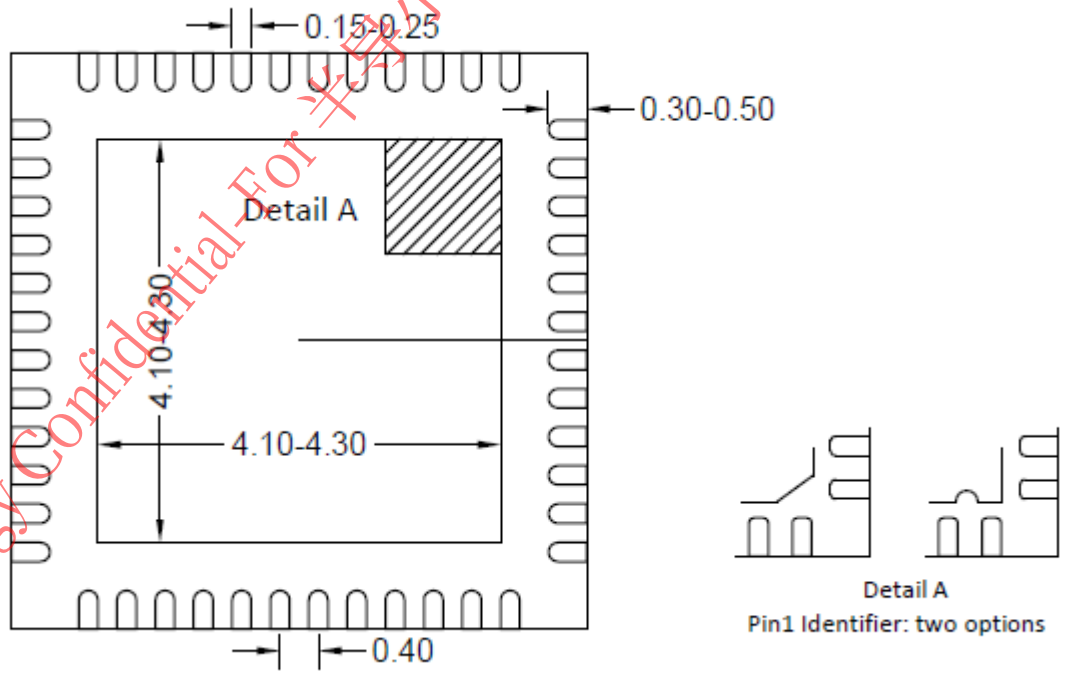
QFN6×6-48 Package Outline Drawing



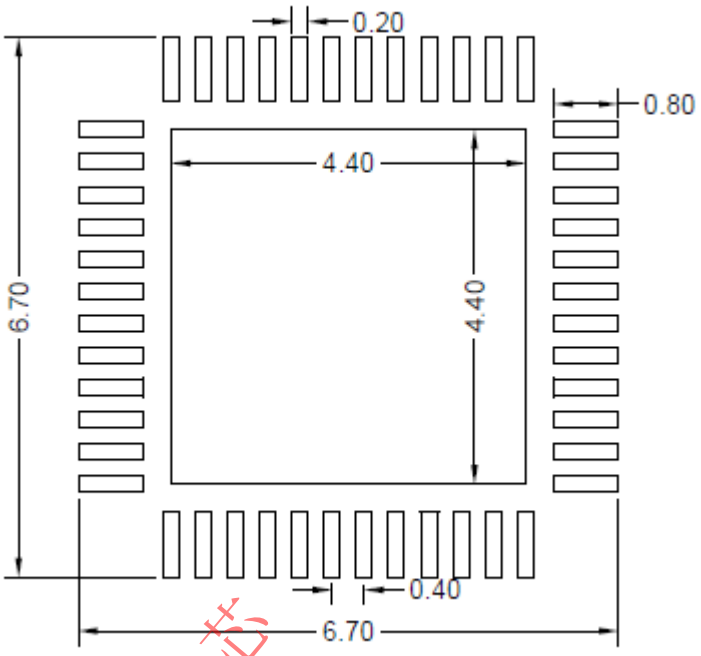
Top View



Side View



Bottom View



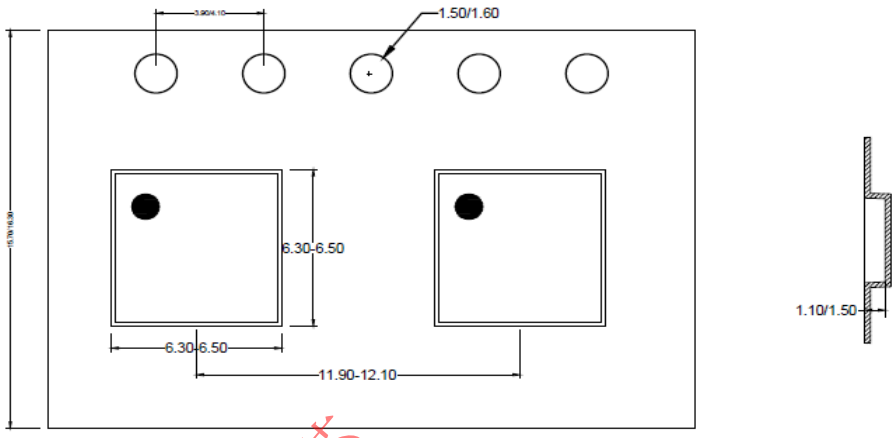
Recommended PCB layout

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

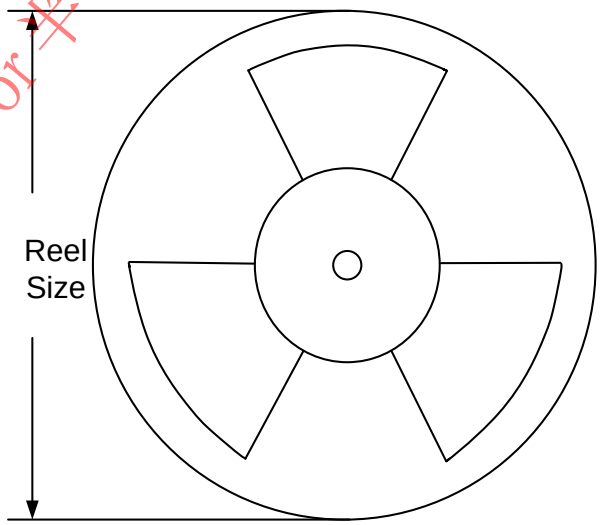
Taping & Reel Specification

1. Taping Orientation

QFN6×6-48



2. Carrier Tape & Reel Specification for Packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
QFN6×6	16	12	13"	400	400	2500

3. Others: NA