SY7901

High Efficiency 500kHz, 25V PWM Controller with DC Input Current Limit

General Description

The SY7901 is a current mode DC/DC controller targeted for Boost, Sepic, Flyback and Forward applications. The SY7901 has an accurate DC input current limit. External compensation provides flexible adjustment of control loops for different applications. The internal low side driver is capable of sourcing 1.5A and sinking 3A current.

Features

- Input Voltage Range 3V to 25V
- 500kHz Fixed Switching Frequency
- An Accurate DC Input Current Limit
- External Compensation
- Internal Soft-start Limits the Inrush Current
- Integrated Low Side Driver: 1.5A Sourcing and 3A Sinking
- RoHS Compliant and Halogen Free
- Compact Package: DFN3×3-10

Ordering Information

SY7901 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY7901DBC	DFN3×3-10	----

Applications

- GPS Navigation Systems
- Handheld Devices
- Portable Media Player

Typical Applications

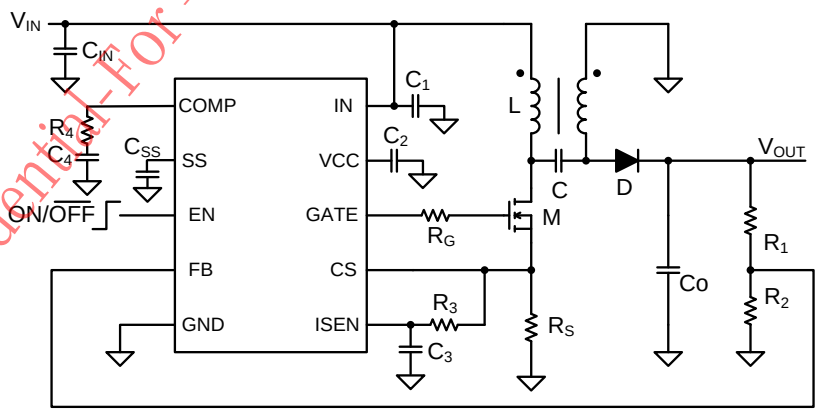
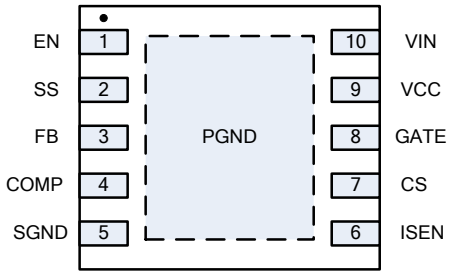


Figure1. Schematic Diagram

Pinout (top view)



(DFN3×3-10)

Top Mark: FR*xyz* for SY7901 (Device code: FR, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
VIN	10	Input pin. Decouple this pin to the PGND pin with at least a 1µF ceramic capacitor.
VCC	9	5V Internal LDO output from VIN. Connect a 4.7 µF capacitor from this pin to PGND.
GATE	8	Driver pin. Connect the gate of the power NFET to this pin.
CS	7	Current sense pin. Connect an external current sensing resistor R_S from this pin to GND. The voltage on this pin is used for providing MOSFET current feedback in the control loop and cycle-by-cycle peak current limit. Peak current limit is triggered when the sensed voltage plus the slope compensation exceed 340mV.
ISEN	6	Connect this pin to CS to program the input average current limit. The input current limit should be I_{iLIM}=100mV/Rs
SGND	5	Signal ground pin.
COMP	4	External compensation pin. Connect the RC network from this pin to SGND to compensate the control loop.
FB	3	Output voltage feedback pin. Connect this pin to the output voltage divider to program output voltage: V_{OUT}=1V×(1+R_1/R_2)
SS	2	Connect a capacitor from this pin to SGND to program the soft-start time.
EN	1	Enable pin. Pull it high to turn on the chip. Do not leave this pin floating.
PGND	Exposed Paddle	Power ground pin.

Absolute Maximum Ratings (Note 1)

IN, EN ---------- 26V
GATE ---------- VCC+0.3V
All Other Pins ---------- 6V
Power Dissipation, P_D @ T_A = 25°C, DFN3×3-10---------- 2.6W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 38°C/W
θ_{JC} ---------- 8°C/W
Junction Temperature Range ---------- -40 to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

IN---------- 3V to 25V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified)

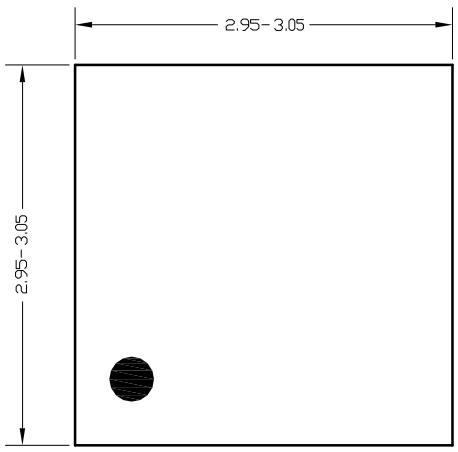
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		3		25	V
Quiescent Current	I_Q	FB=1.1V		170		μA
Shutdown Current	I_{SHDN}	EN=0		0.1		μA
Feedback Reference Voltage	V_{REF}		0.98	1	1.02	V
FB Input Current	I_{FB}	$V_{FB}=V_{IN}$	-50		50	nA
Current Sense Limit	I_{SEN}		98	100	102	mV
Internal Slope Compensation	V_{SLOPE}			40		mV/μS
Gm of EA	Gm			300		μA/V
Gate Driver Output Peak Current	I_{SOURCE}			1.5		A
	I_{SINK}			3		A
EN Rising Threshold	V_{ENH}		1.5			V
EN Falling Threshold	V_{ENL}				0.4	V
Input UVLO threshold	V_{UVLO}				2.9	V
UVLO hysteresis	V_{HYS}			0.3		V
Oscillator Frequency	F_{OSC}			500		kHz
Min ON Time				200		ns
Min OFF Time				200		ns
Internal LDO Output	V_{VCC}	V_{IN}=5.5V	4.9	5	5.1	V
Thermal Shutdown	T_{SD}			150		℃
Thermal Hysteresis	T_{HYST}			20		℃

Note 1: Stresses beyond "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

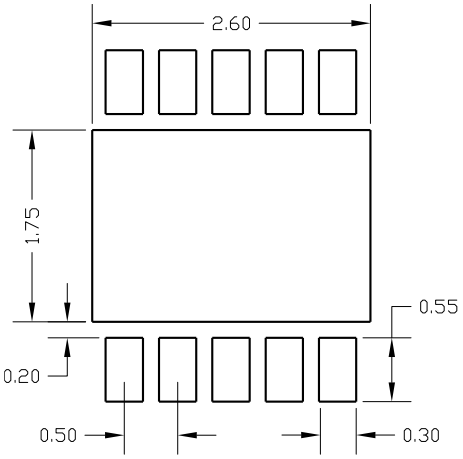
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: The device is not guaranteed to function outside its operating conditions.

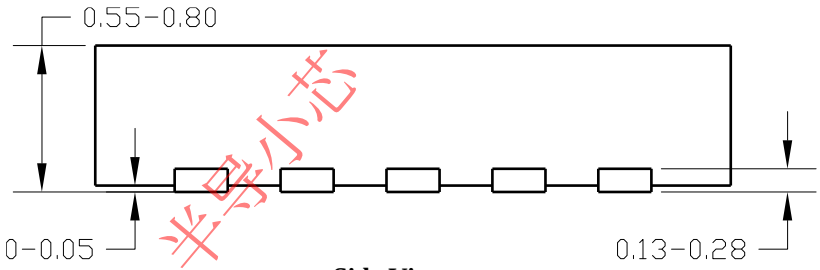
DFN3×3-10 Package Outline



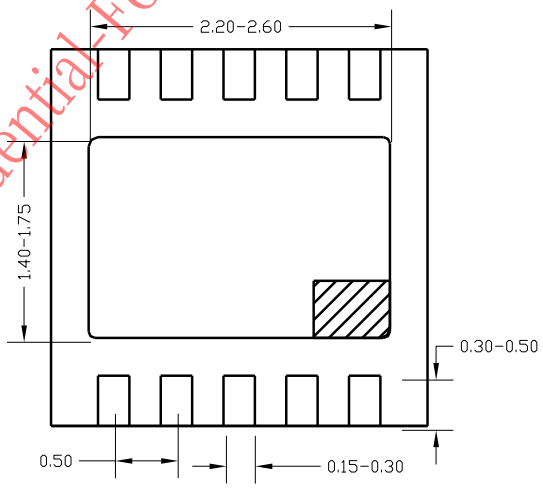
Top View

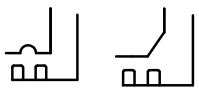


PCB layout (recommended)



Side View





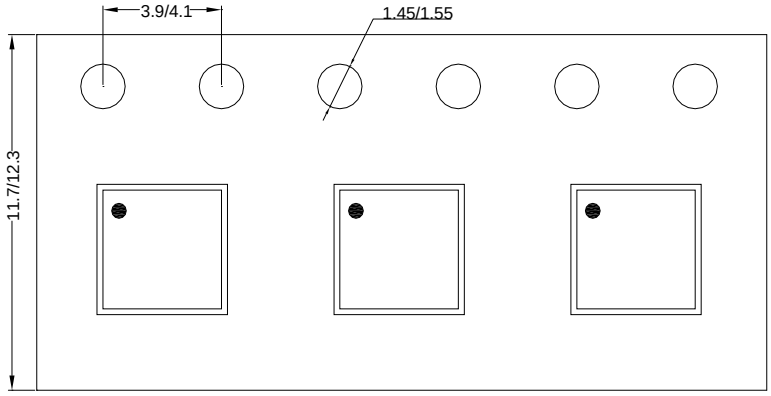
Detail A
Pin1 identifier: two options

Bottom View

Notes: All dimensions are in millimeters and exclude mold flash & metal burr.

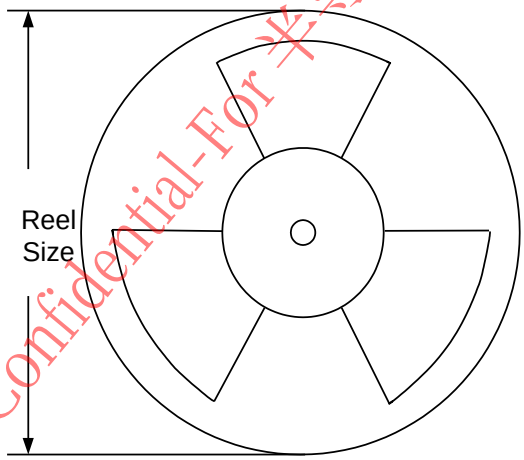
Taping & Reel Specification

1. DFN3×3-10 taping orientation



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN3×3	10	8	13"	400	400	5000