SY8003A1

High Efficiency, 1.5MHz, 3A Synchronous Step Down Regulator

General Description

The SY8003A1 is a high efficiency 1.5MHz synchronous step down DC/DC regulator, which is capable of delivering up to 3A output current. It can operate over a wide input voltage range from 2.5V to 5.5V and integrate main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The low output voltage ripple, the small external inductor and the capacitor sizes are achieved with 1.5MHz switching frequency.

Ordering Information

SY8003 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY8003A1DFC	DFN2×2-8	--

Features

- 2.5V to 5.5V Input Voltage Range
- 50μA Low Quiescent Current
- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom) 130mΩ /85mΩ
- High Switching Frequency 1.5MHz Minimizes the External Components
- Internal Soft-start Limits the Inrush Current
- 100% Dropout Operation
- Hic-cup for Short Circuit Protection
- Power Good Indicator
- Output Auto Discharge Function
- RoHS Compliant and Halogen Free
- Compact Package: DFN2×2-8

Applications

- Set Top Box
- USB Dongle
- Media Player
- Smart phone

Typical Applications

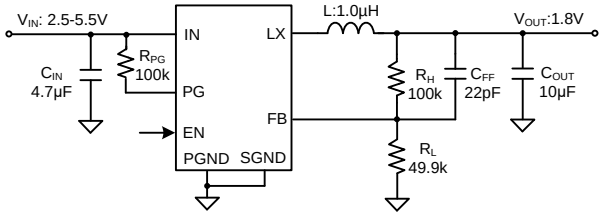


Figure1. Schematic Diagram

Inductor and C_{OUT} Selection Table

V_{OUT} [V]	L [μH]	C_{OUT} [μF]			
		4.7	10	22	2×22
1.2/ 1.8 /3.3	0.47		√	√	√
	1.0		☆	√	√
	2.2			√	√

Note: '☆' means recommended for most applications.

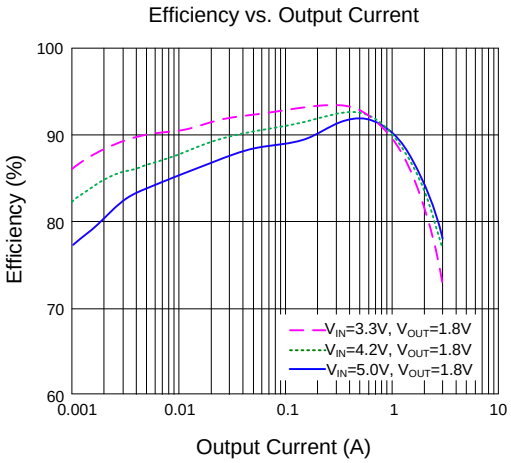
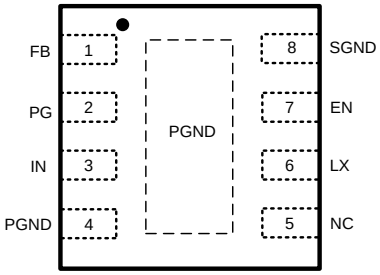


Figure2. Efficiency vs. Output Current

Pinout (Top View)



(DFN2×2-8)

Top Mark: rD*xyz* (device code: rD, ***x=year code, y=week code, z= lot number code)***

Pin Name	Pin Number	Pin Description
FB	1	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.6\times(1+R_H/R_L)$.
PG	2	Power good indicator (Open drain output). Low if the output < 90% of regulation voltage or >120% regulation voltage; High otherwise. Connect a pull-up resistor to the input.
IN	3	Input pin. Decouple this pin to the GND pin with at least a 4.7μF ceramic capacitor.
PGND	4/Exposed Paddle	Power ground pin.
NC	5	No connection.
LX	6	Inductor pin. Connect this pin to the switching node of the inductor.
EN	7	Enable control. Pull high to turn on. Do not leave it floating.
SGND	8	Signal ground pin.

Block Diagram

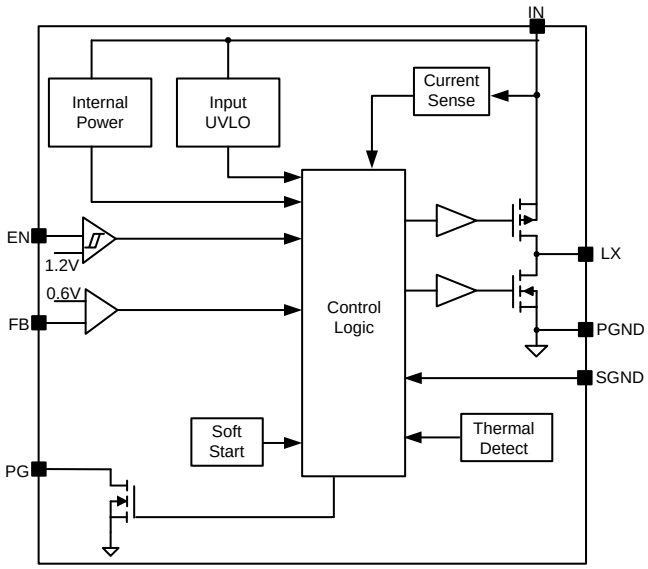


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- -0.3V to 6.0V
PG, FB, EN Voltage---------- -0.3V to V_{IN}+0.6V
LX Voltage---------- -0.3V(*1) to 6.0V(*2)
Power Dissipation, P_D @ T_A = 25°C ----------1W
Package Thermal Resistance (Note 2)
θ_{JA} ----------100°C/W
θ_{JC} ----------50°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
(*1) LX Voltage Tested Down to -3V<40ns
(*2) LX Voltage Tested Up to +7V<40ns

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 2.5V to 5.5V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 5V, V_{OUT} = 1.8V, L = 1.0μH, C_{OUT} = 10μF, T_A = 25°C, unless otherwise specified)

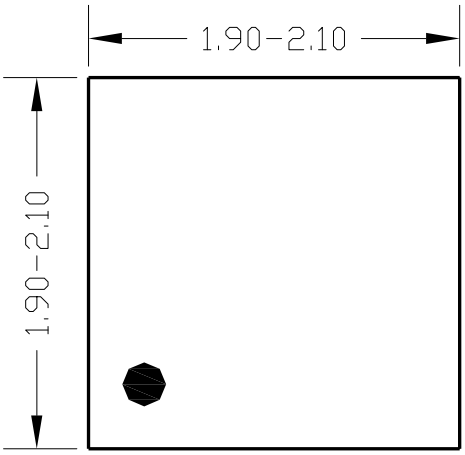
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.5		5.5	V
Input UVLO Threshold	V_{UVLO}				2.5	V
Input UVLO Hysteresis	V_{HYS}			150		mV
Quiescent Current	I_Q	V_{FB}=V_{REF}×105%		50	70	μA
Shutdown Current	I_{SHDN}	V_{EN}=0V		0.1	1	μA
Feedback Reference Voltage	V_{REF}		591	600	609	mV
LX Node Discharge Resistance	R_{DIS}			50		Ω
Top FET R_{ON}	$R_{DS(ON)1}$			130		mΩ
Bottom FET R_{ON}	$R_{DS(ON)2}$			85		mΩ
EN Input Voltage High	$V_{EN,H}$		1.2			V
EN Input Voltage Low	$V_{EN,L}$				0.4	V
PG Threshold for Under Voltage Detection	$V_{PG,UVP}$			90		%V_{REF}
PG Low Delay Time for Under Voltage Detection	$t_{UVP,DLY}$			20		μs
PG Threshold for Over Voltage Detection	$V_{PG,OVP}$			120		%V_{REF}
PG Low Delay Time for Over Voltage Detection	$t_{OVP,DLY}$			20		μs
Min ON Time	$t_{ON,MIN}$			60		ns
Maximum Duty Cycle	D_{MAX}		100			%
Turn On Delay	$t_{ON,DLY}$	from EN high to LX start switching		0.5		ms
Soft-start Time	t_{SS}	V_{OUT} from 0% to 100%		1		ms
Switching Frequency	f_{SW}			1.5		MHz
Top FET Current Limit	$I_{LMT,TOP}$		3.5			A
Thermal Shutdown Temperature	T_{SD}			160		°C
Thermal Shutdown Hysteresis	T_{HYS}			20		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

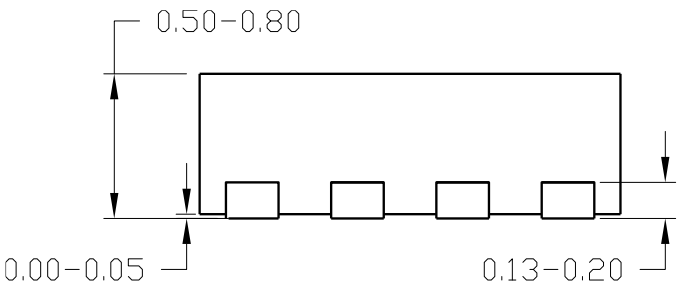
Note 2: θ_{JA} of SY8003A1 is measured in the natural convection at T_A = 25ºC on a 2OZ two-layer Silergy evaluation board. Paddle of DFN2×2-8 package is the case position for θ_{JC} measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

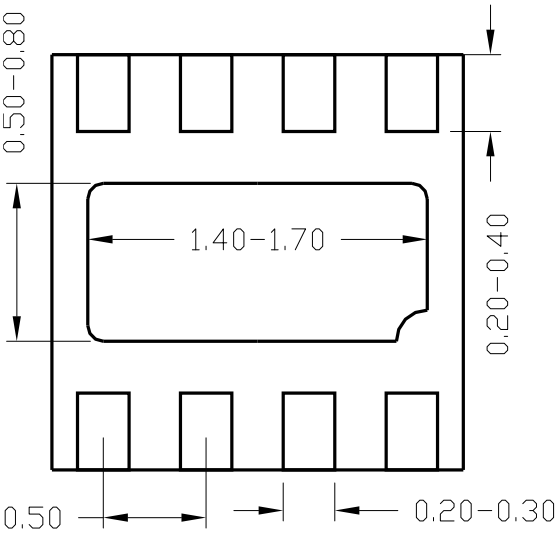
DFN2x2-8 Package Outline



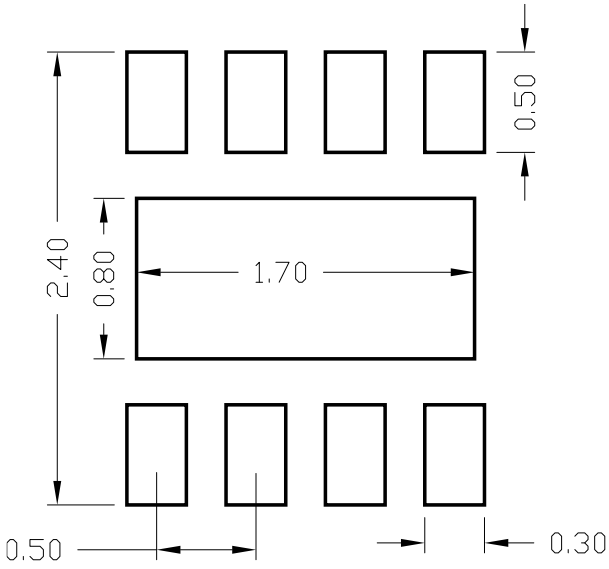
Top View



Side View



Bottom View

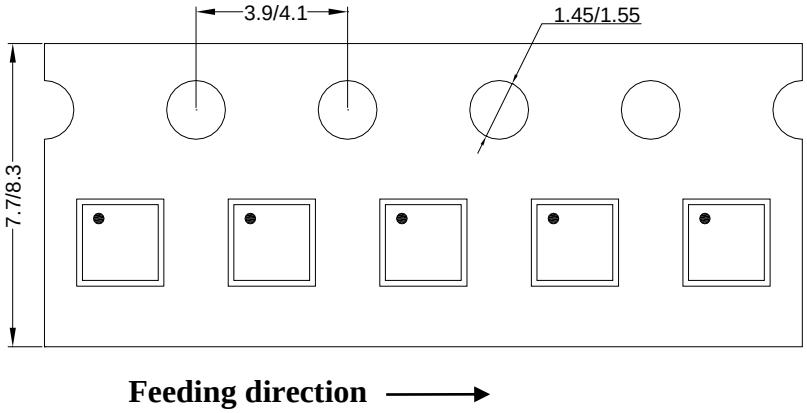


PCB Layout (Reference Only)

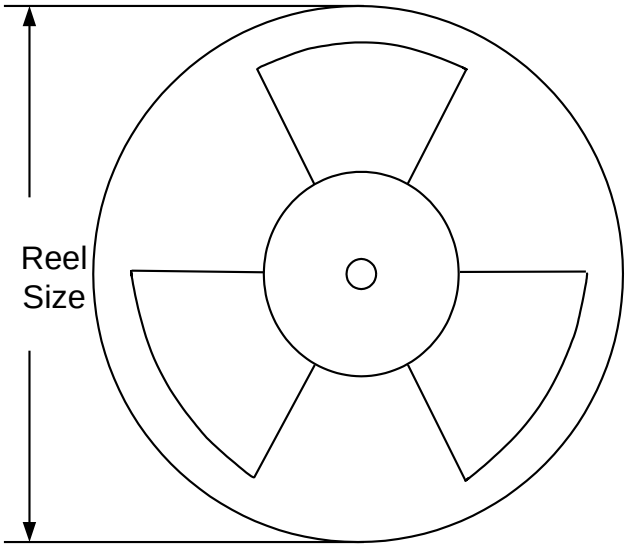
Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

1. DFN2×2



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN2×2	8	4	7"	400	160	3000

3. Others: NA