Application Note: SY8301

High Efficiency, 1A 40V Input Synchronous Step Down Regulator

General Description

The SY8301 develops a high efficiency synchronous step-down DC/DC converter capable of delivering 1A load current. The SY8301 operates over a wide input voltage range from 4.5V to 40V and integrates main switch and synchronous switch with low $R_{DS(ON)}$ to minimize the conduction loss.

The SY8301 adopts peak current control scheme. The switching frequency is 2MHz. Low output voltage ripple and small external inductor and capacitor sizes are achieved with 2MHz switching frequency.

The device also features ultra low quiescent operating to achieve high efficiency under light load. And the internal soft-start limits inrush current during power on.

Ordering Information

SY8301 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY8301ABC	SOT23-6	--

Features

- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom):380mΩ/180mΩ
- 4.5-40V Input Voltage Range
- 1A Output Current Capability
- 2MHz Fixed Switching Frequency
- 0.8V±1.0% Reference Voltage
- Low Quiescent Current
- Internal Soft-start Limits the Inrush Current
- Hic-cup Mode Output Short Circuit Protection
- Thermal Shutdown and Auto Recovery
- Compact Package: SOT23-6

Applications

- LCD-TV
- SetTop Box
- Notebook
- Storage
- High Power AP Router
- Networking

Typical Applications

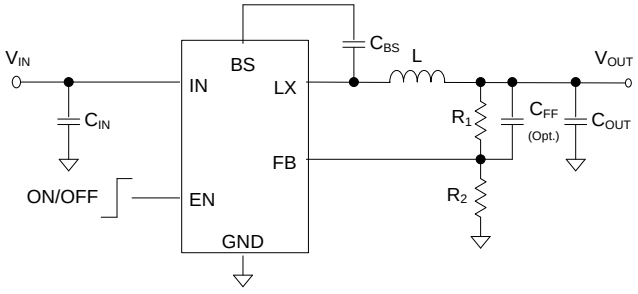


Figure1. Schematic Diagram

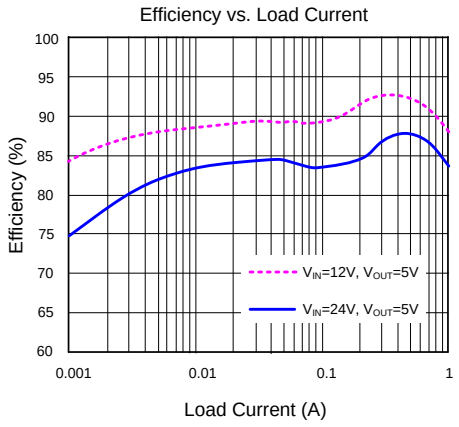
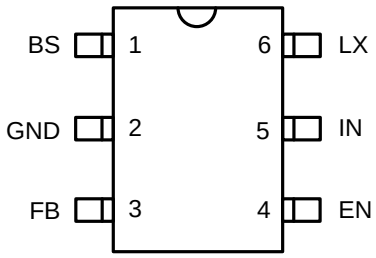


Figure2. Efficiency

Pinout (top view)



Top Mark: **Iu*xyz*** **(**Device code: Iu; ***x=year code, y=week code, z= lot number code*****)**

Pin Name	Pin Number	Pin Description
BS	1	Boot-strap pin. Supply high side gate driver. Connect a 0.1μF ceramic capacitor between the BS and the LX pin .
GND	2	Ground pin.
FB	3	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: V_{OUT}=0.8× (1+R1/R2)
EN	4	Enable control pin. Pulling this pin high to turn on the IC. Do not leave this pin floating.
IN	5	Input pin. Decouple this pin to the GND pin with at least a 1μF ceramic capacitor.
LX	6	Inductor pin. Connect this pin to the switching node of the inductor.

Block Diagram

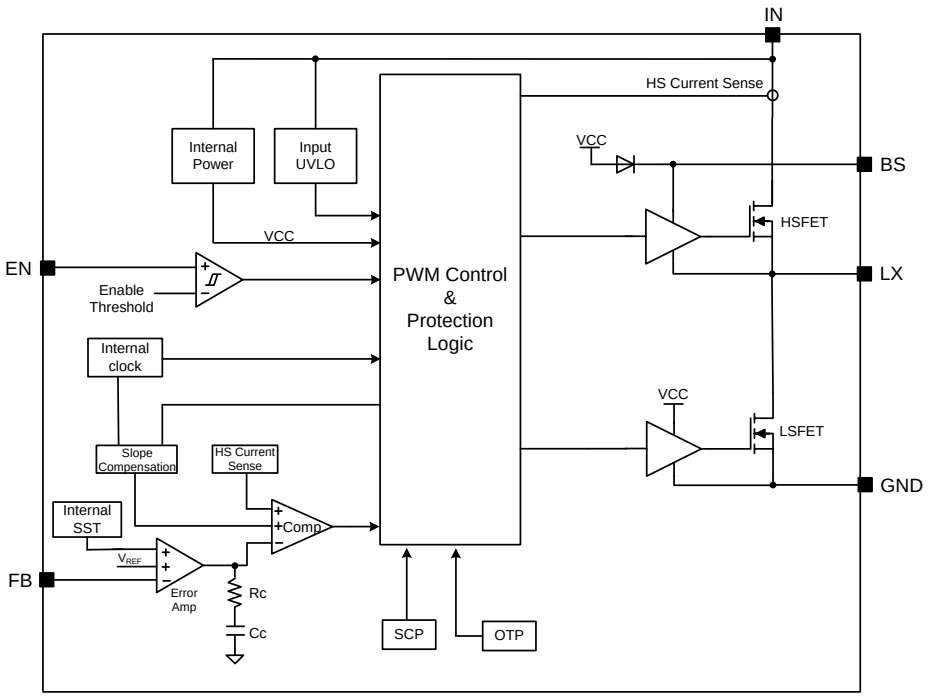


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- -0.3 to 40V
LX, FB, EN Voltage ---------- -0.3 to 40V
BS-LX Voltage---------- -0.3 to 4V
Power Dissipation, P_D @ T_A = 25°C SOT23-6---------- 0.4W
Package Thermal Resistance (Note 2)
θ_{JA} ----------100°C/W
θ_{JC} ---------- 30°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
Dynamic LX Voltage in 10ns Duration ---------- IN+3V to GND -5V

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 4.5V to 40V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, I_{OUT}=1A, unless otherwise specified)

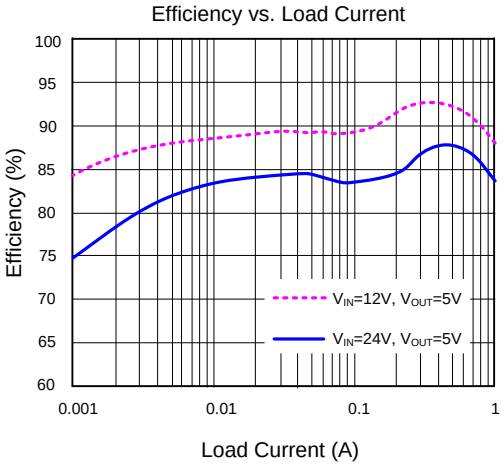
Parameter	symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.5		40	V
Input UVLO Threshold	V_{UVLO_R}		3.6	4	4.4	V
Input UVLO Hysteresis	V_{HYS}			0.6		V
Quiescent Current	I_Q	I_{OUT}=0,V_{FB}=V_{REF}×105%	12	22	28	μA
Shutdown Current	I_{SHDN}	EN=0		1	2	μA
Feedback Reference Voltage	V_{REF}		0.792	0.8	0.808	V
FB Input Current	I_{FB}	V_{FB}=3.3V	-50		50	nA
Top FET RON	$R_{DS(ON),TOP}$			380		mΩ
Top FET Peak Current Limit	$I_{LIM,TOP}$		1.6		2.5	A
Bottom FET RON	$R_{DS(ON),BOT}$			180		mΩ
EN Rising Threshold	V_{ENH}		1.4			V
EN Falling Threshold	V_{ENL}				1	V
Soft-start Time	t_{SS}			1		ms
Switching Frequency	f_{SW}		1.6	2	2.4	MHz
Output UVP Threshold	V_{UVP}			50		%V_{REF}
Output UVP Wait Time	t_{WAIT}			60		μs
Min ON Time	t_{ON}			80		ns
Min OFF Time	t_{OFF}			100		ns
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C

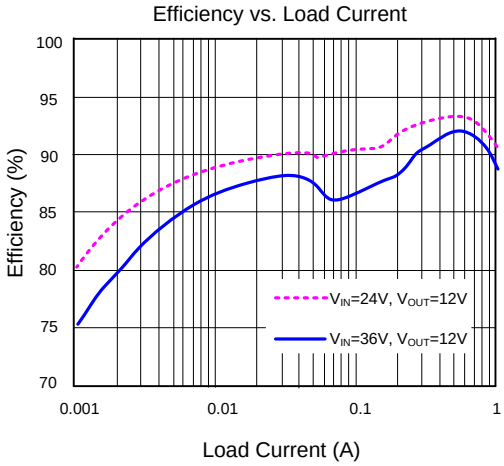
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

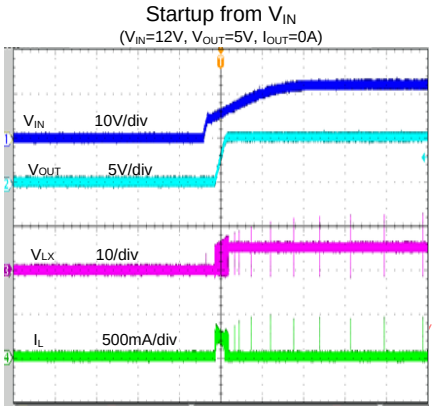
Note 2: Package thermal resistance is measured in the natural convection at T_A = 25°C on a two-layer Silergy Evaluation Board.

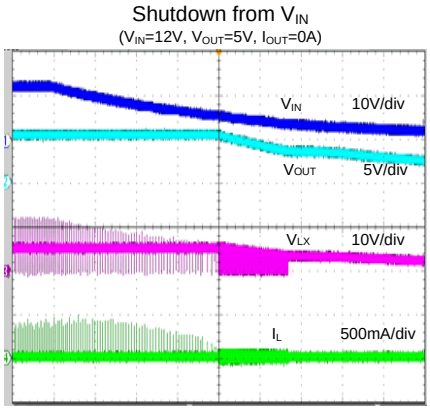
Note 3: The device is not guaranteed to function outside its operating conditions.

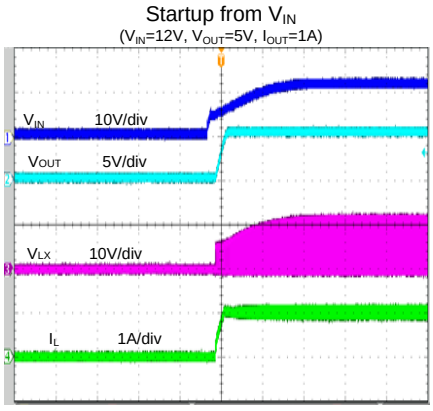
Typical Performance Characteristics

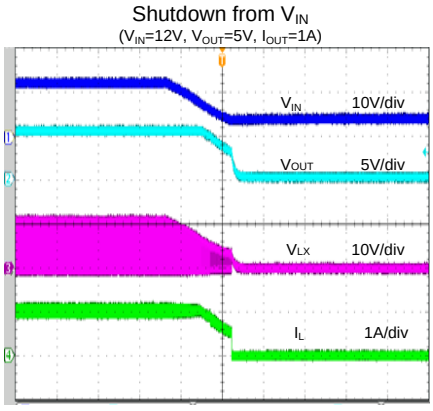






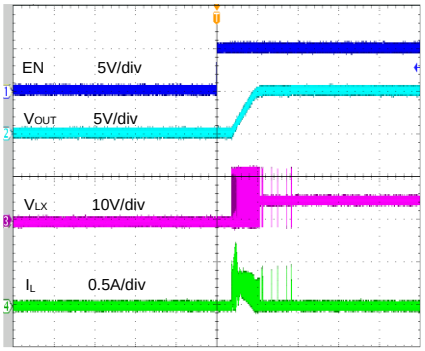






Startup from Enable

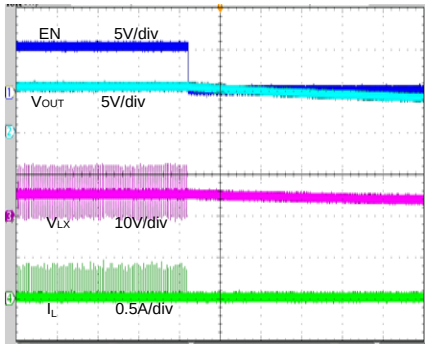
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0A)



Time (800μs/div)

Shutdown from Enable

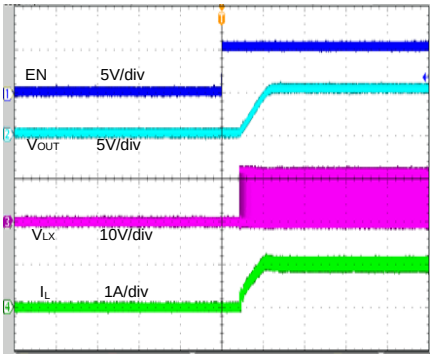
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0A)



Time (100ms/div)

Startup from Enable

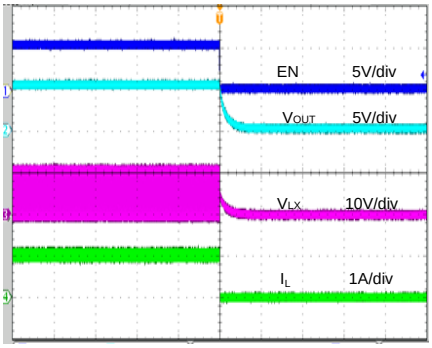
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=1A)



Time (800μs/div)

Shutdown from Enable

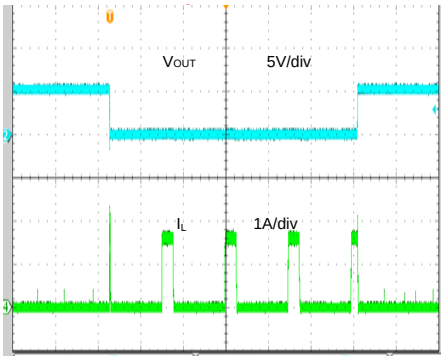
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=1A)



Time (800μs/div)

Short Circuit Protection

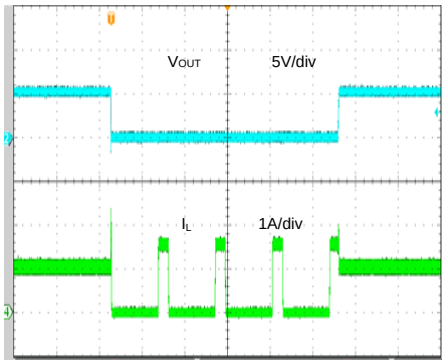
(V_{IN}=12V, V_{OUT}=5V, 0A to Short)



Time (4ms/div)

Short Circuit Protection

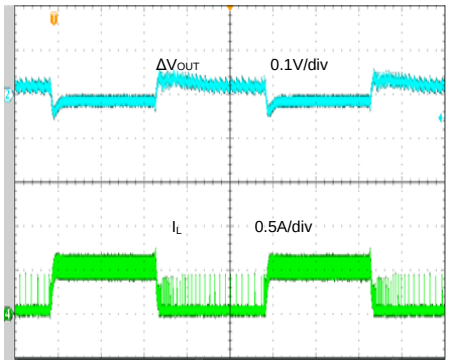
(V_{IN}=12V, V_{OUT}=5V, 1A to Short)



Time (4ms/div)

Load Transient

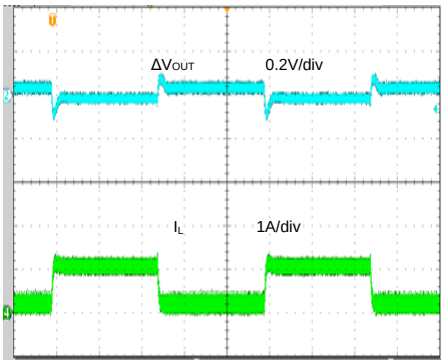
(V_{IN}=12V, V_{OUT}=5V, 0A to 0.5A)



Time (200μs/div)

Load Transient

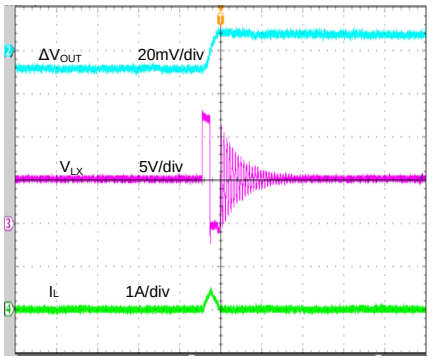
(V_{IN}=12V, V_{OUT}=5V, 0.1A to 1A)



Time (200μs/div)

Output Ripple

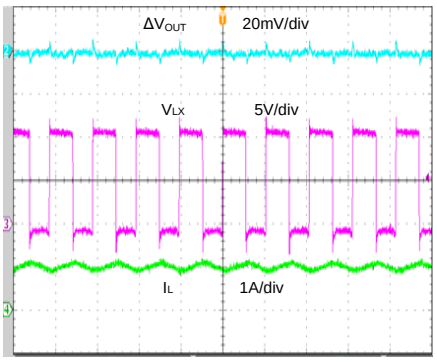
(V_{IN}=12V, V_{OUT}=5V, I_{OUT}=0A)



Time (2μs/div)

Output Ripple

(V_{IN}=12V, V_{OUT}=5V, I_{OUT}= 1A)



Time (400ns/div)

Operation

The SY8301 develops a high efficiency synchronous step-down DC/DC converter capable of delivering 1A load current. The SY8301 operates over a wide input voltage range from 4V to 40V and integrates main switch and synchronous switch with low $R_{DS(ON)}$ to minimize the conduction loss.

The SY8301 adopts peak current control scheme. The switching frequency is 2MHz. Low output voltage ripple and small external inductor and capacitor sizes are achieved with 2MHz switching frequency.

The device also features ultra low quiescent operating to achieve high efficiency under light load. And the internal soft-start limits inrush current during power on.

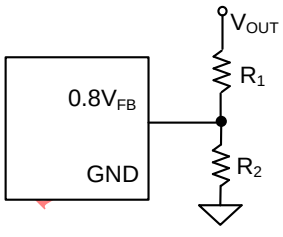
Applications Information

Because of the high integration in the SY8301, the application circuit based on this regulator is rather simple. Only the input capacitor C_{IN}, the output capacitor C_{OUT}, the output inductor L and the feedback resistors (R_1 and R_2) need to be selected for the targeted applications specifications.

Feedback Resistor Dividers R_1 and R_2:

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10kΩ and 1MΩ is highly recommended for both resistors. If V_{OUT} is 3.3V, R_1=100k is chosen, then using following equation, R_2 can be calculated to be 32k:

$$R_2 = \frac{0.8V}{V_{OUT}-0.8V} R_1 .$$



Input Capacitor C_{IN}

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D(1-D)} .$$

To minimize the potential noise problem, a typical X5R or a better grade ceramic capacitor should be placed really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins. In this case, a 4.7µF low ESR ceramic capacitor is recommended.

Output Capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use an X5R or a better grade ceramic capacitor greater than 22µF capacitance.

Output Inductor L

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{f_{SW} \times I_{OUT,MAX} \times 40\%}$$

Where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY8301 is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

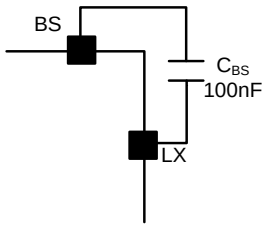
$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mΩ to achieve a good overall efficiency.

External Bootstrap Capacitor

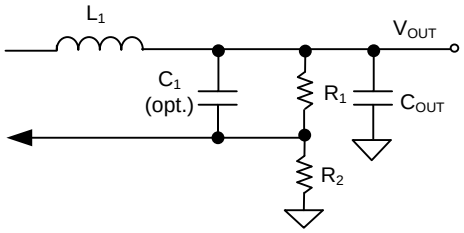
This capacitor provides the gate driver voltage for internal high side MOSEFET. A 100nF low ESR

ceramic capacitor connected between the BS pin and the LX pin is recommended.



Load Transient Considerations

The SY8301 integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a ceramic cap in parallel with R_1 may further speed up the load transient response and it is recommended for applications with large load transient step requirements.



Short Circuit Protection:

The SY8301 integrates hic-cup mode short circuit protection function. If the device V_{OUT} drops below 50% of the set-point, the short-circuit protection mode will be initiated. The device will shut down for approximately 5ms, and then restart with a complete soft-start cycle that is approximately 1ms. If the short circuit condition remains, another 'hic-cup' cycle of shutdown and restart will continue indefinitely.

Over Temperature Protection (OTP)

The SY8301 includes over temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will shut down switching operation when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 15°C, the IC will resume normal operation with a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the OTP threshold.

Layout Design

The layout design of the SY8301 is relatively simple. For the best efficiency and minimum noise problem, the following components should be placed close to the IC: C_{IN}, L_1, R_1 and R_2.

1) It is desirable to maximize the PCB copper area connecting to the GND pin to achieve the best thermal and noise performance. If the board space allows, a ground plane is highly desirable.

2) C_{IN} must be close to the pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

3) The PCB copper area associated with the LX pin must be minimized to avoid the potential noise problem.

4) The components R_1 and R_2 and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull-down 1MΩ resistor between the EN and the GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

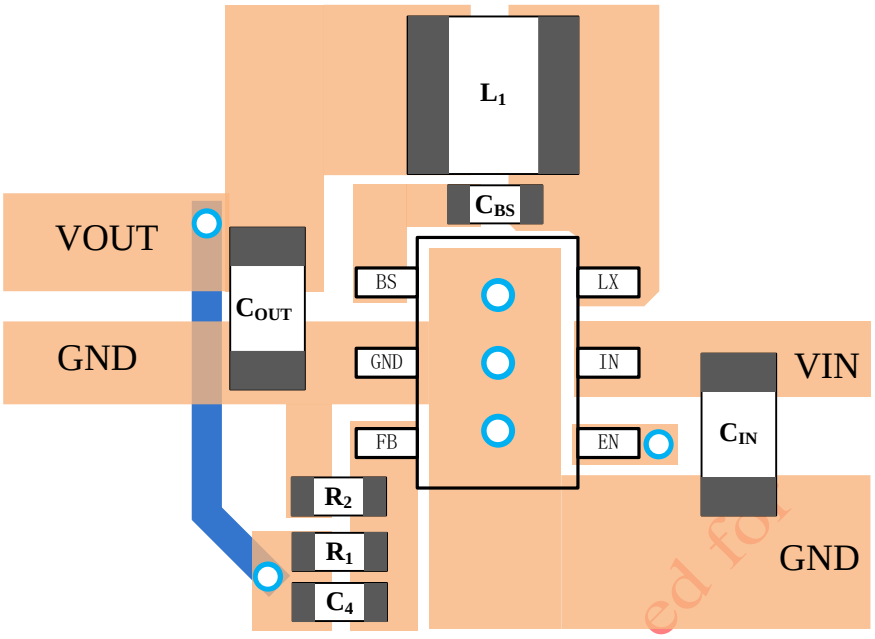
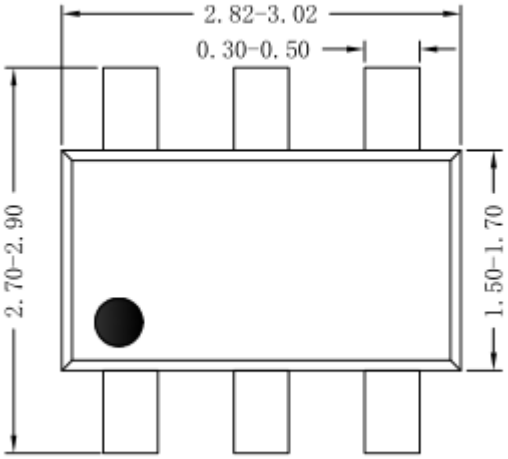
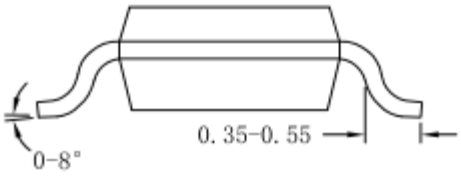


Figure4. PCB Layout Suggestion

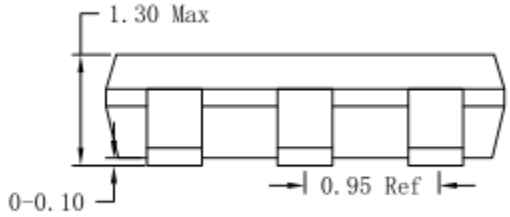
SOT23-6 Package Outline & PCB Layout



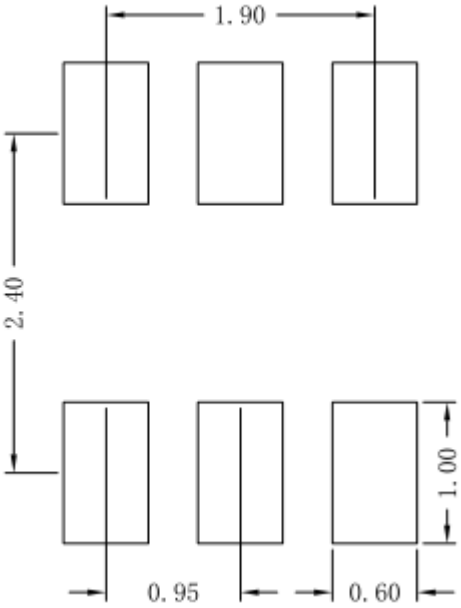
Top View



Side View



Side View



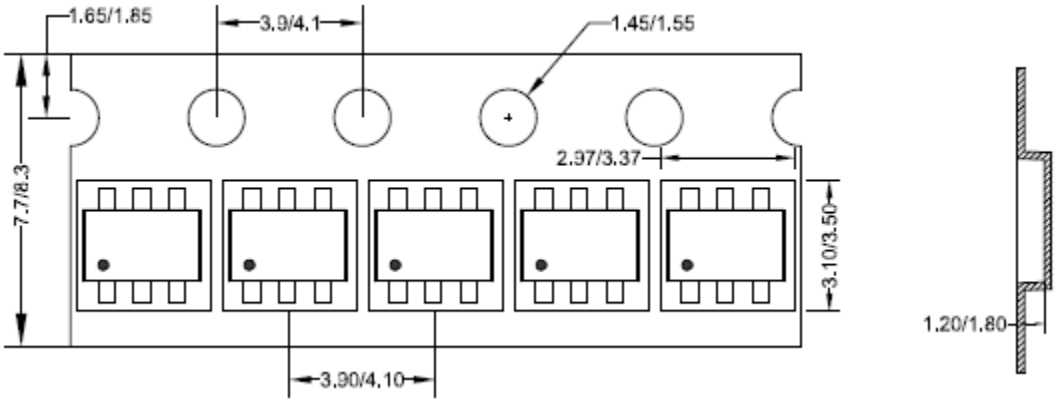
Recommended Pad Layout

Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

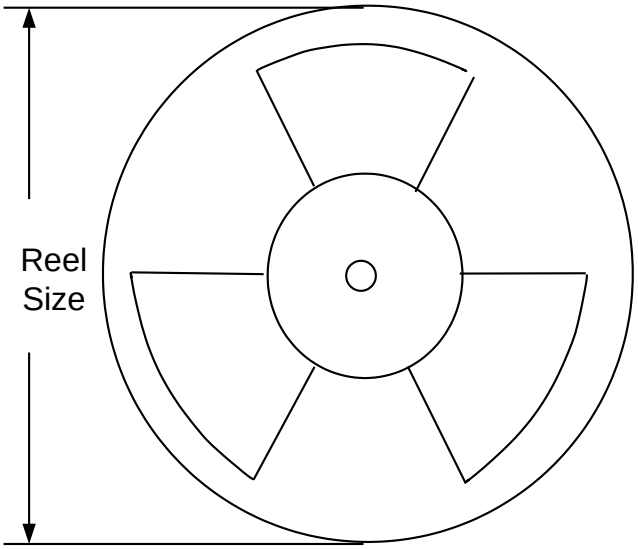
1. Taping orientation

SOT23-6



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOT23-6	8	4	7"	280	160	3000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Nov.16, 2018	Revision 0.9	Initial Release
Jun.08, 2020	Revision 0.9A	Update in the EC table (page 4) 1. The max value of the Input UVLO Threshold changes from 4.2V to 4.4V; 2. The typical value of the Quiescent Current changes from 18μA to 22μA, max value changes from 24μA to 28μA.

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