



SILERGY

SY83088C

High Efficiency Fast Response, 8A, 28V Input, Fixed 5.1V Output Synchronous Buck Converter with 100mA 5V LDO

General Description

The SY83088C develops a high efficiency synchronous Buck converter capable of delivering 8A current. It integrates the top MOSFET and the bottom MOSFET with very low $R_{DS(ON)}$ to minimize the conduction loss. In addition, it operates at pseudo-constant frequency of 600kHz under CCM condition to minimize the size of inductor and capacitor. The SY83088C also provides a fixed 5V LDO with 100mA current capability, which can be used to power the external peripherals. The 5V LDO can switch to Buck converter output to reduce power loss.

Silergy's constant on-time and ripple-based control strategy supports high input/output voltage ratios (low duty cycles), and fast transient response while maintaining a near constant operating frequency over line, load and output voltage ranges. This control method provides stable operation without complex compensation and even with low ESR ceramic capacitors.

The SY83088C operates over a wide input voltage range from 5.5V to 24V. Cycle-by-cycle current limit, input under voltage lockout, internal soft-start, output under voltage protection, over voltage protection and over temperature protection provide safe operation in all operating conditions.

Features

- Low $R_{DS(ON)}$ for Internal MOSFETs: 20mΩ Top, 10mΩ Bottom
- Wide Input Voltage Range: 5.5V ~ 24V
- Fixed 5.1V Output Voltage
- Large Duty Cycle On-Time Stretch
- 8A Continuous Output Current Capability
- 100mA LDO Current Capability
- 600kHz Pseudo-Constant Frequency
- $\pm 1.5\%$ Internal Reference Voltage
- Internal 0.8ms Soft-Start Limits the Inrush Current
- Constant On-Time and Ripple-Based Control to Achieve Fast Transient Responses
- Integrated 1.5Ω Bypass Switch
- PFM/USM Selectable Light Load Operation Mode
- Power Good Indicator
- Output Auto-Discharge Function
- Cycle-by-Cycle Valley and Peak Current Limit Protection
- Latch-Off Mode Output Under Voltage Protection for Buck
- Latch-Off Mode Output Over Voltage Protection for Buck
- Latch-Off Mode Over Temperature Protection for Buck
- Auto-Recovery Mode Output Under Voltage Protection for LDO
- Auto-Recovery Mode Over Temperature Protection for LDO
- Input Under Voltage Lockout(UVLO)
- RoHS Compliant and Halogen Free
- Compact Package: QFN2.5x2.5-16

Applications

- LCD-TV/Net-TV/3D-TV
- Set Top Box
- Notebook
- High Power AP

Typical Applications

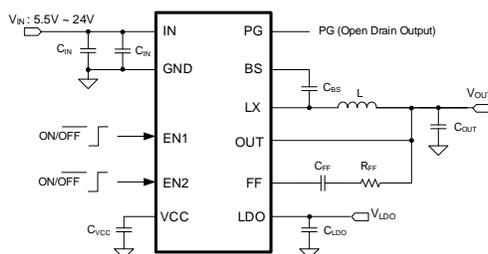


Figure1. Schematic Diagram

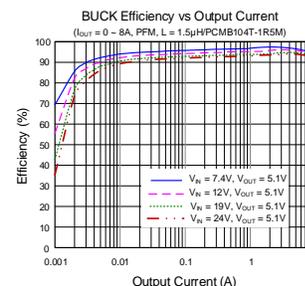


Figure2. Buck Efficiency vs. Output Current

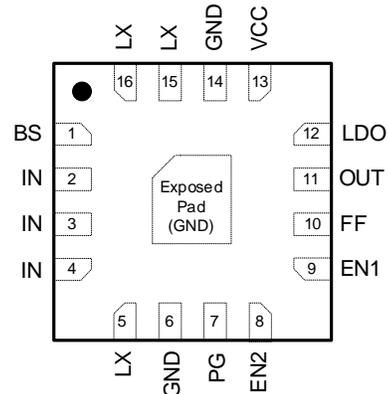


Ordering Information

Ordering Number	Package type	Top Mark
SY83088CRHC	QFN2.5×2.5-16 RoHS Compliant and Halogen Free	GBExyz

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	BS	Bootstrap pin. Supply top FET gate driver. Connect a 0.1 μ F ceramic capacitor between the BS pin and the LX pin.
2, 3, 4	IN	Input pin. Decouple this pin to the GND pin with at least a 10 μ F ceramic capacitor. A 0.1 μ F input ceramic capacitor is recommended to reduce the input noise.
5, 15, 16	LX	Inductor pin. Connect this pin to the switching node of the inductor.
6, 14, EP	GND	Ground pin.
7	PG	Power good indicator pin. Open drain output when the output voltage is within 90% to 120% of the regulated value.
8	EN2	Enable control pin of the device and internal LDO. Pull this pin high to turn on the device and internal LDO. Pull this pin low to turn off the device and LDO. Do not leave this pin floating.
9	EN1	Enable control pin of the Buck converter. Pull this pin high to turn on the Buck converter. Pull this pin low to turn off the Buck converter. Do not leave this pin floating. The pin is also used for controlling operation mode of the Buck converter under light load condition after its output is within the regulated range. When its voltage is lower than 1.6V and higher than 1V, the Buck converter works under ultra-sonic mode. When its voltage is higher than 2.2V, the Buck converter works under PFM mode.
10	FF	Output feedforward pin. Connect the RC network to this pin from the node of output capacitors closest to the inductor.
11	OUT	Output pin. Connect this pin with output capacitors where you want to regulate the voltage. The pin also provides the bypass input for 5V LDO.
12	LDO	5V LDO output pin. Decouple this pin to ground with at least a 4.7 μ F ceramic capacitor.
13	VCC	Internal 3.6V LDO output pin. Power supply for internal analog circuits and driving. Decouple this pin to ground with at least a 2.2 μ F ceramic capacitor.



Block Diagram

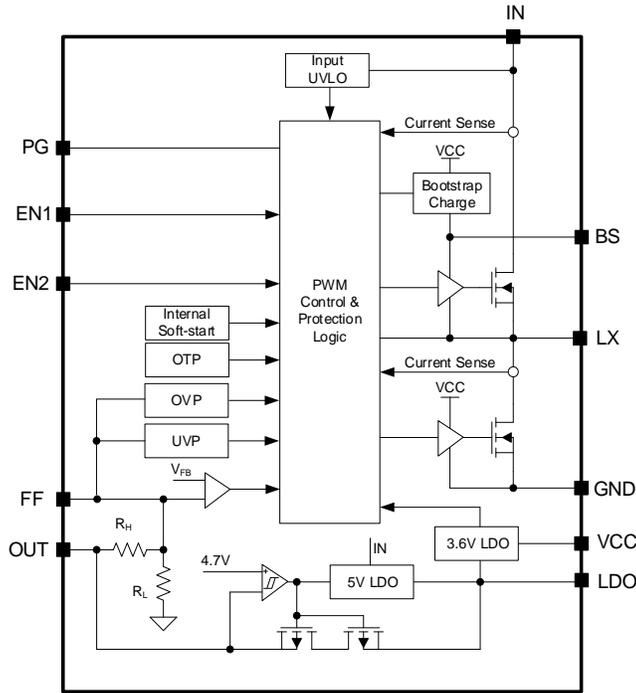


Figure3. Block Diagram

Absolute Maximum Ratings

Parameter (Note1)	Min	Max	Unit
IN	-0.3	28	V
IN-LX, LX, PG, EN2, EN1	-0.3	26	
BS-LX, VCC, FF	-0.3	4	
OUT, LDO	-0.3	6.5	
LX, 10ns Duration	-5	29	
LX, 20ns Duration	-1	28	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	33	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	5.5	
P_D Power Dissipation $T_A = 25^\circ\text{C}$	3	W

Recommended Operating Conditions

Parameter (Note3)	Min	Max	Unit
IN	5.5	24	V
Buck Output Current		8	A
LDO Output Current		100	mA
Ambient Temperature	-40	85	°C
Junction Temperature	-40	125	



Electrical Characteristics

(V_{IN} = 12V, C_{OUT} = 66μF, C_{FF} = 470pF, R_{FF} = 1kΩ, T_J = 25°C, I_{OUT} = 1A unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input	Voltage Range	V _{IN}	5.5		24	V	
	UVLO Threshold	V _{IN,UVLO}	V _{IN} rising		5		
	UVLO Hysteresis	V _{IN,HYS}		0.5			
	Quiescent Current	I _Q	I _{OUT} = 0A, EN2 = EN1 = High, V _{OUT} = V _{SET} × 105%		96	120	μA
	Shutdown Current 1	I _{SHDN1}	EN1 = Low, EN2 = High		60	85	
	Shutdown Current 2	I _{SHDN2}	EN1 = Low, EN2 = Low		6	9	
Output	Voltage Set-Point	V _{SET}	CCM	5.023	5.1	5.177	V
	Discharge Current	I _{DIS}	V _{OUT} = 5.1V		100		mA
	Soft-Start Time	t _{SS}	V _{OUT} from 0% to 100% V _{SET}		0.8		ms
	OVP Threshold	V _{OVP}	V _{FB} rising	117	120	123	%V _{REF}
	OVP Hysteresis	V _{OVP,HYS}			5		
	OVP Delay	t _{OVP,DLY}	(Note4)	30	40		μs
	UVP Threshold	V _{UVP}		55	60	65	%V _{REF}
	UVP Delay	t _{UVP,DLY}	(Note4)		200		μs
MOSFET	Top FET R _{DS(ON)}	R _{DS(ON),TOP}		20			mΩ
	Bottom FET R _{DS(ON)}	R _{DS(ON),BOT}		10			
	Top FET Current Limit Threshold	I _{LMT,TOP}			20		A
	Bottom FET Current Limit Threshold	I _{LMT,BOT}		10			
	Bottom FET Reverse Current Limit Threshold	I _{LMT,RVS}	USM mode	3	4.8		
Enable (EN)	Input Voltage High	V _{EN,H}	1			V	
	Input Voltage Low	V _{EN,L}			0.4		
	EN1 Voltage for Ultra-Sonic Mode	V _{EN1,USM}	1		1.6		
	EN1 Voltage for PFM Mode	V _{EN1,PFM}	2.2		V _{IN}		
	De-Glitch Time	t _{EN,DG}	(Note4)		40		μs
Frequency	Switching Frequency	f _{SW}	CCM	510	600	690	kHz
	Ultra-Sonic Mode Frequency	f _{USM}	USM mode, I _{OUT} = 0A	20			
	Minimum On-Time	t _{ON,MIN}			50		ns
	Minimum Off-Time	t _{OFF,MIN}			150		
Power Good	Rising Threshold	V _{PG,R}	V _{FB} rising (good)	87	90	93	%V _{REF}
	Falling Threshold	V _{PG,F}	V _{FB} falling (not good)	80	83	86	
	Delay Time	t _{PG,R}	Low to high (Note4)		200		μs
		t _{PG,F}	EN1 = High, High to low (Note4)		40		
	Low Voltage	V _{PG,LOW}	V _{FB} = 0V, I _{PG} = 5mA			0.45	V
VCC	Output Voltage	V _{CC}	VCC adds 1mA load	3.45	3.6	3.75	V



Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
LDO	Output Voltage	V _{LDO}	Bypass switch turns off, I _{LDO} = 0mA	4.85	5	5.15	V
	Dropout Voltage	V _{DROPOUT}	I _{LDO} = 100mA		300		mV
	Output Current Limit Threshold	I _{LMT,LDO}		150		310	mA
BYP	R _{DS(ON)}	R _{DS(ON),BYP}			1.5		Ω
	Turn on Voltage	V _{BYP}		4.5	4.7	4.95	V
	Turn on Hysteresis	V _{BYP,HYS}			0.2		
	OVP Voltage	V _{BYP,OVP}	V _{OUT} sweeps	114	120	126	%V _{LDO}
OTP	Buck Temperature	T _{OTP,BUCK}	T _J rising (Note4)		150		°C
	Buck Temperature Hysteresis	T _{BUCK,HYS}	T _J falling (Note4)		15		
	LDO Temperature	T _{OTP,LDO}	(Note4)		160		
	LDO Temperature Hysteresis	T _{LDO,HYS}	(Note4)		25		

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Note 2: Package thermal resistance is measured in the natural convection at T_A = 25°C on a 8.5cm×8.5cm size, four-layer Silergy Evaluation Board with 2-oz copper.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Guaranteed by design.

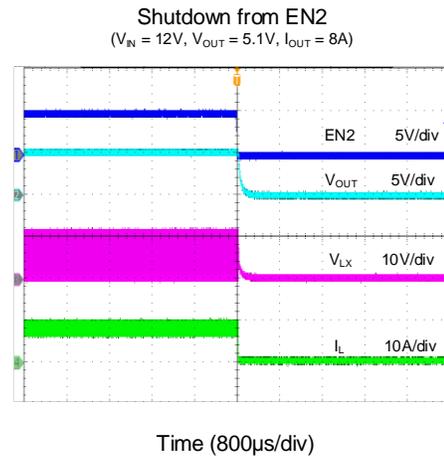
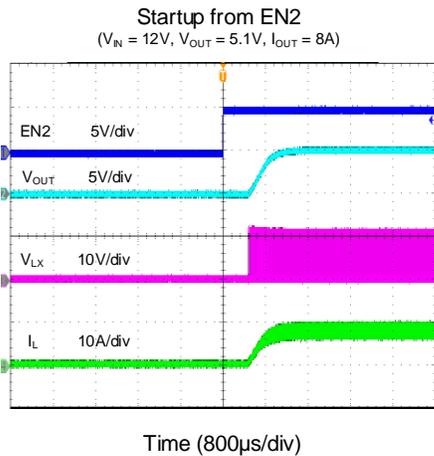
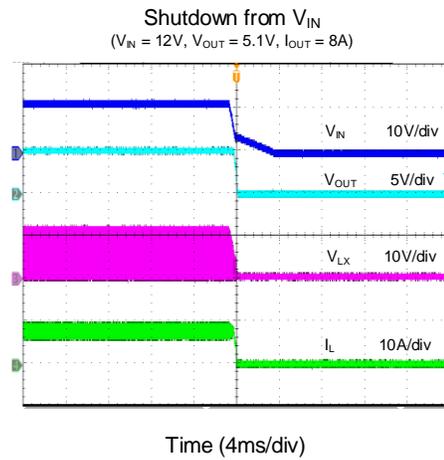
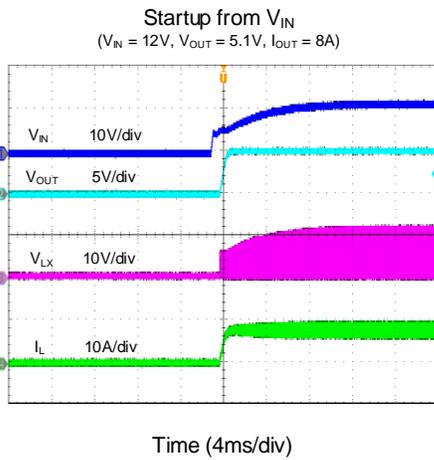
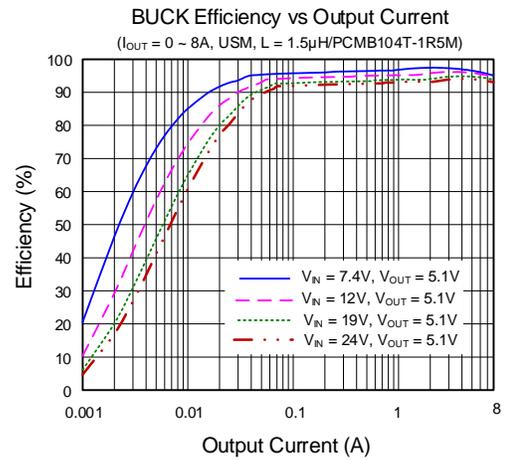
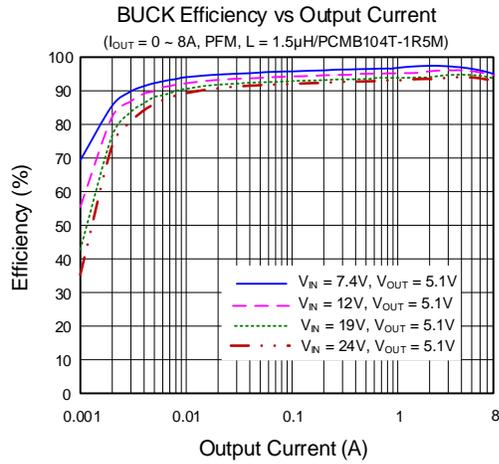


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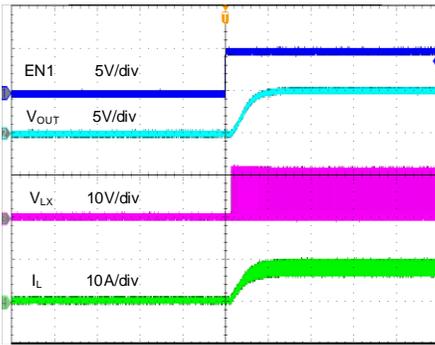
SY83088C

Typical Performance Characteristics

($T_A = 25^\circ\text{C}$, $V_{IN} = 12\text{V}$, $V_{OUT} = 5.1\text{V}$, $L = 1.5\mu\text{H}$, $C_{OUT} = 66\mu\text{F}$, $C_{FF} = 470\text{pF}$, $R_{FF} = 1\text{k}\Omega$, unless otherwise specified)

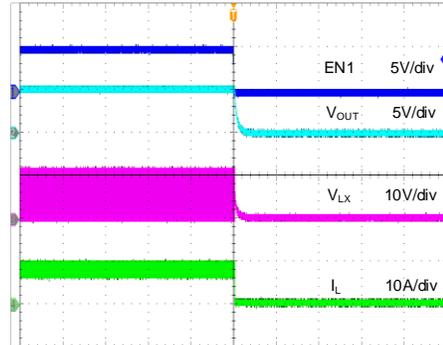


Startup from EN1
 $(V_{IN} = 12V, V_{OUT} = 5.1V, I_{OUT} = 8A)$



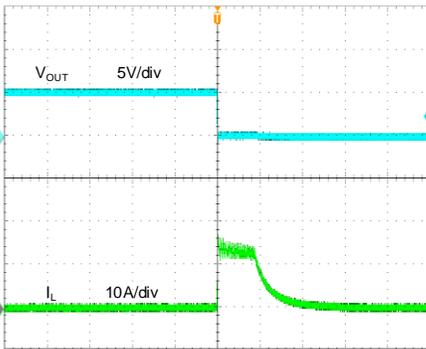
Time (800μs/div)

Shutdown from EN1
 $(V_{IN} = 12V, V_{OUT} = 5.1V, I_{OUT} = 8A)$



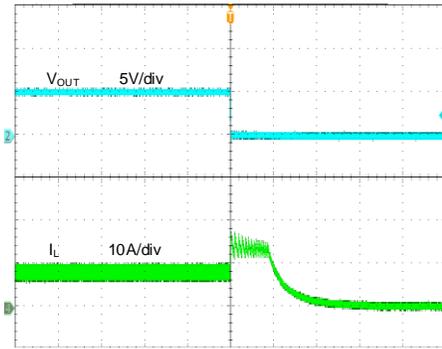
Time (800μs/div)

Output Short Circuit Protection
 $(V_{IN} = 12V, V_{OUT} = 5.1V, I_{OUT} = 0A \sim \text{Short})$



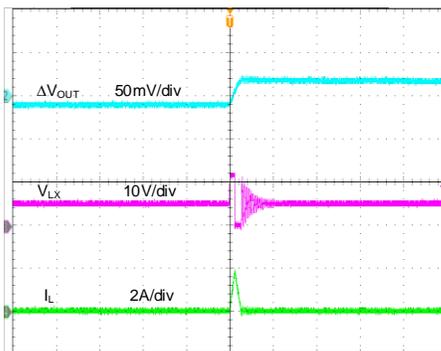
Time (200μs/div)

Output Short Circuit Protection
 $(V_{IN} = 12V, V_{OUT} = 5.1V, I_{OUT} = 8A \sim \text{Short})$



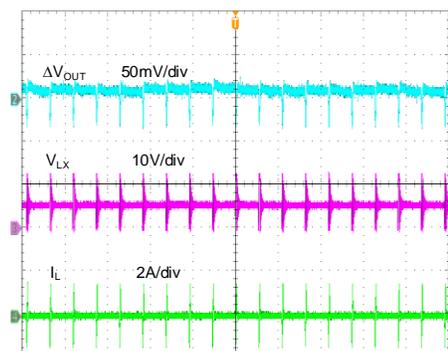
Time (200μs/div)

Output Ripple
 $(V_{IN} = 12V, V_{OUT} = 5.1V, I_{OUT} = 0A, \text{PFM})$



Time (4μs/div)

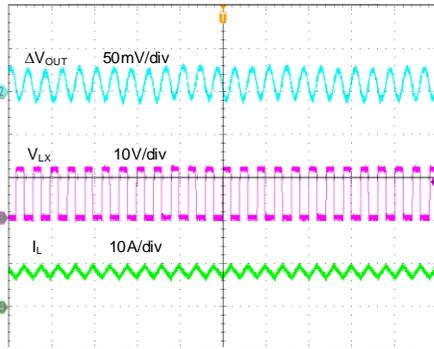
Output Ripple
 $(V_{IN} = 12V, V_{OUT} = 5.1V, I_{OUT} = 0A, \text{USM})$



Time (40μs/div)

Output Ripple

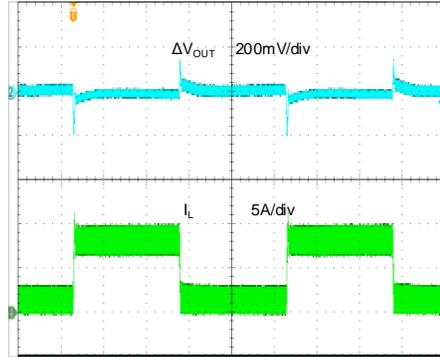
($V_{IN} = 12V$, $V_{OUT} = 5.1V$, $I_{OUT} = 8A$)



Time (4 μ s/div)

Load Transient

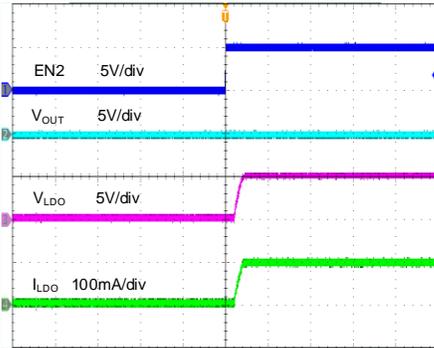
($V_{IN} = 12V$, $V_{OUT} = 5.1V$, $I_{OUT} = 0.8 - 8A$)



Time (200 μ s/div)

LDO Startup from EN2

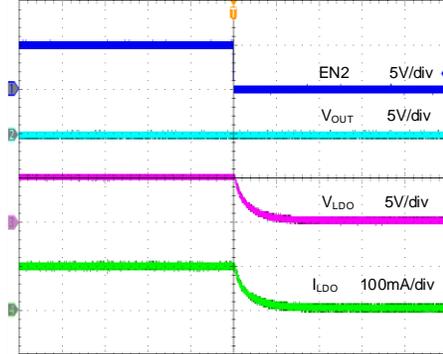
($V_{IN} = 12V$, $I_{LDO} = 100mA$, $EN1 = Low$)



Time (800 μ s/div)

LDO Shutdown from EN2

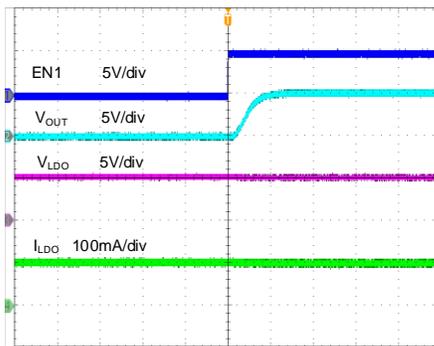
($V_{IN} = 12V$, $I_{LDO} = 100mA$, $EN1 = Low$)



Time (800 μ s/div)

LDO Switchover When EN1 ON

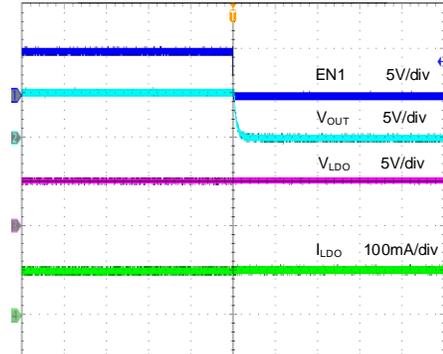
($V_{IN} = 12V$, $V_{OUT} = 5.1V$, $I_{OUT} = 8A$, $I_{LDO} = 100mA$, $EN2 = High$)



Time (800 μ s/div)

LDO Switchover When EN1 OFF

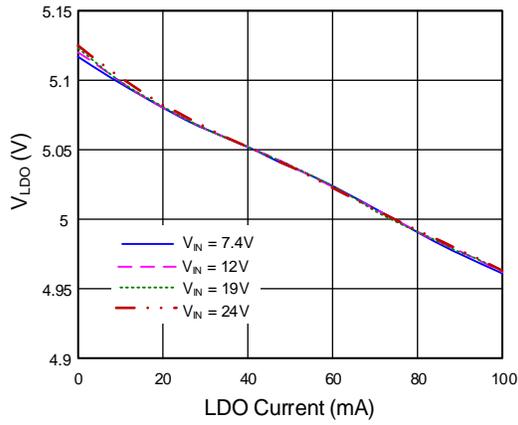
($V_{IN} = 12V$, $V_{OUT} = 5.1V$, $I_{OUT} = 8A$, $I_{LDO} = 100mA$, $EN2 = High$)



Time (800 μ s/div)

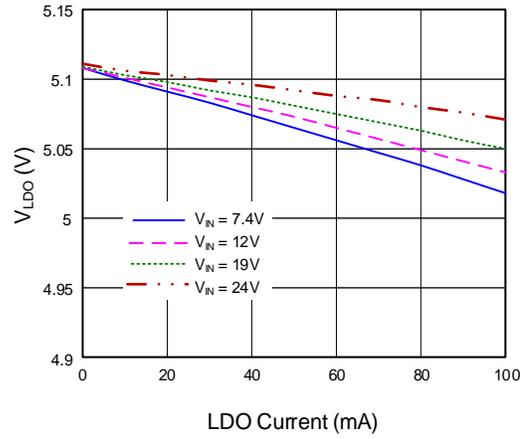
LDO Load Regulation

(EN2 = High, EN1 = High, bypass switch turns on)



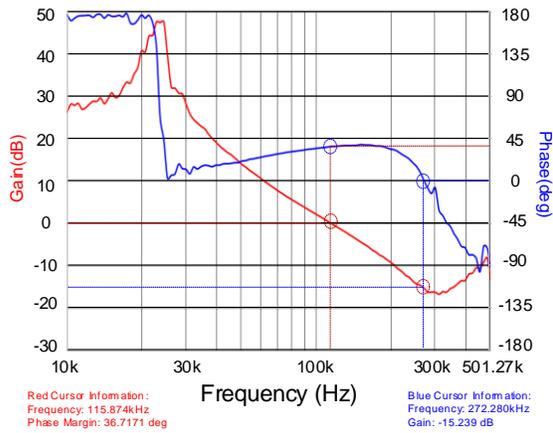
LDO Load Regulation

(EN2 = High, EN1 = Low, bypass switch turns off)



Bode Plot

(V_{IN} = 20V, V_{OUT} = 5.1V, I_{OUT} = 4A)





Detailed Description

General Features

Constant On-Time Architecture

Fundamental to any constant on-time (COT) architecture is the one-shot circuit or on-time generator, which determines how long to turn on the top FET. Each on-time (t_{ON}) is a “fixed” voltage ration,

$$t_{ON} = \left(\frac{V_{OUT}}{V_{IN}}\right) \times \left(\frac{1}{f_{SW}}\right)$$

For example, considering that a hypothetical converter targets 5.1V output from a 12V input at 600kHz, the target on-time is

$$\frac{5.1V}{12V} \times \frac{1}{600kHz} = 708.33ns$$

Each t_{ON} pulse is triggered by the feedback comparator when the output voltage as measured at FB node drops below the regulated value. After one t_{ON} period, a minimum off-time ($t_{OFF,MIN}$) is imposed before any further switching is initiated, even if the output voltage is lower than the regulated value. This approach avoids making any switching decisions during the noisy periods just after switching events and while the switching node (LX) is rapidly rising or falling.

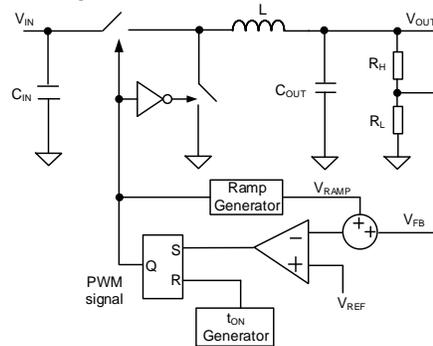
In a COT architecture, there is no fixed clock, so the top FET can turn on almost immediately after a load transient and subsequent switching pulses can be quickly initiated, ramping the inductor current up to meet load requirements with minimal delays. Traditional current mode or voltage mode control methods must simultaneously monitor the feedback voltage, current feedback and internal ramps and compensation signals to determine when to turn off the top FET and turn on the bottom FET. Considering these small signals in a switching environment are difficult to be noise-free after transmitting large current, making those architectures difficult to apply in noisy environments, even under low duty cycle operation.

Minimum Duty Cycle and Maximum Duty Cycle

In the COT architecture, there is no limitation for small duty cycle, since at very low duty cycle operation, once the on-time is close to the minimum on-time, the switching frequency can be reduced as needed to always ensure a proper operation.

Under $T_J = -40^{\circ}C \sim 125^{\circ}C$ condition, the Buck converter can support 5.1V fixed output even the input voltage is as low as 5.5V.

Instant-PWM Operation



Silergy's COT ripple-based control strategy adds several proprietary improvements to the traditional COT architecture. Whereas most legacy based on COT implementations require a dedicated connection to the output voltage terminal to calculate the t_{ON} duration, instant-PWM control method derives this signal internally. Another improvement optimizes operation with low ESR ceramic output capacitors. In many applications it is desirable to utilize very low ESR ceramic output capacitors, but legacy COT converters may become unstable in these cases because the beneficial ramp signal that results from the inductor current flowing into the output capacitor maybe become too small to maintain stable operation. For this reason, instant-PWM synthesizes a virtual replica of this signal internally. This internal virtual ramp and the feedback voltage are combined and compared to the reference voltage. When the sum is lower than the reference voltage, the t_{ON} pulse is triggered as long as the minimum off-time has been satisfied and the inductor current as measured in the bottom FET is lower than the bottom FET current limit threshold. As the t_{ON} pulse is triggered, the bottom FET turns off and the top FET turns on. Then the inductor current ramps up linearly during the t_{ON} period. At the conclusion of the t_{ON} period, the top FET turns off, the bottom FET turns on and the inductor current ramps down linearly. This action also initiates the minimum off-time timer to ensure sufficient time for stabilizing any transient conditions and settling the feedback comparator before the next cycle is initiated. This minimum off-time is relatively short so that during fast speed load transient t_{ON} can be retrIGGERED with minimal delay, allowing the inductor current to ramp quickly to provide sufficient energy to the load side.

In order to avoid shoot-through, a dead time (t_{DEAD}) is generated internally between the top FET off and the bottom FET on period or the bottom FET off and the top FET on period.

Light Load Operation Mode Selection

PFM or USM light load operation is selected by EN1 pin. EN1 is not only Buck converter enable pin but also mode selection pin to control operation mode of the Buck converter under light load condition after its output is within the regulated range. If the voltage on this pin is lower than 1.6V and higher than 1V, the Buck converter works under ultra-sonic mode (USM). If the voltage on this pin is higher than 2.2V, the Buck converter works under pulse-frequency modulation mode (PFM).

If PFM light load operation is selected, under light load conditions, typically

$$I_{OUT} < \frac{1}{2} \times \Delta I_L$$

the current through the bottom FET will ramp to near zero before the next t_{ON} time. When this occurs, the bottom FET turns off, preventing recirculation current that can seriously reduce efficiency under these light load conditions. As load current is further reduced, the combined feedback and ramp signals remain much higher than the reference voltage, the instant-PWM control loop will not trigger another t_{ON} until needed, so the apparent operating switching frequency will correspondingly drop, further enhancing efficiency. The switching frequency can be lower than audible frequency area under deep light load or null load conditions. Continuous conduction mode (CCM) resumes smoothly as soon as the load current increases sufficiently for the inductor current to remain above zero at the time of the next t_{ON} cycle. The Buck converter enters CCM once the load current exceeds the critical level. After that, the switching frequency stays fairly constant over the output current range. The critical level of the load current is determined with

$$I_{OUT_CTL} = \frac{\Delta I_L}{2} = \frac{V_{OUT} \times (1 - D)}{2 \times f_{SW} \times L}$$

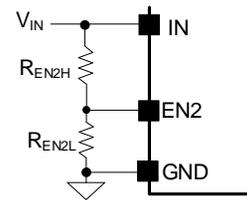
If USM light load operation is selected, it keeps the switching frequency above an audible frequency area even under deep light load or null load conditions. Once the Buck converter detects that both the top FET and the bottom FET turn off for more than one certain time, it forces the bottom FET turn on in advance of one t_{ON} cycle and discharge the output capacitor electric quantity so that the switching frequency is out of audio range. There is also one feedback loop to match the bottom FET forced turn on time with the error amplifier output voltage to avoid output voltage becoming much higher than regulated value.

Input Under Voltage Lockout (UVLO)

To prevent operation before the internal circuitry is ready and to ensure that the top and bottom FETs can be sufficiently enhanced, the device incorporates one input undervoltage lockout protection.

The device remains in a low current state and LX switching actions and LDO are inhibited until V_{IN} exceeds its own UVLO (rising) threshold. At that time, if EN2 is high, the LDO will be built up, then if EN1 is also high, the Buck converter will startup by initiating a soft-start ramp. If V_{IN} falls below $V_{IN,UVLO}$ less than the input UVLO hysteresis, LX switching actions and LDO will again be suppressed.

If the input UVLO threshold is low for some high input UVLO threshold requirement applications, use EN2 to adjust the input UVLO by adopting two external divided resistors.



EN2/EN1 Control

The SY83088C has two enable pins to control the Buck converter and LDO.

The Buck converter and LDO are all turned off under S4/S5 state (EN2 = Low, EN1 = High or Low). Under S3 state (EN2 = High, EN1 = Low), only LDO is turned on while the Buck converter is turned off. Under S0 state (EN2 = High, EN1 = High), the Buck converter and LDO are all turned on. Only if EN2 is high could LDO be turned on, and only if EN1 and EN2 are both high could the Buck converter be turned on. See EN2/EN1 logic details in below table.

EN2	EN1	STATE	LDO	Buck
High	High	S0	On	On
High	Low	S3	On	Off
Low	Low/High	S4/S5	Off	Off

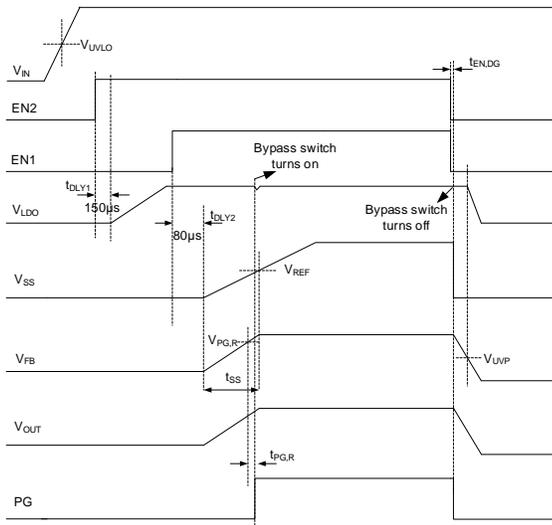
The EN2/EN1 input is a high-voltage capable input with logic-compatible threshold. When EN2/EN1 is driven $> 1V$, normal device will be turned on. When driven $< 0.4V$, the device will be turned off, reducing the input current to $< 9\mu A$.

It is not recommended to connect EN2 or EN1 and IN directly. A resistor in a range of $1k\Omega$ to $1M\Omega$ should be used if EN2/EN1 is pulled high by IN.

Startup and Shutdown

The SY83088C incorporates an internal soft-start circuit to smoothly ramp the Buck converter output to the desired voltage whenever the Buck converter is enabled. Internally, the soft-start circuit clamps the output at a low

voltage and then allows the output to rise to the desired voltage over approximately 0.8ms, which avoids high current flow and transients during startup. The startup and shutdown sequence chart is shown below.



After V_{IN} exceeds its own UVLO (rising) threshold, the internal LDO regulator is turned on after the delay time t_{DLY1} if EN2 is high, the Buck converter is turned on after the delay time t_{DLY2} if EN1 is also high. When the output voltage is 90% of the regulated value, PG is in the high-impedance state after the delay time $t_{PG,R}$, and at the same time, LDO output switches to the Buck output if the output voltage is higher than bypass switch turn on voltage. LDO output will switch to internal LDO regulator once either EN2 or EN1 is low.

If the output is pre-biased to a certain voltage before startup, the Buck converter disables the switching of both the top FET and the bottom FET until the internal soft-start voltage V_{SS} exceeds the output sensed voltage at the FB node.

Buck Output Power Good Indicator

The Buck power good indicator is an open drain output controlled by a window comparator connected to the feedback signal. If V_{FB} is higher than $V_{PG,R}$ and less than V_{OVP} for at least the power good delay time (low to high), PG will be in the high-impedance state.

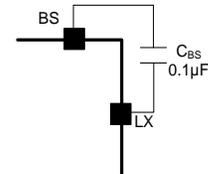
PG should be connected to V_{IN} or another voltage source through a resistor (e.g., 100k Ω). After V_{IN} rises until the internal initial power is ready, the PG FET is turned on so that PG is pulled to GND before output voltage is ready. After feedback voltage V_{FB} reaches $V_{PG,R}$, PG is pulled high (after the delay time typical 200 μ s). When V_{FB} drops to $V_{PG,F}$, or rises to V_{OVP} for the OVP delay time, PG is pulled low (after the delay time typical 40 μ s).

Buck Output Auto-Discharge Function

The SY83088C discharges the output voltage when the Buck converter shuts down from V_{IN} or EN2/EN1, or latch-off, so that output voltage can be discharged in a minimal time, even Buck output load current is zero. The discharge FET in parallel with the bottom FET turns on after the bottom FET turns off when shut down logic is triggered. The output discharge current is typically 100mA under $V_{OUT} = 5.1V$ condition. Note that the discharge FET is not active beyond these shutdown conditions.

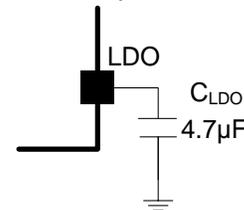
External Bootstrap Capacitor

This device integrates a floating power supply for the gate driver of the top FET. Proper operation requires a 0.1 μ F low ESR ceramic capacitor to be connected between BS and LX. This bootstrap capacitor provides the gate driver supply voltage for the N-channel top FET.



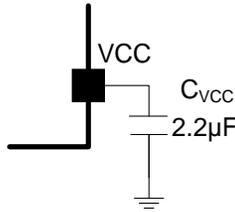
LDO Output

The SY83088C integrates one high performance, low drop-out linear regulator (LDO) and its output voltage set-point is fixed 5V, which can not only power the internal 3.6V VCC, but also power the external peripheries with 100mA capability. This LDO is intended mainly for an auxiliary 5V supply for the notebook system in standby time. Once the input voltage exceeds its own UVLO (rising) threshold, and EN2 is high, LDO is turned on and supplied power by V_{IN} . After the EN1 is also high, until the output voltage exceeds bypass switch turn on voltage and at the same time PG is in the high-impedance state, the internal LDO regulator will be turned off and the bypass switch will be turned on so that LDO output switch to output voltage to reduce power consumption. Connect a 4.7 μ F low ESR ceramic capacitor from LDO to GND.



VCC Linear Regulator

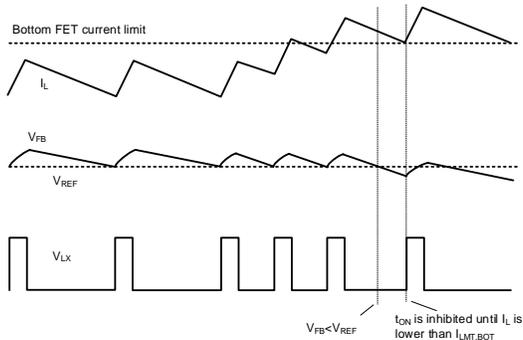
The SY83088C integrates one high performance, low drop-out linear regulator 3.6V VCC, which can power the internal gate drivers, PWM logic, analog circuitry and other blocks. VCC is supplied by LDO. Connect a 2.2 μ F low ESR ceramic capacitor from VCC to GND. Make sure the loop formed by VCC capacitor is shorter than LDO capacitor if there is position conflict between them.



Fault Protection Modes

Buck Output Current Limit

The Buck converter features cycle-by-cycle “valley” current limit (bottom FET current limit). Inductor current is monitored in the bottom FET when it turns on and as the inductor current ramps down. If the monitored current is higher than the bottom FET current limit threshold, t_{ON} is inhibited until the current returns back to the limit threshold or lower.



When the valley current limit occurs, the output current limit value is

$$I_{LMT,OUT} = I_{LMT,BOT} + \frac{\Delta I_L}{2}$$

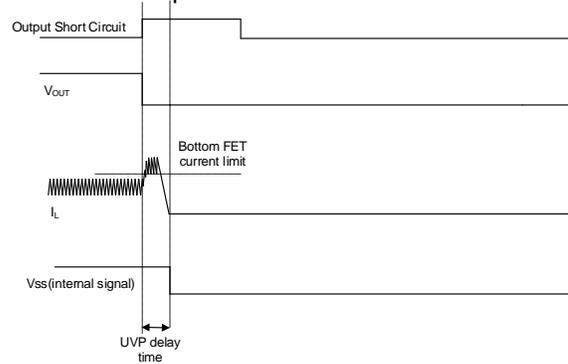
$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

The valley current limit protection limits the inductor current but the OCP itself is one non-latch protection. When the load current is higher than the bottom FET current limit threshold by one half of the peak-to-peak inductor ripple current, the output voltage starts to drop. Once the feedback voltage falls lower than the under voltage protection (UVP) threshold and continues for the UVP delay time, the Buck converter will enter latch off status. On the other hand, over temperature protection may also be triggered under the over current condition and the Buck converter will enter latch off status, too.

The Buck converter also features cycle-by-cycle “peak” current limit (top FET current limit). During t_{ON} time, the top FET current is monitored. If the monitored current exceeds the top FET current limit threshold, the top FET will be turned off, the bottom FET will be turned on. t_{ON} can be not inhibited any more once bottom FET current is lower than the bottom FET current limit threshold.

Buck Output Under Voltage Protection (UVP)

If $V_{OUT} < \sim 60\%$ of the regulated value for approximately 200µs occurring when the output short circuit or the load current is much heavier than the maximum current capacity, the output under voltage protection (UVP) will be triggered, and the Buck converter will latch off. Reset EN2 or EN1 input to re-enable the Buck converter.



Buck Output Over Voltage Protection (OVP)

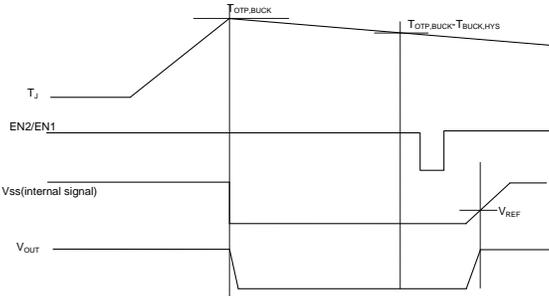
The Buck converter includes output over voltage protection (OVP). If the feedback voltage rises above the reference voltage level, the top FET naturally remains off and different actions are adopted in different operation mode.

When operating in PFM light load mode, if the feedback voltage remains high, the bottom FET remains on until the inductor current reaches zero and the LX node switching actions are suppressed. If the feedback voltage doesn't exceed over voltage protection threshold, the LX node switching actions will be recovered once the combined feedback and ramp signals become lower than the reference voltage. If the feedback voltage exceeds over voltage protection threshold and lingers for the OVP delay time, and the output voltage exceeds bypass switch OVP voltage, the output over voltage protection (OVP) will be triggered, and the Buck converter will enter latch off status. Reset EN2 or EN1 input to re-enable the Buck converter.

When operating in USM light load mode, if the feedback voltage remains high, the bottom FET forced turn on time will be longer and inductor current average value becomes more and more negative until the reverse current limit is triggered, trying to make output voltage lower. If the feedback voltage exceeds the over voltage protection threshold and lingers for the OVP delay time, and the output voltage exceeds bypass switch OVP voltage, the output over voltage protection (OVP) will be triggered, and the Buck converter will enter latch off status. Reset EN2 or EN1 input to re-enable the Buck converter. False OVP may happen under USM light load condition if the inductance value is chosen too low.

Buck Over Temperature Protection (OTP)

The Buck converter includes over temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. When the Buck thermal sensor detects the Buck junction temperature exceeds 150°C, the over temperature protection (OTP) will be triggered, and the Buck converter will enter latch off status (LDO is still alive). Recycling EN2 or EN1 input to re-enable the Buck converter after the junction temperature cools down about 15°C.



LDO Output Current Limit

The device features LDO current limit to guarantee LDO safe operation in all operating conditions. Once the LDO output voltage is less than its regulated value after LDO is turned on, the internal LDO regulator or bypass switch will work under current limit condition until the LDO output voltage is within its regulated range. For example, when the LDO output short circuit occurs, the LDO will work in a current limit status. LDO output voltage can recover after the short circuit condition is removed.

LDO Over Temperature Protection

The device also features auto-recovery mode LDO over temperature protection to guarantee LDO safe operation when the internal LDO regulator power loss is large. Once the LDO thermal sensor detects that LDO junction temperature exceeds 160°C, the LDO will be turned off. When the LDO junction temperature cools down by approximately 25°C, the LDO will be turned on and Buck converter will also be recovered from any latch off cases.

Design Procedure

Buck Input Capacitor Selection

Input filter capacitors are needed to reduce the ripple voltage on the input, to filter the switched current drawn from the input supply and to reduce potential EMI. When selecting the input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating above the system requirements. X5R series ceramic capacitors are most often selected due to their small size, low cost, surge current capability and high RMS current ratings over a wide temperature and voltage range. However, systems which are powered by a wall adapter or long inductive cable may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding

some bulk capacitance like electrolytic, tantalum or polymer type capacitors. Using a combination of bulk capacitors (to reduce input overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current,

$$I_{CIN,RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

The worst-case condition occurs at $D = 0.5$, then

$$I_{CIN,RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

On the other hand, the input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification. Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated by

$$V_{CIN_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1 - D)$$

The worst-case condition occurs at $D = 0.5$, then

$$V_{CIN_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. In most applications a single 10µF X5R capacitor is sufficient. Take care to locate the ceramic input capacitor as close to the device's IN and GND pin as possible.

Buck Inductor Selection

The inductor is necessary to supply constant current to the output load while being driven by the LX node switching actions.

The Buck converter operates well over a wide range of inductance values. This flexibility allows for optimization to find the best trade-off of efficiency, cost and size for a particular application. Selecting a low inductance value will help reduce size and cost and enhance transient response, but will increase peak inductor ripple current, reducing efficiency and increasing output voltage ripple. The low DC resistance (DCR) of these low inductance value inductors may help reduce DC losses and increase efficiency. On the other hand, choosing higher inductance value inductors tend to have higher DCR and will slow down transient response.

A reasonable compromise between size, efficiency, and transient response can be determined by selecting a

ripple current (ΔI_L) about 20% ~ 50% of the desired full output load current. Start calculating the approximate inductance value by selecting the input and output voltages, the operating frequency (f_{SW}), the maximum output current ($I_{OUT,MAX}$) and estimating a ΔI_L as some percentage of that current.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Use this inductance value to determine the actual inductor ripple current (ΔI_L) and required peak current inductor current $I_{L,PEAK}$.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L,PEAK} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

Select an inductor with a saturation current and thermal rating in excess of $I_{L,PEAK}$.

If USM light load operation is selected, make sure the inductance value is high enough to avoid reverse current limit threshold is been triggered just under steady state if the load current is zero.

For highest efficiency, select an inductor with a low DCR that meets the inductance, size and cost targets. Low loss ferrite materials is recommended to be selected.

Buck Inductor Design Example

Consider a typical design for a Buck converter providing 5.1V_{OUT} at 8A from 12V_{IN}, operating at 600kHz and using target inductor ripple current (ΔI_L) of 40% or 3.2A. Determine the approximate inductance value at first:

$$L = \frac{5.1V \times (12V - 5.1V)}{12V \times 600kHz \times 3.2A} = 1.53\mu H$$

Next, select the nearest standard inductance value, in this case 1.5 μ H, and calculate the resulting inductor ripple current (ΔI_L):

$$\Delta I_L = \frac{5.1V \times (12V - 5.1V)}{12V \times 600kHz \times 1.5\mu H} = 3.26A$$

$$I_{L,PEAK} = 8A + \frac{3.26A}{2} = 9.63A$$

The resulting 3.26A ripple current is 3.26A/8A is ~40.75%, well within the 20% ~ 50% target.

$$I_{L,PEAK,RVS} = \frac{3.26A}{2} = 1.63A < I_{LMT,RVS}$$

Finally, select an available inductor with a saturation current higher than the resulting $I_{L,PEAK}$ of 9.63A.

Buck Output Capacitor Selection

The Buck converter provides excellent performance with a wide variety of output capacitor types. Ceramic and POS types are most often selected due to their small size and low cost. Total capacitance is determined by the

transient response and output voltage ripple requirements of the system.

Buck Steady State Output Ripple

Steady state output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitors ESR (ESR ripple) as well as the stored charge (capacitive ripple). When considering total ripple, both should be considered.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Consider a typical application with $\Delta I_L = 3.26A$ using three 22 μ F ceramic capacitors, each with an ESR of ~6m Ω for parallel total of 66 μ F and 2m Ω ESR.

$$V_{RIPPLE,ESR} = 3.26A \times 2m\Omega = 6.52mV$$

$$V_{RIPPLE,CAP} = \frac{3.26A}{8 \times 66\mu F \times 600kHz} = 10.29mV$$

Total ripple = 16.81mV. The actual capacitive ripple may be higher than calculated value because the capacitance decreases with the voltage on the capacitor.

Using a 150 μ F 40m Ω POS cap, the above result is

$$V_{RIPPLE,ESR} = 3.26A \times 40m\Omega = 130.40mV$$

$$V_{RIPPLE,CAP} = \frac{3.26A}{8 \times 150\mu F \times 600kHz} = 4.53mV$$

Total ripple = 134.93mV.

Buck Output Transient Undershoot/Overshoot

If very fast load transient must be supported, consider the effect of the output capacitor on the output transient undershoot and overshoot. Instant-PWM responds quickly to changing load conditions, however, some considerations must be needed, especially when using small ceramic capacitors which have low capacitance at low output voltages which results in insufficient stored energy for load transient. Output transient undershoot and overshoot have two causes: voltage changes caused by the ESR of the output capacitor and voltage changes caused by the output capacitance and inductor current slew rate.

ESR undershoot or overshoot may be calculated as

$$V_{ESR} = \Delta I_{OUT} \times ESR$$

Using the ceramic capacitor example above and a fast load transient of +/- 4A, $V_{ESR} = +/- 4A \times 2m\Omega = +/- 8mV$. The POS capacitor result with the same load transient, $V_{ESR} = +/- 4A \times 40m\Omega = +/- 160mV$.

Capacitive undershoot (load increasing) is a function of the output capacitance, the load step, the inductor value and the input-output voltage difference and the maximum duty factor. During a fast load transient, the maximum duty factor of Buck converter is a function of t_{ON} and the $t_{OFF,MIN}$

as the control scheme is designed to rapidly ramp the inductor current by grouping together many t_{ON} pulses in this case. The maximum duty factor D_{MAX} may be calculated by

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF,MIN}}$$

Given this, the capacitive undershoot may be calculated by

$$V_{UNDERSHOOT,CAP} = -\frac{L \times \Delta I^2_{OUT}}{2 \times C_{OUT} \times (V_{IN,MIN} \times D_{MAX} - V_{OUT})}$$

Consider a 4A load increase using the ceramic capacitor case when $V_{IN} = 12V$. At $V_{OUT} = 5.1V$, the result is $t_{ON} = 708.33ns$, $t_{OFF,MIN} = 150ns$, $D_{MAX} = 708.33 / (708.33 + 150) = 0.825$ and

$$V_{UNDERSHOOT,CAP} = -\frac{1.5\mu H \times (4A)^2}{2 \times 66\mu F \times (12V \times 0.825 - 5.1V)} = -37.88mV$$

Using the POS capacitor case, the above result is

$$V_{UNDERSHOOT,CAP} = -\frac{1.5\mu H \times (4A)^2}{2 \times 150\mu F \times (12V \times 0.825 - 5.1V)} = -16.67mV$$

Capacitive overshoot (load decreasing) is a function of the output capacitance, the inductor value and the output voltage.

$$V_{OVERSHOOT,CAP} = \frac{L \times \Delta I^2_{OUT}}{2 \times C_{OUT} \times V_{OUT}}$$

Consider a 4A load decrease using the ceramic capacitor case above. At $V_{OUT} = 5.1V$ the result is

$$V_{OVERSHOOT,CAP} = \frac{1.5\mu H \times (4A)^2}{2 \times 66\mu F \times 5.1V} = 35.65mV$$

Using the POS capacitor case, the above result is

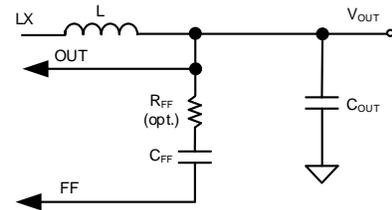
$$V_{OVERSHOOT,CAP} = \frac{1.5\mu H \times (4A)^2}{2 \times 150\mu F \times 5.1V} = 15.69mV$$

Combine the ESR and capacitive undershoot and overshoot to calculate the total overshoot and undershoot for a given application.

Load Transient Considerations

The SY83088C adopts the COT ripple-based control strategy to achieve good stability and fast transient response. In applications with high step load current, adding an RC network R_{FF} and C_{FF} between the OUT pin and the FF pin may further speed up the load transient response. $R_{FF} = 1k\Omega$ and $C_{FF} = 470pF$ have been shown to perform well in most applications. Increase C_{FF} will

speed up the load transient response if there is no stability issue.



Note that when $C_{OUT} > 500\mu F$ and minimum load current is low, set feed-forward values as $R_{FF} = 1k\Omega$ and $C_{FF} = 2.2nF$ to provide sufficient ripple to FB node for small output ripple and good transient behavior.

Thermal Design Considerations

Maximum power dissipation depends on the thermal resistance of the device package, the PCB layout, the surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation may be calculated by:

$$P_{D,MAX} = \frac{T_{J,MAX} - T_A}{\theta_{JA}}$$

Where, $T_{J,MAX}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

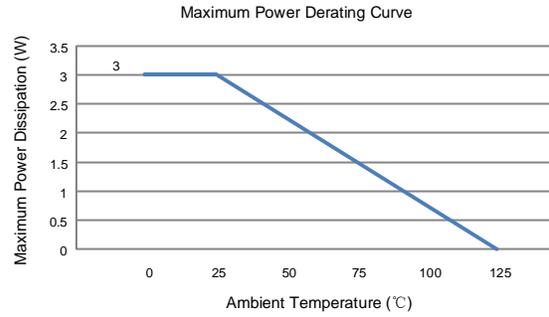
To comply with the recommended operating conditions, the maximum junction temperature is $125^\circ C$. The junction to ambient thermal resistance θ_{JA} is layout dependent. For the QFN2.5x2.5-16 package the thermal resistance θ_{JA} is $33^\circ C/W$ when measured on a standard Silergy 8.5cmx8.5cm size four-layer thermal test board. These standard thermal test layouts have a very large area with long 2-oz copper traces connected to each device pin and very large, unbroken 1-oz internal power and ground planes.

Meeting the performance of the standard thermal test board in a typical tiny evaluation board area requires wide copper traces well-connected to the device backside pads leading to exposed copper areas on the component side of the board as well as good thermal via from the exposed pad connecting to a wide middle-layer ground plane and, perhaps, to an exposed copper area on the board's solder side.

The maximum power dissipation at $T_A=25^\circ\text{C}$ may be calculated by the following formula:

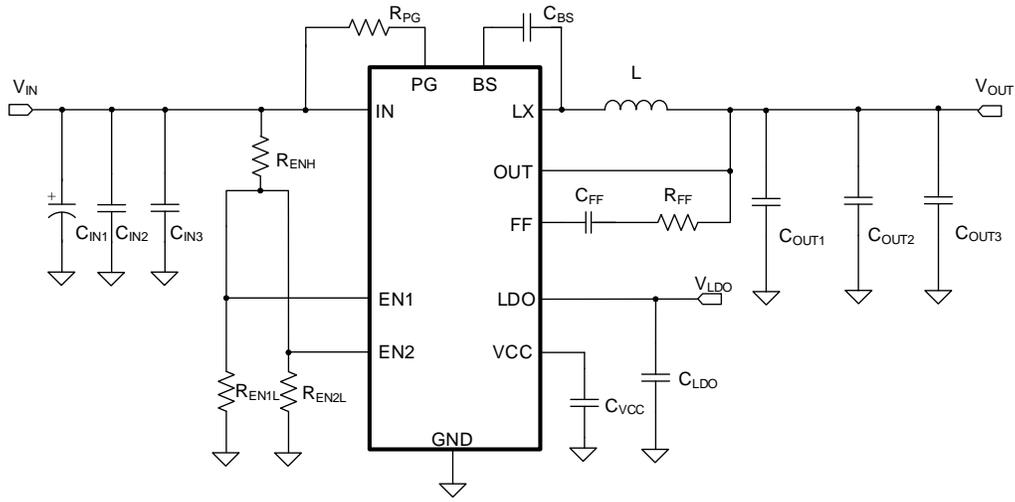
$$P_{D,MAX} = \frac{125^\circ\text{C} - 25^\circ\text{C}}{33^\circ\text{C}/\text{W}} = 3\text{W}$$

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J,MAX}$ and thermal resistance θ_{JA} . Use the derating curve in figure below to calculate the effect of rising ambient temperature on the maximum power dissipation.





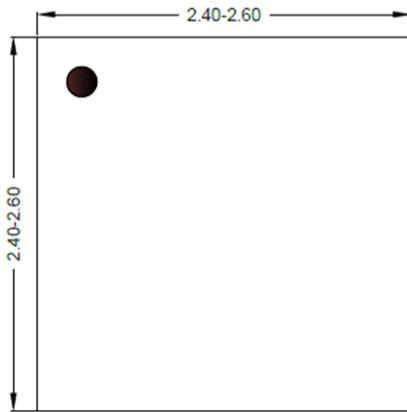
Application Schematic (V_{OUT}=5.1V)



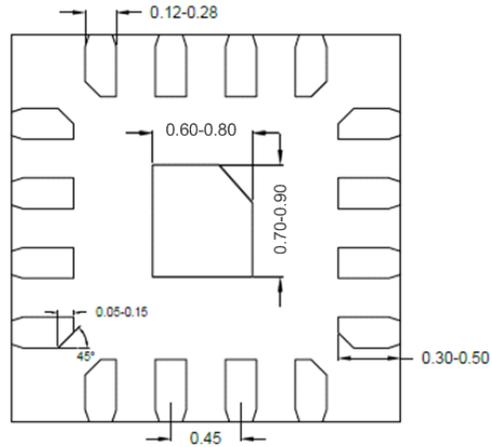
BOM List

Reference Designator	Description	Part Number	Manufacturer
C _{IN1}	47μF/50V, Electrolytic Capacitor		
C _{IN2}	10μF/50V/X5R, 1206	GRM31CR61H106KA12L	μpRata
C _{IN3} , C _{BS}	0.1μF/50V/X5R, 0603	GRM188R61H104KA93D	μpRata
C _{OUT1} , C _{OUT2} , C _{OUT3}	22μF/16V/X5R, 1206	GRM31CR61C226ME15L	μpRata
C _{LDO}	4.7μF/16V/X5R, 0603	GRM185R61C475KE11D	μpRata
C _{VCC}	2.2μF/16V/X5R, 0603	GRM188R61C225KE15D	μpRata
C _{FF}	470pF/50V/C0G, 0603	GRM1885C1H471JA01D	μpRata
L	1.5μH/16A, inductor	PCMB104T-1R5MS	CYNTEC
R _{ENH}	10kΩ, 1%, 0603		
R _{EN1L} , R _{EN2L}	1MΩ, 1%, 0603		
R _{PG}	100kΩ, 1%, 0603		
R _{FF}	1kΩ, 1%, 0603		

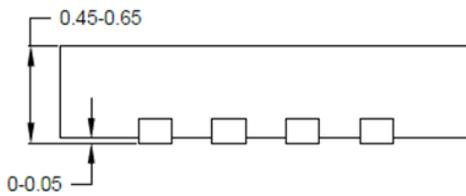
QFN2.5x2.5-16 Package Outline Drawing



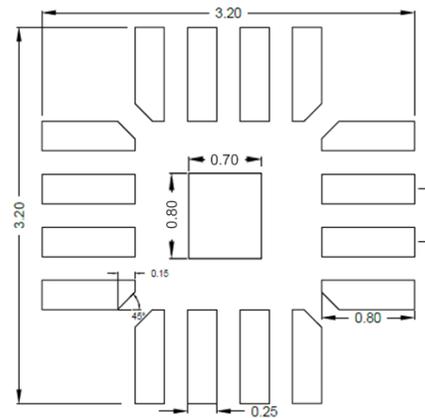
Top view



Bottom view



Side view

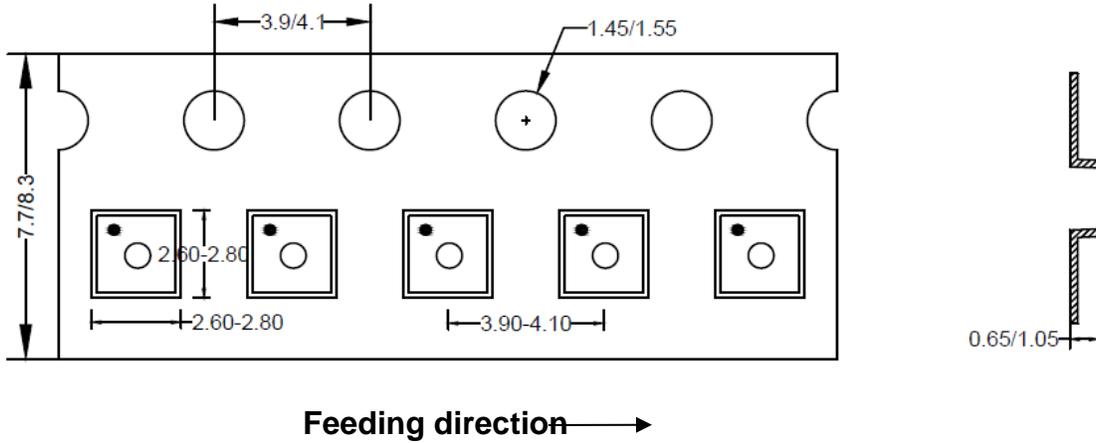


**Recommended PCB layout
(Reference only)**

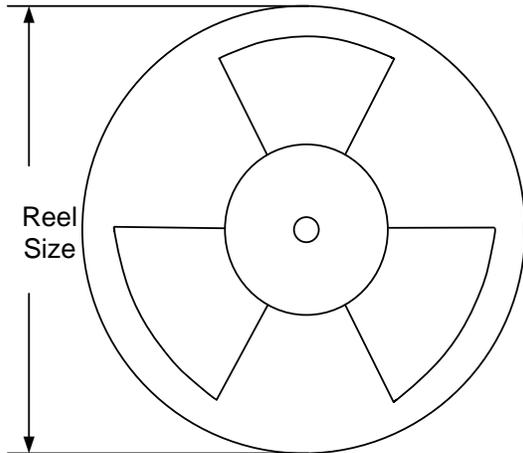
Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

1. QFN2.5x2.5 taping orientation



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN2.5x2.5	8	4	7"	400	160	3000

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change	Pages changed
Oct.26, 2023	1.0	Initial Release	-
Dec.18, 2023	1.0A	Replace the start up waveform and efficiency diagram.	Page 1,6,7,8
		Add some Electrical Characteristics values. ($I_Q/I_{SHDN1}/I_{SHDN2}$ max, $V_{PG,R}$ min and max)	Page 4
		Adjust V_{BYP} max from 4.9V to 4.95V.	Page 5

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