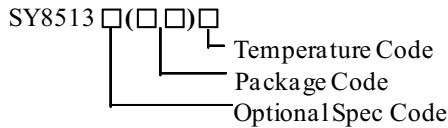


General Description

The SY8513 develops a high efficiency, current mode adaptive constant off time controlled, asynchronous step-down DC/DC converter capable of delivering 3A output current. The SY8513 operates over a wide input voltage range from 4.5V to 100V and integrates main switch with very low $R_{DS(ON)}$ to minimize the conduction loss. The switching frequency is adjustable from 100kHz to 500kHz using an external resistor. And the device features cycle-by-cycle peak current limitation.

Ordering Information



Ordering Number	Package type	Note
SY8513FCC	SO8E	--

Features

- Low $R_{DS(ON)}$ for Internal N-channel Power FET(TOP):150m Ω
- 4.5-100V Input Voltage Range
- 3A Output Current Capability
- Adjustable Switching Frequency Range: 100kHz to 500kHz
- Internal Soft-start Limits the Inrush Current
- Hic-cup Mode Output Short Circuit Protection
- EN ON/OFF Control with Accurate Threshold
- Cycle-by-cycle Peak Current Limit
- 0.8V \pm 1 % Reference Voltage Accuracy
- Compact Package: SO8E

Applications

- Non-isolated Telecommunication Buck Regulator
- Secondary High Voltage Post Regulator
- Automotive Systems
- Electric Bicycle

Typical Applications

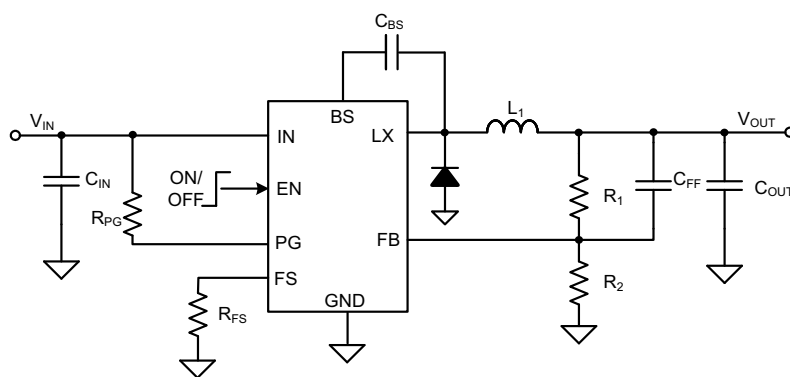


Figure1. Schematic Diagram

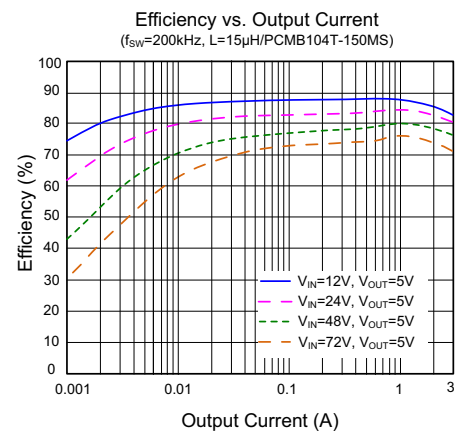
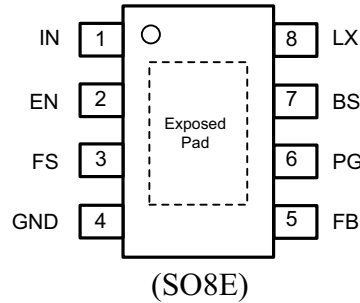


Figure2. Efficiency vs. Output Current

Pinout (top view)



Top Mark: DAGxyz (Device code: DAG; x=year code, y=week code, z=lot number code)

Pin Name	Pin Number	Pin Description
IN	1	Input pin. Decouple this pin to the GND pin with at least a 1 μ F ceramic capacitor.
EN	2	Enable control. Pulled high to turn on. Do not leave it floating.
FS	3	Frequency programming pin. Connect a resistor to ground to program a switching frequency between 100kHz to 500kHz. The switching frequency equals to: $f_{sw}(kHz)=10^5/R_{FS}(k\Omega)$
GND	4	Ground pin
FB	5	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.8 \times (1+R_1/R_2)$.
PG	6	Power good Indicator. Open-drain output when the output voltage is within 90% to 120% of the regulation point.
BS	7	Boot-strap pin. Supply high side gate driver. Connect a 0.1 μ F ceramic capacitor between the BS pin and the LX pin.
LX	8	Inductor pin. Connect this pin to the switching node of the inductor.
Exposed Pad	/	Exposed pad must be connected to the GND pin. Connect to system ground plane on application board for optimal thermal performance.

Block Diagram

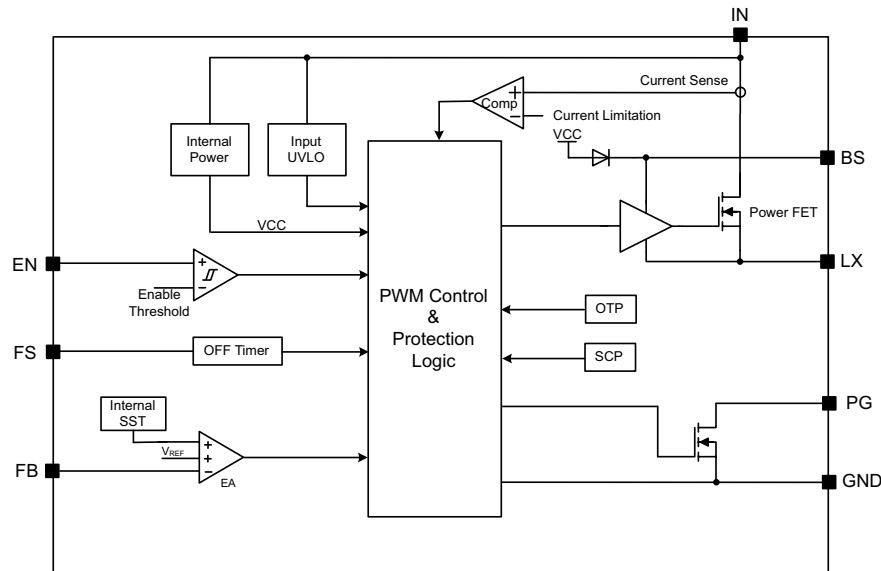


Figure3. Block Diagram



Absolute Maximum Ratings (Note 1)

Supply Input Voltage	-0.3V to 100V
BS-LX Voltage	-0.3V to 6V
EN, FS, FB, PG, LX Voltage	-0.3V to $V_{IN} + 0.3V$
Power Dissipation, P_D @ $T_A = 25^\circ C$, SO8E	-2.38W
Package Thermal Resistance (Note 2)	
θ_{JA}	42°C/W
θ_{JC}	4°C/W
Junction Temperature Range	-40°C to 150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	-65°C to 150°C
Dynamic LX Voltage in 10 ns Duration	$V_{IN} + 3V$ to GND-5V

Recommended Operating Conditions (Note 3)

Supply Input Voltage	4.5V to 100V
Junction Temperature Range	-40°C to 125°C
Ambient Temperature Range	-40°C to 85°C

Electrical Characteristics

($V_{IN}=48V$, $V_{OUT}=5V$, $L=10\mu H$, $C_{OUT}=22\mu F$, $T_A=25^\circ C$, $I_{OUT}=1A$ unless otherwise specified)

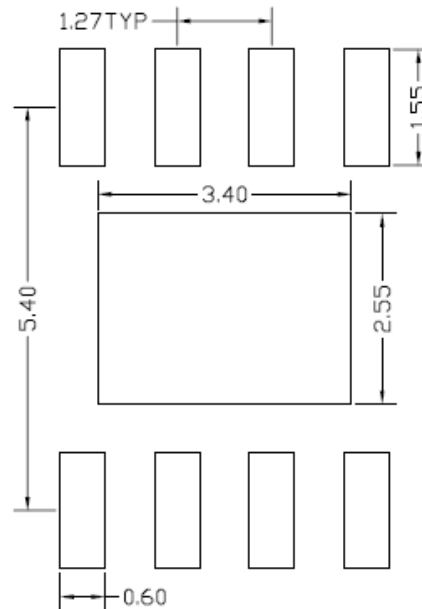
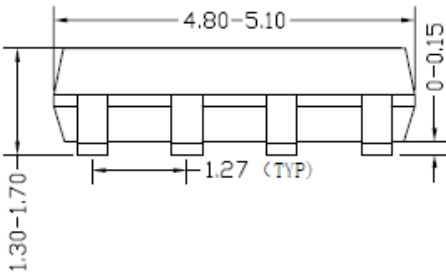
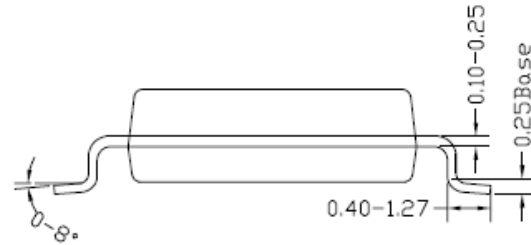
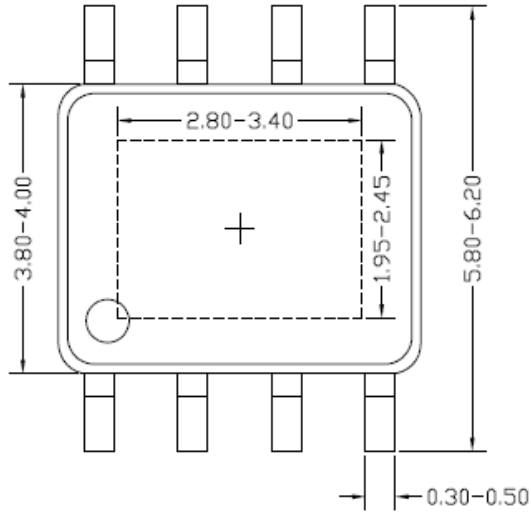
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.5		100	V
Input UVLO Threshold	V_{UVLO}		3.9	4.2	4.5	V
Input UVLO Hysteresis	V_{HYS}			0.3		V
Quiescent Current	I_Q	$V_{FB}=V_{REF}\times 105\%$		100	130	μA
Shutdown Current	I_{SHDN}	$V_{EN}=0V$	2	8	16	μA
Feedback Reference Voltage	V_{REF}		792	800	808	mV
FB Input Current	I_{FB}	$V_{FB}=3.3V$	-50		50	nA
Top FET R_{ON}	$R_{DS(ON)}$			150		m Ω
EN Rising Threshold	$V_{EN,R}$		1	1.1	1.2	V
EN Falling Threshold	$V_{EN,F}$		0.8	0.9	1	V
EN Leakage Current	I_{EN}		-1		1	μA
Min ON Time	$t_{ON,MIN}$			180		ns
Min OFF Time	$t_{OFF,MIN}$			280		ns
Soft-start Time	t_{SS}			2		ms
Switching Frequency Program Range	$f_{SW,RNG}$	$R_{FS}=200k\sim 1M$	100		500	kHz
Switching Frequency Setting Accuracy	f_{SW}	$R_{FS}=200k$	400	500	600	kHz
Power Good Threshold	V_{PG}	V_{FB} falling, PG from high to low		90		$\%V_{REF}$
		V_{FB} rising, PG from low to high		92		$\%V_{REF}$
		V_{FB} rising, PG from high to low		120		$\%V_{REF}$
		V_{FB} falling, PG from low to high		115		$\%V_{REF}$
Power Good Delay	$t_{PG,F}$	High to low		20		μs
	$t_{PG,R}$	Low to high		200		μs
Power Good Output Low	$V_{PG,L}$	$I_{PG}=2mA$			0.3	V
PG High Leakage Current					1	μA
Top FET Current Limit	$I_{LMT,RNG}$		3.8			A
Output Under Voltage Protection Threshold	V_{UVP}		45	50	55	$\%V_{REF}$
Output UVP Delay	$t_{UVP,DLY}$			10		μs
UVP Hiccup ON Time	$t_{UVP,ON}$			2		ms
UVP Hiccup OFF Time	$t_{UVP,OFF}$			16		ms
Thermal Shutdown Temperature	T_{SD}			150		$^\circ C$
Thermal Shutdown Hysteresis	T_{HYS}			15		$^\circ C$

Note 1: Stresses beyond “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at $T_A=25^\circ C$ on a two-layer Silergy demo board.

Note 3: The device is not guaranteed to function outside its operating conditions.

SO8E Package Outline & PCB Layout



Front view

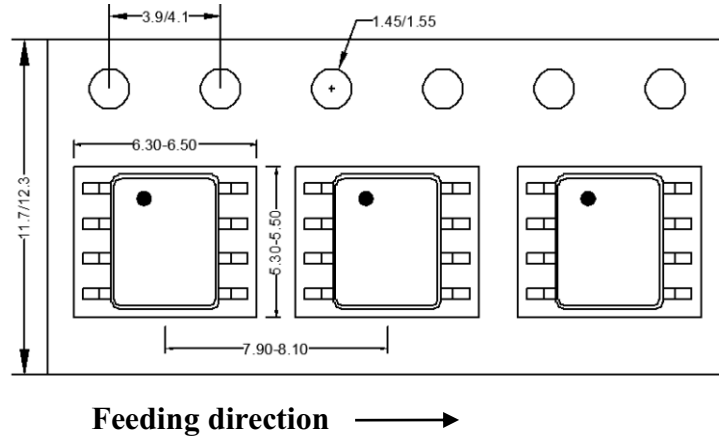
**Recommended PCB Layout
(Reference Only)**

Notes: All dimension in millimeter and exclude mold flash & metal burr.

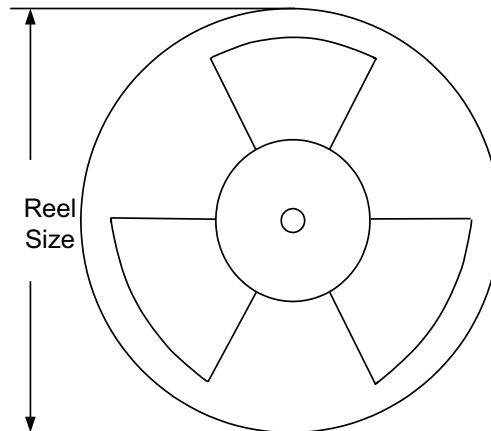
Taping & Reel Specification

1. Taping orientation

SO8E



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
SO8E	12	8	13"	400	400	2500

Others: NA