Applications Note: AN_SY8805A
High Efficiency 1 MHz, 5A Synchronous Step Down Regulator

General Description

The SY8805A is a high-efficiency 1 MHz synchronous step-down DC-DC regulator, Current Mode Control IC capable of delivering up to 5A output current. The SY8805A operates over a wide input voltage range from 3V to 5.5V. It integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss. High intergrated solution and DFN2x2-8 package perform the optimized BOM cost and reduce external component part count. Low input and output voltage ripple, small external inductor and capacitor sizes, small PCB layout space are achived with 1MHz switching frequency.

Ordering Information

SY8805□(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Temperature Range: -40°C to 85°C

Ordering Number	Package type	Note
SY8805ADFC	DFN2x2-8	--

Features

- Low $R_{DS(ON)}$ for internal switches (top/bottom): 35/15 mohm
- 3-5.5V input voltage range
- 1 MHz switching frequency minimizes the external components
- Internal softstart limits the inrush current
- Up to 98% efficiency
- 0.6V reference voltage
- Shutdown mode draws<0.1uA supply current
- 100% dropout operation
- Power good indicator
- OVP/OCP/UVLO/OTP protections
- RoHS Compliant and Halogen Free
- Compact package: DFN2x2-8

Applications

- High definition Set Top Box
- LCD TV
- Access Point Router
- Mini-notebook PC
- Net PC

Typical Applications

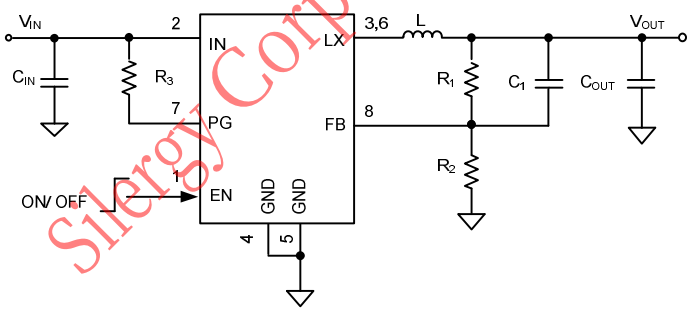


Figure 1. Schematic

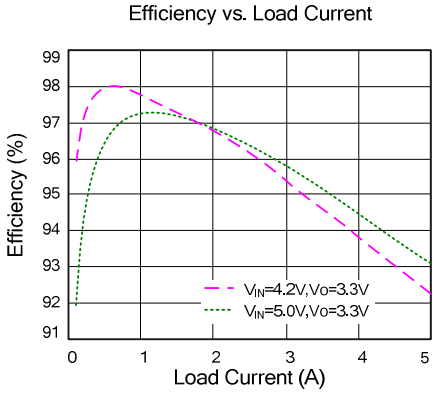
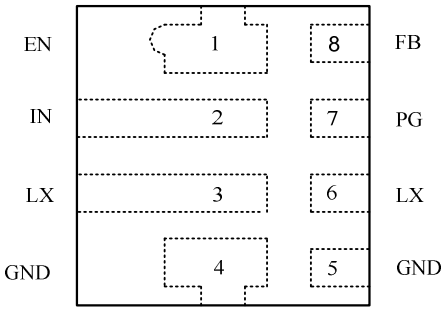


Figure 2. Efficiency vs Load Current

Pinout (top view)



DFN2x2-8

Top Mark: **EJ*xyz* for SY8805ADFC(**device code: EJ, ***x=year code, y=week code, z= lot number code*****)**

Pin Name	DFN2x2-8	Pin Description
EN	1	Enable control. Pull high to turn on. Do not float.
GND	4,5	Ground pins.
LX	3,6	Inductor pin. Connect this pin to the switching node of inductor
IN	2	Power Input Pin.
FB	8	Output Feedback Pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: Vout=0.6*(1+R1/R2)
PG	7	Power good indicator. When the output voltage exceeds 90% of regulation point, it becomes open drain; low otherwise.

Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- 6V
Enable, FB Voltage---------- V_{IN} + 0.6V
Power Dissipation, PD @ TA = 25°C,DFN2x2-8 ---------- 2W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 62.5°C/W
θ_{JC} ---------- 10°C/W
Junction Temperature Range ---------- 125°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- 65°C to 150°C

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 3V to 5.5V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 5V, V_{OUT} = 2.5V, L = 0.47uH, C_{OUT} = 47uFx2, T_A = 25°C, I_{MAX} = 1A unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		3.0		5.5	V
Shutdown Current	I_{SHDN}	EN=0		0.1	1	μA
Quiescent Current	I_Q	I_{OUT}=0, V_{FB}=V_{REF} · 105%		100		μA
Feedback Reference Voltage	V_{REF}	0.6V, ± 1.5%	0.591	0.6	0.609	V
FB Input Current	I_{FB}	V_{FB}=V_{IN}	-50		50	nA
PFET RON	$R_{DS(ON),P}$			35		mΩ
NFET RON	$R_{DS(ON),N}$			15		mΩ
PFET Current Limit	I_{LIM}		6			A
EN rising threshold	V_{ENH}		1.5			V
EN falling threshold	V_{ENL}				0.4	V
Input UVLO threshold	V_{UVLO}				2.8	V
UVLO hysteresis	V_{HYS}			0.4		V
Oscillator Frequency	F_{OSC}	I_{OUT}=100mA		1		MHz
Min ON Time				80		ns
Max Duty Cycle			100			%
Thermal Shutdown Temperature	T_{SD}			150		°C
Internal Soft Start Time	T_{SS}			1.5		ms
Phase Node Discharge Resistance	R_{DISCHG}			10		Ω

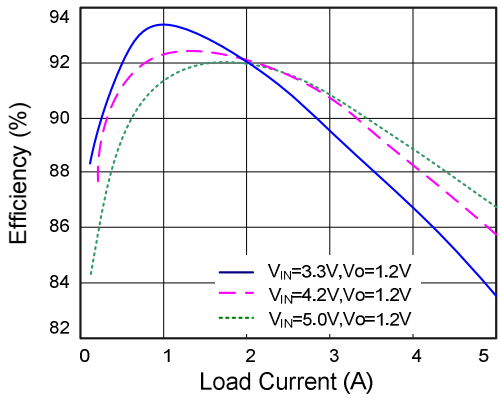
Note 1: Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2: θJA is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz and four-layer copper with recommended pad.

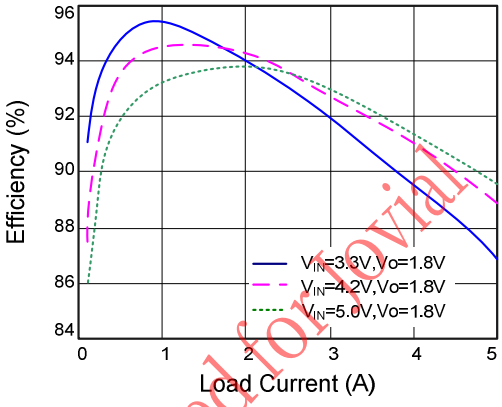
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

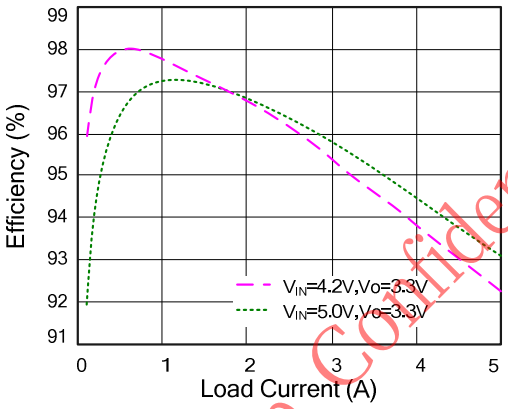
Efficiency vs. Load Current



Efficiency vs. Load Current

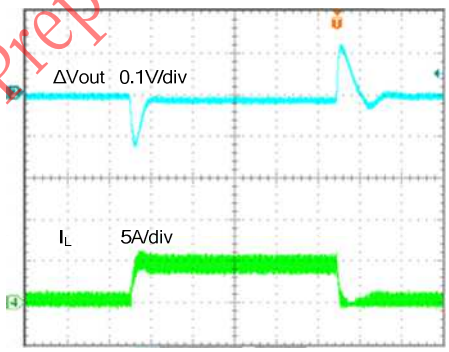


Efficiency vs. Load Current



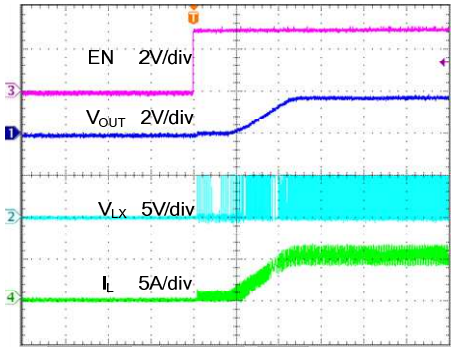
Load Transient

V_{IN}=5.0V, V_{OUT}=1.8V, Io=0.5~5A



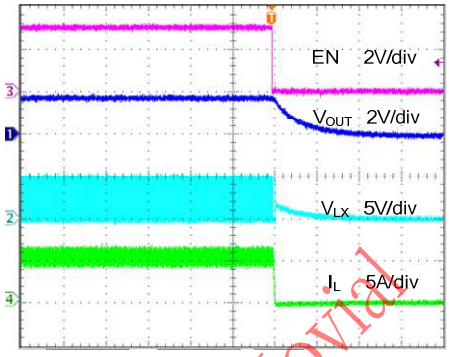
Time (40us/div)

Startup from Enable
V_{IN}=5.0V, V_{OUT}=1.8V, Io=5A



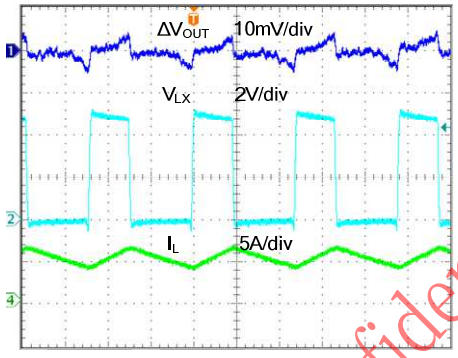
Time (1ms/div)

Shutdown from Enable
V_{IN}=5.0V, V_{OUT}=1.8V, Io=5A



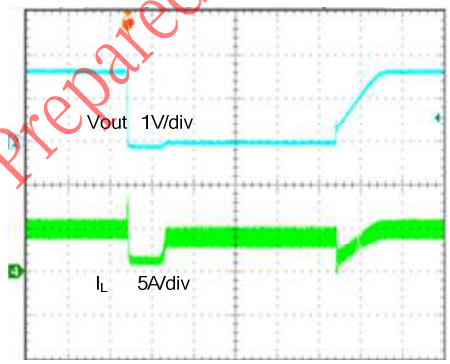
Time (40us/div)

Output Ripple
V_{IN}=5.0V, V_{OUT}=1.8V, Io=5A



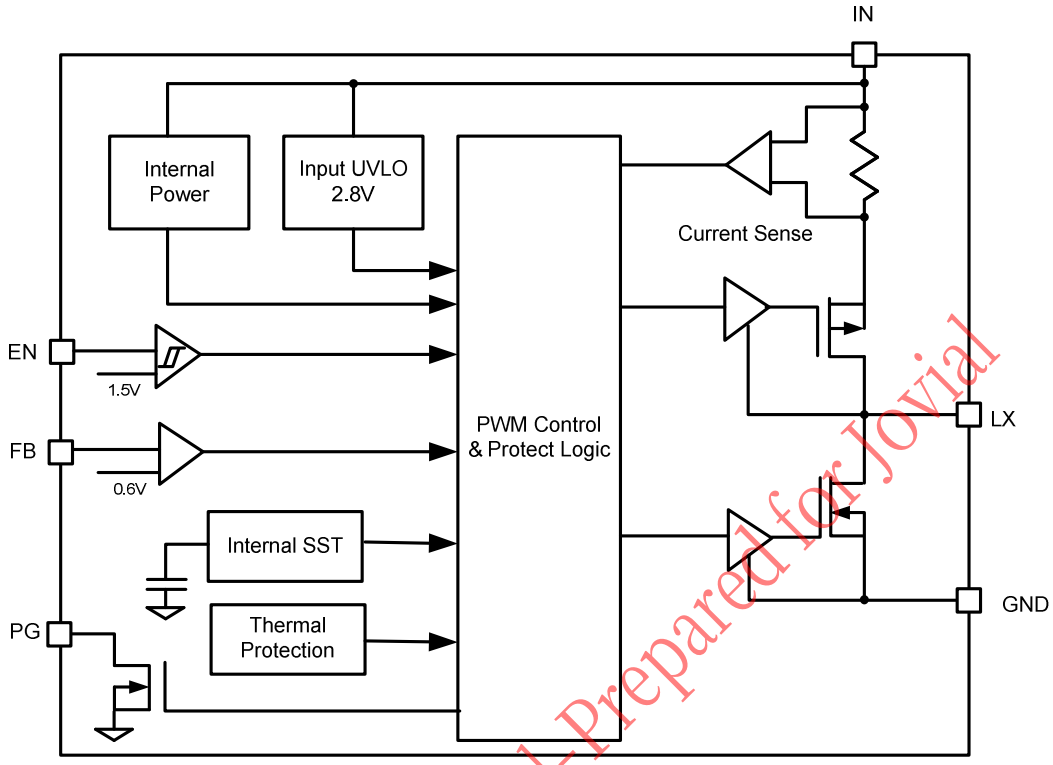
Time (400ns/div)

Short Circuit Protection
V_{IN}=5.0V, V_{OUT}=1.8V,Io=5A to Short



Time (1ms/div)

Block Diagram



Operation

SY8805A is a synchronous buck regulator IC that integrates the PWM control, top and bottom switches on the same die to minimize the switching transition loss and conduction loss. With ultra low Rds(on) power switches and proprietary PWM control, this regulator IC can achieve the highest efficiency and the highest switch frequency simultaneously to minimize the external inductor and capacitor size, and thus achieving the minimum solution footprint.

SY8805A will sense the output voltage conditions for the fault protection. If the DC output voltage is about 3% over the regulation level, both switches will turn off and remain in this OFF state. If the DC output voltage is below 33% of the regulation level, the internal softstart node is discharged and the error amplifier output is reset to minimum. When the output voltage is below 33% of the regulation, the frequency is folded back to about 20% of the normal frequency and the current limit is folded back to 5.0A to prevent the inductor current runaway and to reduce the power dissipation within the IC under true short circuit conditions.

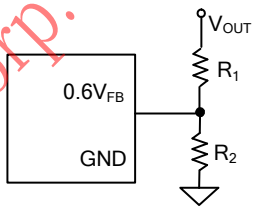
Applications Information

Because of the high integration in the SY8805A IC, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, output inductor L and feedback resistors (R_1 and R_2) need to be selected for the targeted applications specifications.

Feedback resistor dividers R_1 and R_2:

Choose R1 and R2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R1 and R2. A value of between 10k and 1M is highly recommended for both resistors. If Vout is 1.8V, R1=100k is chosen, then R2 can be calculated to be 50k.:

$$R_2 = \frac{0.6V}{V_{OUT} - 0.6V} R_1$$



Input capacitor CIN:

This ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \bullet \sqrt{D(1-D)}$$

This formula has a maximum at $V_{IN}=2V_{OUT}$ condition, where $I_{CIN\_RMS}=I_{OUT}/2$. This simple worst-case condition is commonly used for DC/DC design.

With the maximum load current at 5A, a typical X5R or better grade ceramic capacitor with 6.3V rating and more than two pcs 22uF capacitance can handle this ripple current well. To minimize the potential noise problem, place this ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins.

Output capacitor COUT:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor with 6.3V rating and greater than two pcs 47uF capacitance.

Output inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

where F_{sw} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.
The SY8805A regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,\,MIN} > I_{OUT,\,MAX} + \frac{V_{OUT}(1\text{-}V_{OUT}/V_{IN,MAX})}{2 \cdot F_{SW} \cdot L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<15mohm to achieve a good overall efficiency.

Enable Operation

Pulling the EN pin low (<0.4V) will shut down the device. During shut down mode, the SY8805A shutdown current drops to lower than 0.1uA. Driving the EN pin high (>1.5V) will turn on the IC again.

PG (Power Good):

The power good is an open-drain output. Connect an above 100k pull up resistor to VIN to obtain an output voltage. The power good will output high immediately after the output voltage within 90% of normal output voltage.

Load Transient Considerations:

The SY8805A regulator IC integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a 22pF~220pF ceramic capacitor in parallel with R_2 may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements.

Layout Design:

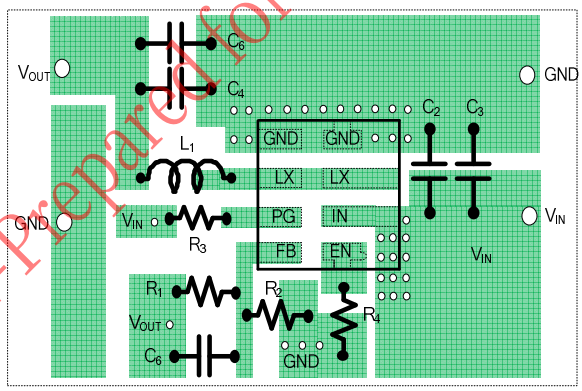
The layout design of SY8805A regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{IN}, L, R_1 and R_2.

(1) Multi-layer board is suggested for SY8805A 5A output current application. It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. Reasonable vias are suggested to be placed around GND pins to enhance the soldering qualityand thermal performance.

(2) CIN must be close to Pins IN and GND. The loop area formed by CIN and GND must be minimized. It is desirable to maximize the PCB copper area connecting to VIN pin to achieve the best thermal performance. Reasonable vias are suggested to be placed around VIN pin to enhance the thermal performance.

(3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

(4) The components R1 and R2, and the trace connecting to the FB pin must not be adjacent to the LX net on the PCB layout to avoid the noise problem.



Design Specifications

Input Voltage (V)	Output Current (A)	Output Voltage (V)	Test conditions
3-5.5	0~5	1.8	K_1, close

Schematic

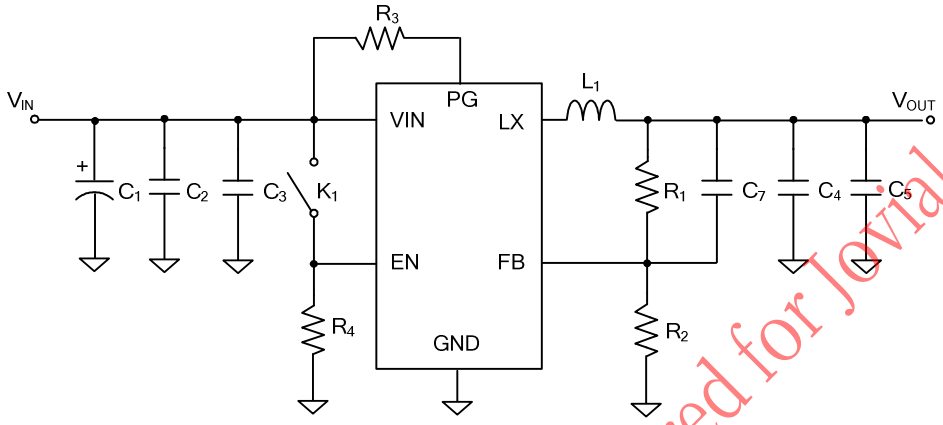


Figure1. Schematic Diagram

Quick Start Guide (Refer to Figure 4)

1. Connect the output load to VOUT and GND output connectors. Preset the load current between 0A and 5.0A.
2. Preset the input supply to a voltage between 3V and 5.5V. Turn the supply off. Connect the input supply to VIN and GND input connectors.
3. Short Jumper K1. Turn on the input supply and measure the output voltage.

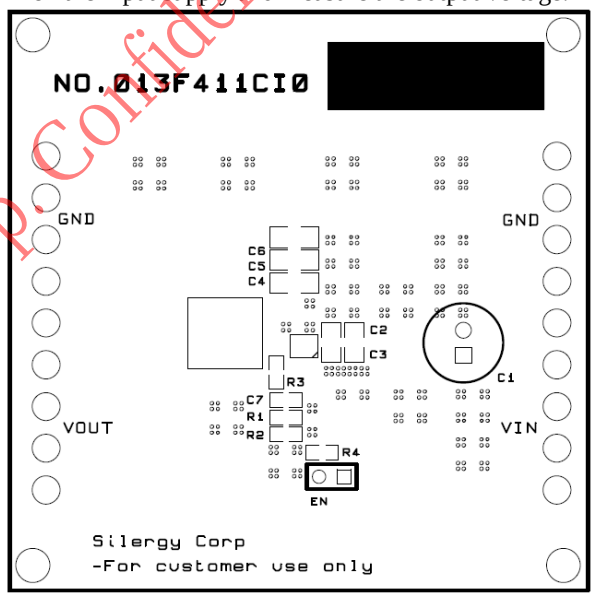
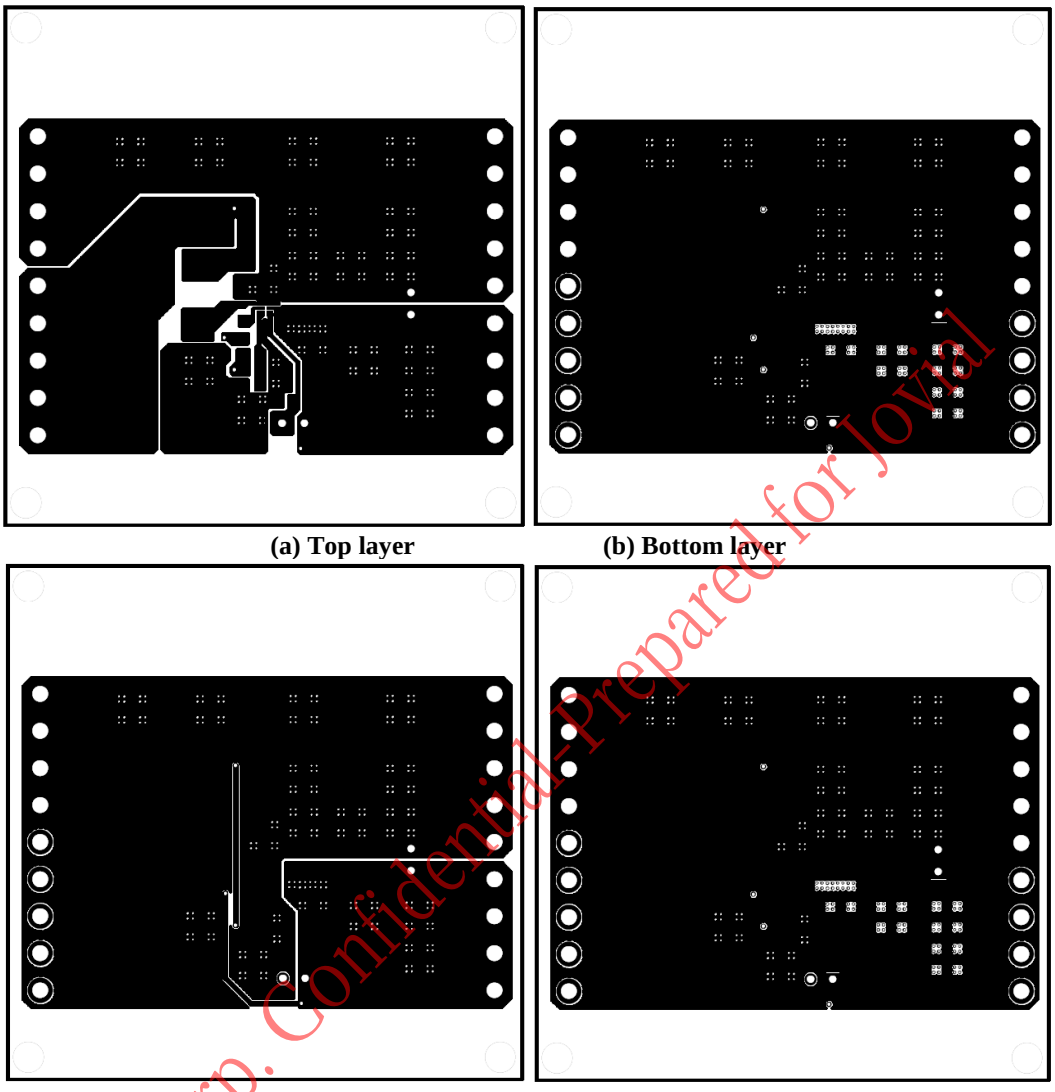


Figure 4. Top Silkscreen

PCB Layout



(a) Top layer (b) Bottom layer

(c)Middle layer 1 (d) Middle layer 2

Figure5. PCB Layout Plots

BOM List

Reference Designator	Description	Part Number	Manufacturer
U_1	5A, 1MHz Sync Buck(DFN2*2-8)	SY8805ADFC_1	
C_1	470uF/16V (electrolytic capacitor)		
C_2 , C_3	22uF/10V,1206,X5R	C3216X5R1A226M	TDK
C_4, C_5	47uF/6.3V,1206, X5R	C3216X5R0J4765M	TDK
C_7	22pF/50V/C0G,0603	C1608C0G1H220J	TDK
L_1	0.47uH/20.5A inductor	SPM6530T-R47M	TDK
R_1	100k, 1%,0603		
R_2	49.9k,1%,0603		
R_3	100k, 0603		
R_4	1M, 0603		

Output voltage ripple test

A proper output ripple measurement should be done according to Figure 6 setup. Output voltage ripple should be measured across the output ceramic cap near the IC.

1. Remove the ground clip and head of the probe. Wind thin wires around the ground ring of the probe. Solder the end of the ground ring wire to the negative node of the COUT. Touch the probe tip to the positive node of the COUT. Refer to Figure.6.
2. Minimize the loop formed by COUT terminals, probe tip and ground ring.
3. Change the probing direction to decouple the electromagnetic noise generated from the nearby buck inductor (Refer to Figure.6).

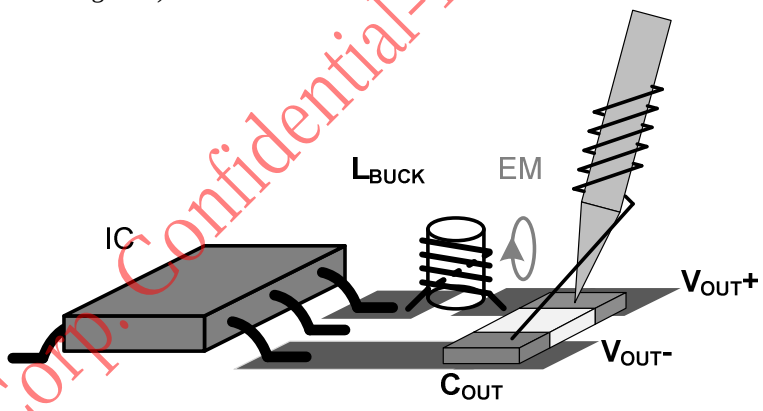
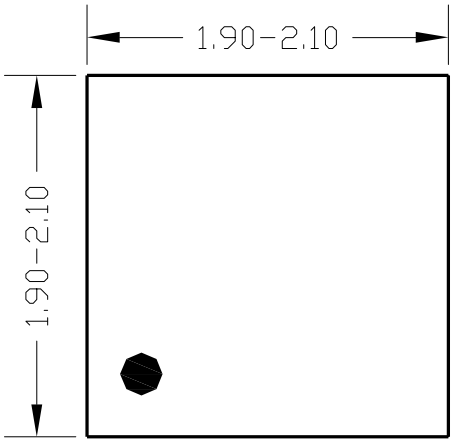
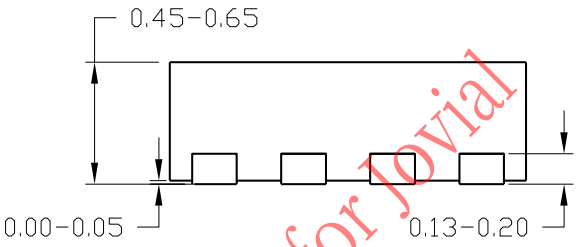


Figure.6 Recommended way to measure the output voltage ripple

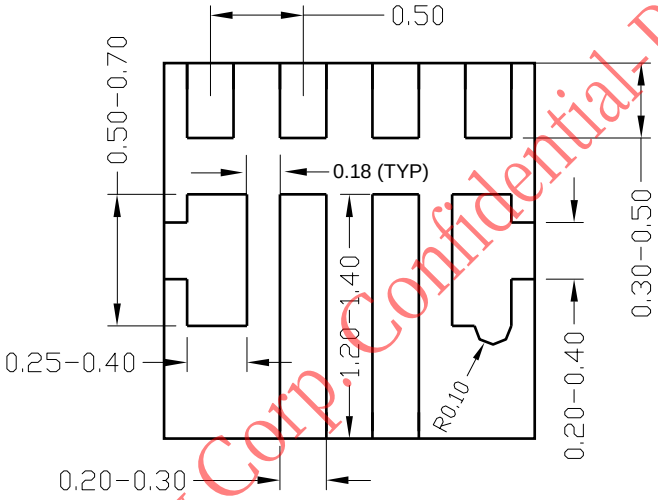
DFN2x2-8 (FC) Package Outline



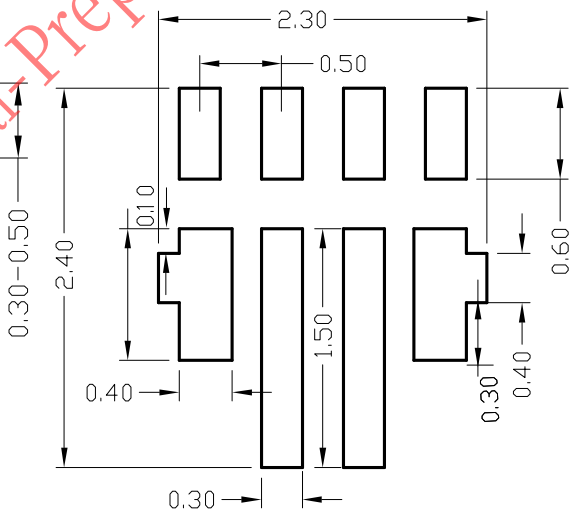
Top View



Side View



Bottom View

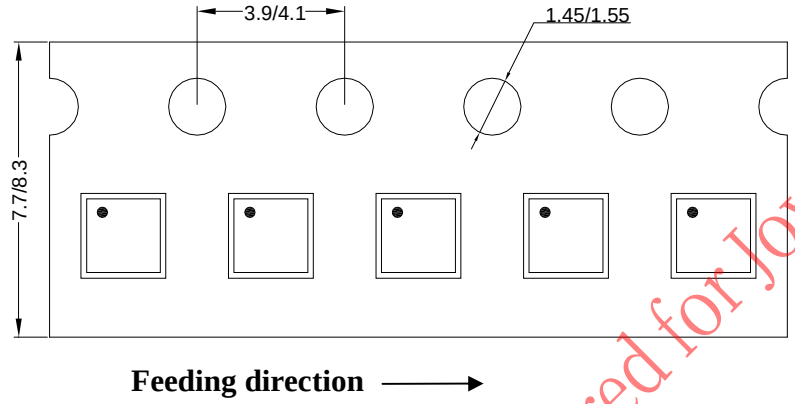


Recommended PCB

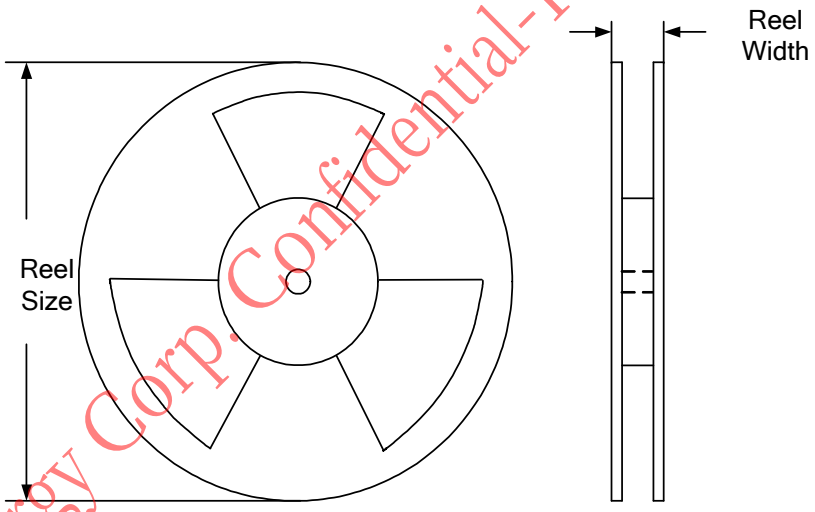
Notes: **All dimension in MM**
All dimension do not include mold flash & metal burr

Taping & Reel Specification

1. DFN2x2



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Reel width(mm)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN2x2	8	4	7"	8.4	400	160	3000

3. Others: NA