MICREL®

SY88289BL

3.3V, 3.2Gbps CML Limiting Post Amplifier with High-Gain TTL Loss-of-Signal

General Description

The SY88289BL low-power limiting, post amplifier is designed for use in fiber-optic receivers. The device connects to typical transimpedance amplifiers (TIAs). The linear signal output from TIAs can contain significant amounts of noise and may vary in amplitude over time. The SY88289BL quantizes these signals and outputs CML level waveforms.

The SY88289BL operates from a single +3.3V power supply, over temperatures ranging from –40°C to +85°C. With its wide bandwidth, high gain, and signals with data rates up to 3.2Gbps and as small as $5mV_{PP}$ can be amplified to drive devices with CML inputs or AC-coupled CML/PECL inputs.

The SY88289BL generates a high-gain loss-of-signal (LOS) open-collector TTL output. This function has a high-gain input stage for increased LOS sensitivity. A programmable loss-of-signal level set pin (LOS_{LVL}) sets the sensitivity of the input amplitude detection. LOS asserts high if the input amplitude falls below the threshold set by LOS_{LVL} and de-asserts low otherwise. The enable bar input (/EN) de-asserts the true output signal without removing the input signal. The LOS output can be fed back to the /EN input to maintain output stability under a loss-of-signal condition. Typically 3.5dB LOS hysteresis is provided to prevent chattering.

All support documentation cab be found on Micrel's web site at: www.micrel.com.

Features

- Single 3.3V power supply
- DC to 3.2Gbps operation
- Low-noise CML data outputs
- High-gain LOS
- Chatter-free open-collector TTL signal detect (LOS) output with internal 4.75kΩ pull-up resistor
- TTL /EN input
- Programmable LOS level set (LOS_{LVL})
- Ideal for mutil-rate applications
- Available in a tiny 16-pin MLF® package

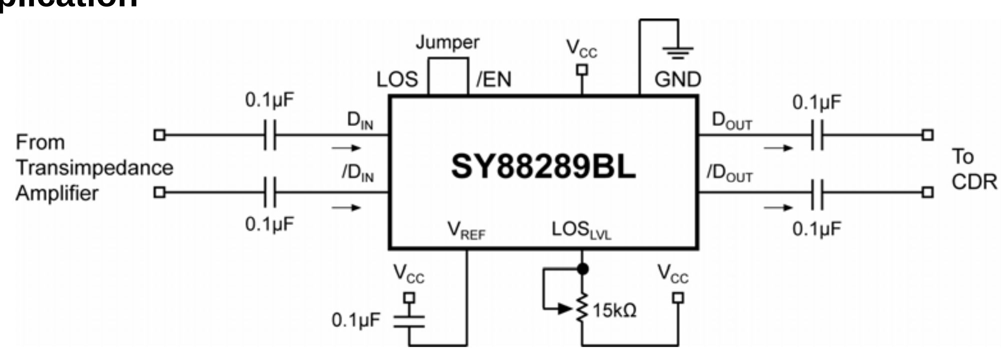
Applications

- APON, BPON, EPON, and gpon
- Gigabit Ethernet
- Fibre Channel
- OC-3 and OC-12/24 SONET/SDH
- High-gain line driver and line receiver

Markets

- FTTP
- Optical transceivers
- Datacom/telecom
- Low-gain TIA interface
- Long reach FOM

Typical Application



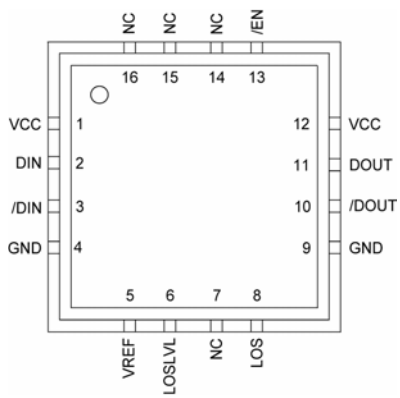
Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY88289BLMG	MLF-16	Industrial	289B with Pb-Free bar line indicator	NiPdAu Pb-Free
SY88289BLMGTR(1)	MLF-16	Industrial	289B with Pb-Free bar line indicator	NiPdAu Pb-Free

Note:

1. Tape and Reel.

Pin Configuration



16-Pin MLF® (MLF-16)

Pin Description

Pin Number	Pin Name	Type	Pin Function
1, 12	VCC	Power Supply	Positive power supply.
2	DIN	Data Input	True data input.
3	/DIN	Data Input	Complementary data input.
4, 9	GND	Ground	Device ground.
5	VREF		Reference voltage: Placing a capacitor here to VCC helps stabilize LOS_{LVL}.
6	LOSLVL	Input	Loss-of-signal Level Set: a resistor from this pin to V_{CC} sets the threshold for the data input amplitude at which LOS will be asserted.
7, 14, 15, 16	N/C		No connect.
8	LOS	Open-collector TTL output w/internal 4.75kΩ pull-up resistor	Loss-of-signal: asserts high when the data input amplitude falls below the threshold set by LOS_{LVL}.
10	/DOUT	CML Output	Complementary data output.
11	DOUT	CML Output	True data output.
13	/EN	TTL Input: Default is HIGH.	/Enable: This input enables the outputs when it is LOW. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) .... 0V to +7.0V
Input Voltage (DIN, /DIN) .... 0 to V_{CC}
Output Current (I_{OUT})
Continuous .... ±50mA
Surge .... ±100mA
/EN Voltage .... 0 to V_{CC}
V_{REF} Current ....-800µA to +500µA
LOS_{LVL} Voltage .... V_{REF} to V_{CC}
Lead Temperature (soldering, 20sec.) .... 260°C
Storage Temperature (T_s) ....-65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) ....+3.0V to +3.6V
Ambient Temperature (T_A) ....–40°C to +85°C
Junction Temperature (T_J) ....–40°C to +120°C
Junction Thermal Resistance
MLF® (θ_{JA})
Still-air .... 61°C/W
MLF® (Ψ_{JB})
Junction-to-board ....38°C/W

DC Electrical Characteristics

V_{CC} = 3.0V to 3.6V; R_L = 50Ω to V_{CC}; T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{CC}	Power Supply Current	No output load		45	62	mA
LOS_{LVL}	LOS_{LVL} Voltage		V_{REF}		V_{CC}	V
V_{OH}	CML Output HIGH Voltage		V_{CC}-0.020	V_{CC}-0.005	V_{CC}	V
V_{OL}	CML Output LOW Voltage	V_{CC} = 3.3V	V_{CC}-0.475	V_{CC}-0.400	V_{CC}-0.350	V
V_{OFFSET}	Differential Output Offset				±80	mV
Z_O	Single-Ended Output Impedance		40	50	60	Ω
Z_I	Single-Ended Input Impedance		40	50	60	Ω
V_{REF}	Reference Voltage			V_{CC}-1.28		V

TTL DC Electrical Characteristics

V_{CC} = 3.0V to 3.6V; R_L = 50Ω to V_{CC}; T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	/EN Input HIGH Voltage		2.0			
V_{IL}	/EN Input LOW Voltage				0.8	V
I_{IH}	/EN Input HIGH Current	V_{IN} = 2.7V V_{IN} = V_{CC}			20 100	µA µA
I_{IL}	/EN Input HIGH Current	V_{IN} = 0.5V	-0.3			mA
V_{OH}	LOS Output HIGH Level	V_{CC} ≥ 3.3V, I_{OH-MAX} < 160uA V_{CC} < 3.3V, I_{OH-MAX} < 160uA	2.4 2.0			V V
V_{OL}	LOS Output LOW Level	I_{OL} = +2mA			0.5	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential (GND) on the PCB. Ψ_{JB} uses 4-layer (θ_{JA}) in still-air-number, unless otherwise stated.

AC Electrical Characteristics

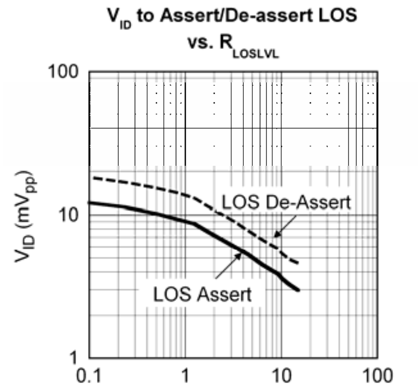
V_{CC} = 3.0V to 3.6V; R_L = 50Ω to V_{CC}; T_A = –40°C to +85°C.

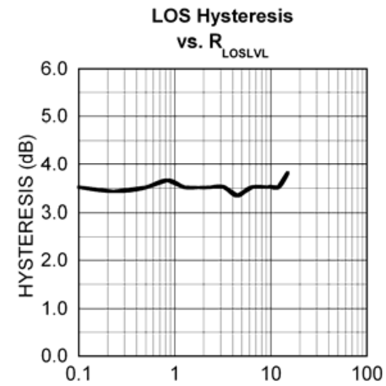
Symbol	Parameter	Condition	Min	Typ	Max	Units
t_r, t_f	Output Rise/Fall Time (20% to 80%)	Note 4		60	120	ps
t_{JITTER}	Deterministic Random	Note 5 Note 6		15 5		ps_{PP} ps_{RMS}
V_{ID}	Differential Input Voltage Swing	Figure 1	5		1800	mV_{PP}
V_{OD}	Differential Output Voltage Swing	$V_{ID} \geq 18mV_{PP}$, Figure 1	700	800	950	mV_{PP}
T_{OFF}	LOS Release Time			2	10	µs
T_{ON}	LOS Assert Time			2	10	µs
LOS_{AL}	Low LOS Assert Level	R_{LOSLVL} = 15kΩ, Note 8		3.1		mV_{PP}
LOS_{DL}	Low LOS De-assert Level	R_{LOSLVL} = 15kΩ, Note 8		4.8		mV_{PP}
HYS_L	Low LOS Hysteresis	R_{LOSLVL} = 15kΩ, Note 7		3.8		dB
LOS_{AM}	Medium LOS Assert Level	R_{LOSLVL} = 5kΩ, Note 8	3	5.2		mV_{PP}
LOS_{DM}	Medium LOS De-assert Level	R_{LOSLVL} = 5kΩ, Note 8		7.5	11	mV_{PP}
HYS_M	Medium LOS Hysteresis	R_{LOSLVL} = 5kΩ, Note 7	2	3.2	4.5	dB
LOS_{AH}	High LOS Assert Level	R_{LOSLVL} = 100Ω, Note 8	8	12		mV_{PP}
LOS_{DH}	High LOS De-assert Level	R_{LOSLVL} = 100Ω, Note 8		18	23	mV_{PP}
HYS_H	High LOS Hysteresis	R_{LOSLVL} = 100Ω, Note 7	2	3.5	4.5	dB
B_{-3dB}	3dB Bandwidth			2		GHz
$A_{V(Diff)}$	Differential Voltage Gain		32	38		dB
S_{21}	Single-ended Small-Signal Gain		26	32		dB

Notes:

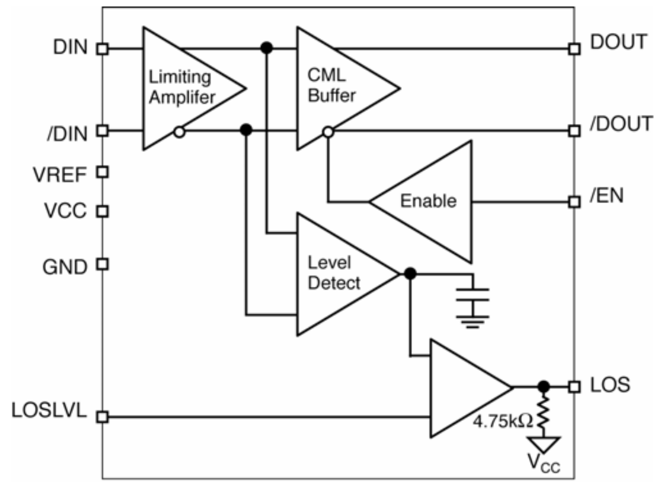
4. Amplifier in limiting mode. Input is a 200MHz square wave.
5. Deterministic jitter measured using 3.2Gbps K28.5 pattern, V_{ID} = 10mV_{PP}.
6. Random jitter measured using 3.2Gbps K28.7 pattern, V_{ID} = 10mV_{PP}.
7. This specification defines electrical hysteresis as 20log (LOS De-assert/LOS Assert). The ratio between optical hysteresis and electrical hysteresis is found to vary between 1.5 and 2 depending upon the level of received optical power and ROSA characteristics. Based on that ratio, the optical hysteresis corresponding to the electrical hysteresis range 1dB-4.5dB, shown in the AC characteristics table will be 0.5dB-3dB Optical Hysteresis.
8. See "Typical Operating Characteristics" for a graph showing how to choose a particular R_{LOSLVL} for a particular LOS assert and its associated de-assert amplitude.

Typical Operating Characteristics





Functional Block Diagram



Detailed Description

The SY88289BL high-sensitivity limiting post amplifier operates from a single +3.3V power supply, over temperatures from –40°C to +85°C. Signals with data rates up to 3.2Gbps and as small as 5mV$_{PP}$ can be amplified. Figure 1 shows the allowed input voltage swing. The SY88289BL generates a LOS output. LOS$_{LVL}$ sets the sensitivity of the input amplitude detection.

Input Amplifier/Buffer

Figure 2 shows a simplified schematic of the SY88289BL's input stage. The high-sensitivity of the input amplifier allows signals as small as 5mV$_{PP}$ to be detected and amplified. The input amplifier also allows input signals as large as 1800mV$_{PP}$. Input signals are linearly amplified with a typical 38dB differential voltage gain. Since it is a limiting amplifier, the SY88289BL outputs typically 800mV$_{PP}$ voltage-limited waveforms for input signals that are greater than 12mV$_{PP}$. Applications requiring the SY88289BL to operate with high-gain should have the upstream TIA placed as close as possible to the SY88289BL's input pins to ensure the best performance of the device.

Output Buffer

The SY88289BL's CML output buffer is designed to drive 50Ω lines. The output buffer requires appropriate termination for proper operation. An external 50Ω resistor to V$_{CC}$ for each output pin provides this. Figure 3 shows a simplified schematic of the output stage.

Loss-of-signal

The SY88289BL generates a chatter-free LOS open-collector TTL output with an internal 4.75kΩ pull-up resistor as shown in Figure 4. LOS is used to determine that the input amplitude is large enough to be considered a valid input. LOS asserts high if the input amplitude falls below the threshold set by LOS$_{LVL}$ and de-asserts low otherwise. LOS can be fed back to the enable bar (/EN) input to maintain output stability under a loss of signal condition. /EN de-asserts the true output signal without removing the input signals. Typical 3.5dB LOS hysteresis is provided to prevent chattering.

Loss-of-signal Level Set

A programmable LOS level set pin (LOS$_{LVL}$) sets the threshold of the input amplitude detection. Connecting an external resistor between V$_{CC}$ and LOS$_{LVL}$ sets the voltage at LOS$_{LVL}$. This voltage ranges from V$_{CC}$ to V$_{REF}$. The external resistor creates a voltage divider between V$_{CC}$ and V$_{REF}$, as shown, in Figure 5.

Hysteresis

The SY88289BL provides typically 3.5dB LOS electrical hysteresis. By definition, a power ratio measured in dB is 10log (power ratio). Power is calculated as V^2_{IN}/R for an electrical signal. Hence, the same ratio can be stated as 20log (voltage ratio). While in linear mode, the electrical voltage input changes linearly with the optical power and therefore, the ratios change linearly. Thus, the optical hysteresis in dB is half the electrical hysteresis in dB given in the data sheet. Since the SY88289BL is an electrical device, this data sheet refers to hysteresis in electrical terms. With 3.5dB LOS hysteresis, a voltage factor of 1.5 is required to assert or de-assert LOS.

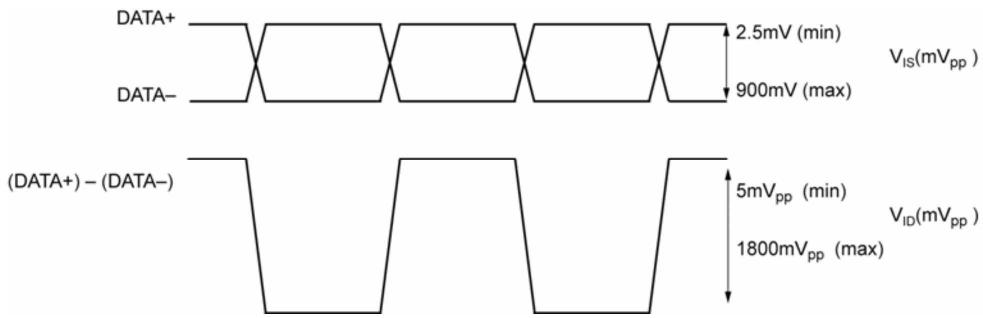


Figure 1. V_{IS} and V_{ID} Definition

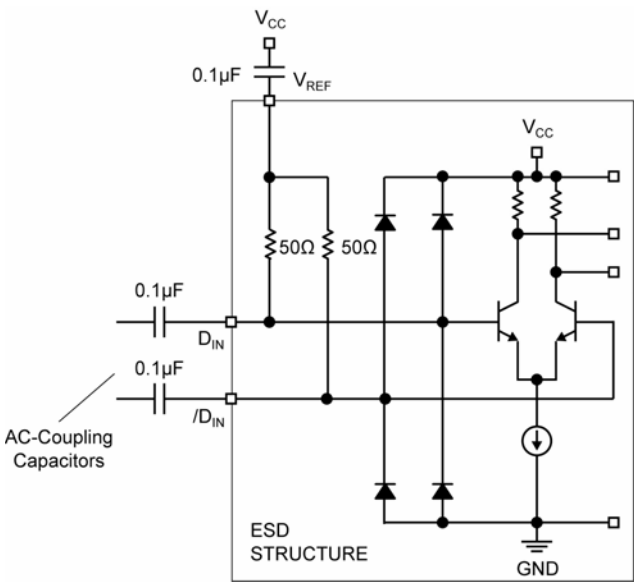


Figure 2. Input Structure

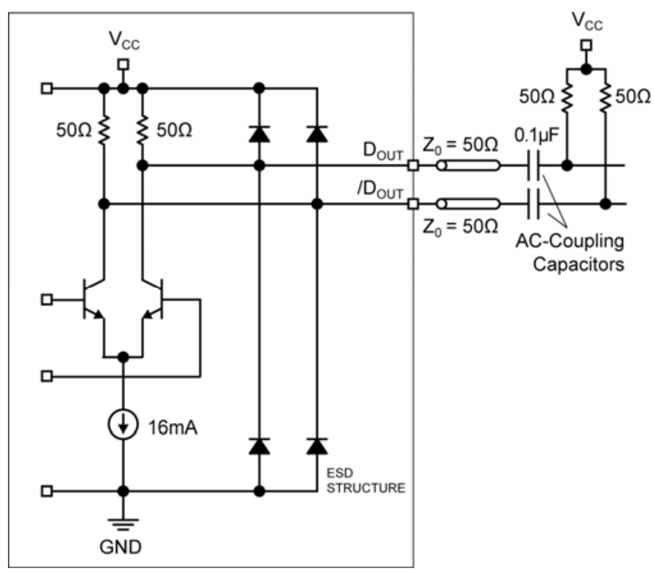


Figure 3. Output Structure

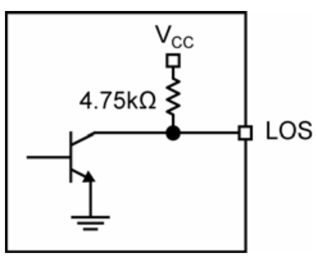


Figure 4. Input Structure

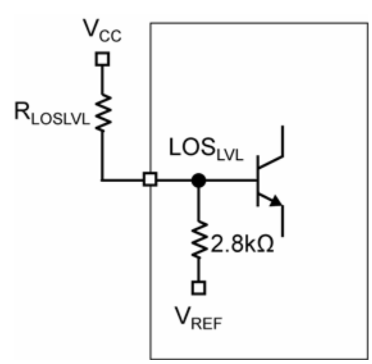
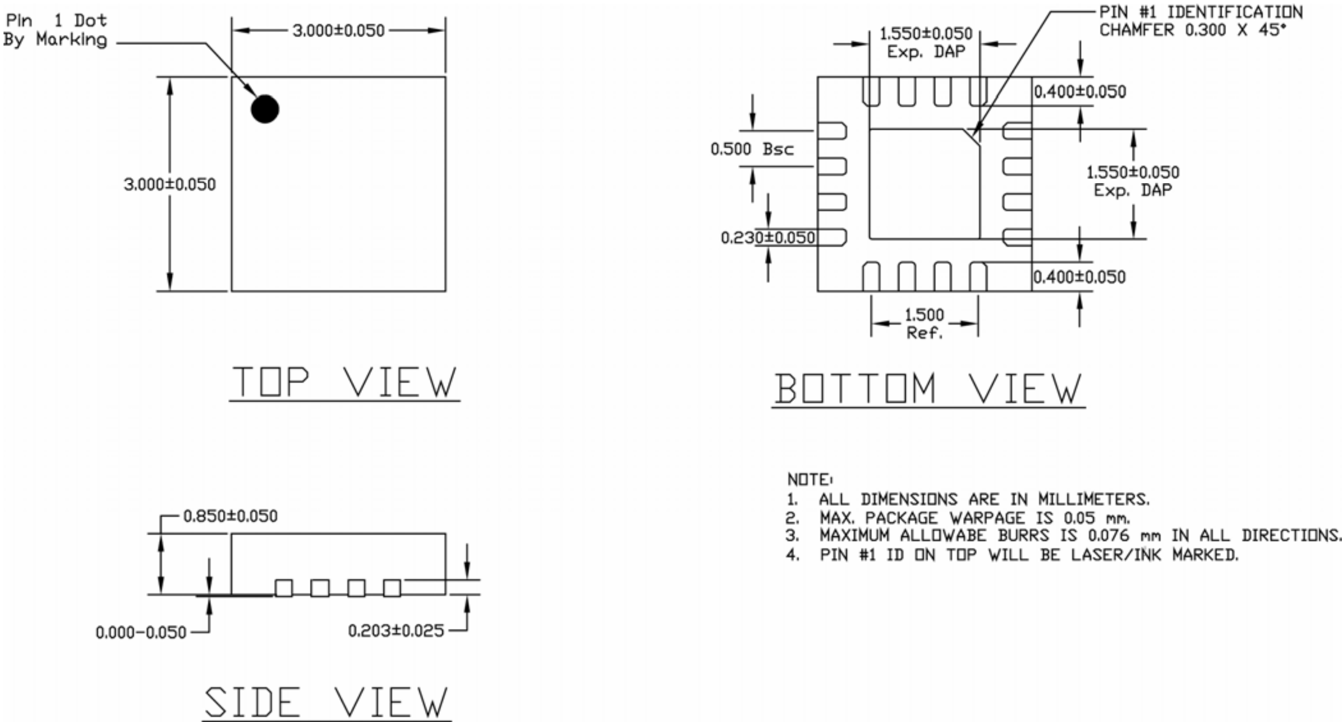
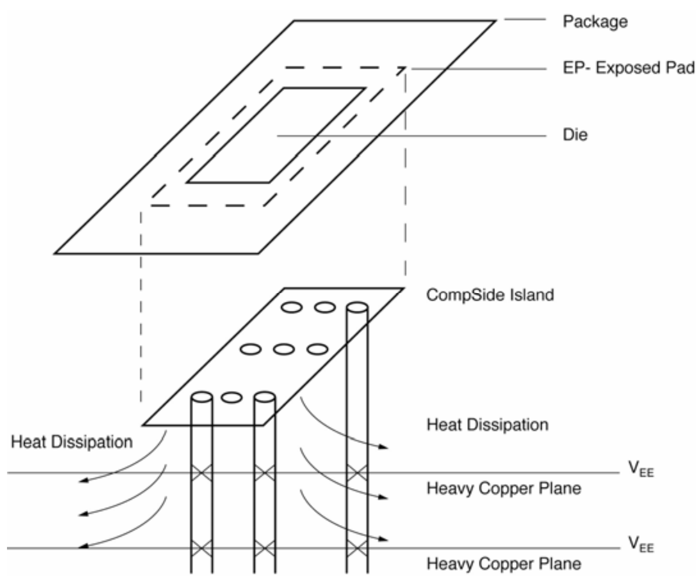


Figure 5. LOS_{LVL} Setting Circuit

Package Information





PCB Thermal Consideration for 16-Pin MLF® Package

Package Notes:

1. Package meets Level Moisture Sensitivity Classification and is shipped in dry-pack form.
2. Exposed pad must be soldered to a ground for proper thermal management.

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