

FEATURES

- 3.3V core supply, 1.8V output supply for reduced power
- LVPECL and HSTL inputs
- 22 differential HSTL (low-voltage swing) output pairs
- HSTL outputs drive 50Ω to ground with no offset voltage
- Low part-to-part skew (200ps max.)
- Low pin-to-pin skew (50ps max.)
- Available in a 64-Pin EPAD-TQFP

APPLICATIONS

- High-performance PCs
- Workstations
- Parallel processor-based systems
- Other high-performance computing
- Communications



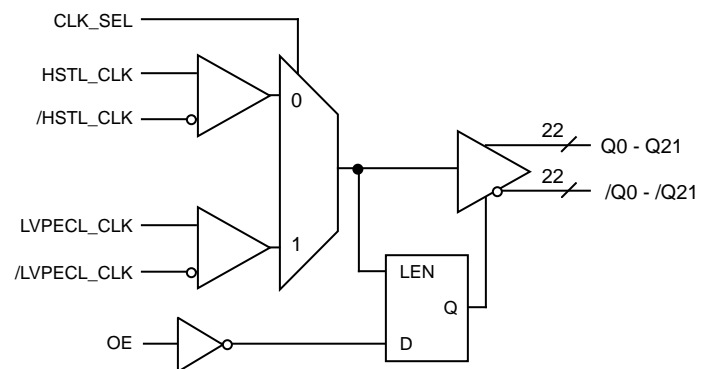
Precision Edge®

DESCRIPTION

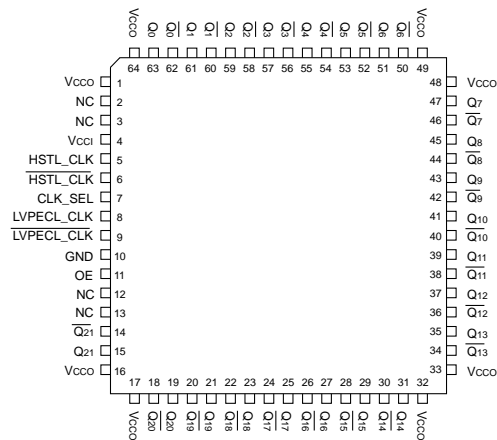
The SY89824L is a High Performance Bus Clock Driver with 22 differential HSTL (High Speed Transceiver Logic) output pairs. The part is designed for use in low voltage (3.3V/1.8V) applications which require a large number of outputs to drive precisely aligned, ultra low skew signals to their destination. The input is multiplexed from either HSTL or LVPECL (Low Voltage Positive Emitter Coupled Logic) by the CLK_SEL pin. The Output Enable (OE) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control.

The SY89824L features low pin-to-pin skew (50ps max.) and low part-to-part skew (200ps max.)—performance previously unachievable in a standard product having such a high number of outputs. The SY89824L is available in a single space saving package, enabling a lower overall cost solution.

LOGIC SYMBOL



PACKAGE/ORDERING INFORMATION



64-Pin EPAD-TQFP (H64-1)

Ordering Information⁽¹⁾

| Part Number | Package Type | Operating Range | Package Marking | Lead Finish |
|--------------------------------|--------------|-----------------|--|------------------|
| SY89824LHC | H64-1 | Commercial | SY89824LHC | Sn-Pb |
| SY89824LHCTR ⁽²⁾ | H64-1 | Commercial | SY89824LHC | Sn-Pb |
| SY89824LHZ ⁽³⁾ | H64-1 | Commercial | SY89824LHZ with Pb-Free bar-line indicator | Pb-Free Matte-Sn |
| SY89824LHZTR ^(2, 3) | H64-1 | Commercial | SY89824LHZ with Pb-Free bar-line indicator | Pb-Free Matte-Sn |

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC electricals only.
2. Tape and Reel.
3. Pb-Free package recommended for new designs.

PIN NAMES

| Pin | Function |
|-------------------------|----------------------------|
| HSTL_CLK, /HSTL_CLK | Differential HSTL Inputs |
| LVPECL_CLK, /LVPECL_CLK | Differential LVPECL Inputs |
| CLK_SEL | Input CLK Select (LVTTL) |
| OE | Output Enable (LVTTL) |
| Q0-Q21, /Q0-/Q21 | Differential HSTL Outputs |
| GND | Ground |
| Vcci | Vcc Core |
| Vcco | Vcc Output |

TRUTH TABLE

| OE ⁽¹⁾ | CLK_SEL | Q0-Q21 | /Q0-/Q21 |
|-------------------|---------|------------|-------------|
| 0 | 0 | LOW | HIGH |
| 0 | 1 | LOW | HIGH |
| 1 | 0 | HSTL_CLK | /HSTL_CLK |
| 1 | 1 | LVPECL_CLK | /LVPECL_CLK |

SIGNAL GROUPS

| Level | Direction | Signal |
|---------------|-----------|-------------------------|
| HSTL | Input | HSTL_CLK, /HSTL_CLK |
| HSTL | Output | Q0-Q21, /Q0-/Q21 |
| LVPECL | Input | LVPECL_CLK, /LVPECL_CLK |
| LVC MOS/LVTTL | Input | CLK_SEL, OE |

NOTE:

- The OE (output enable) signal is synchronized with the low level of the HSTL_CLK and LVPECL_CLK signal.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Rating | Value | Unit |
|-------------------------------------|--|--------------------------|------|
| V _{CCI} , V _{CCO} | V _{CC} Pin Potential to Ground Pin | -0.5 to +4.0 | V |
| V _{IN} | Input Voltage | -0.5 to V _{CCI} | V |
| I _{OUT} | DC Output Current (Output HIGH) | -50 | mA |
| T _{LEAD} | Lead Temperature (soldering, 20sec.) | 260 | °C |
| T _{store} | Storage Temperature | -65 to +150 | °C |
| θ _{JA} | Package Thermal Resistance (Junction-to-Ambient) | | |
| | With Die attach soldered to GND: | | |
| | -Still-Air (TQFP) | 23 | °C/W |
| | -200lfpm (TQFP) | 18 | °C/W |
| | -500lfpm (TQFP) | 15 | °C/W |
| | With Die attach NOT soldered to GND: | | |
| -Still-Air (TQFP) | 44 | °C/W | |
| -200lfpm (TQFP) | 36 | °C/W | |
| -500lfpm (TQFP) | 30 | °C/W | |
| θ _{JC} | Package Thermal Resistance (Junction-to-Case) | 4.3 | °C/W |

NOTE:

- Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data book. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS**Power Supply**

| Symbol | Parameter | T _A = 0°C | | | T _A = +25°C | | | T _A = +85°C | | | Unit |
|------------------|------------------------|----------------------|------|------|------------------------|------|------|------------------------|------|------|------|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| V _{CCI} | V _{CC} Core | 3.0 | 3.3 | 3.6 | 3.0 | 3.3 | 3.6 | 3.0 | 3.3 | 3.6 | V |
| V _{CCO} | V _{CC} Output | 1.6 | 1.8 | 2.0 | 1.6 | 1.8 | 2.0 | 1.6 | 1.8 | 2.0 | V |
| I _{CCI} | I _{CC} Core | — | 115 | 140 | — | 115 | 140 | — | 115 | 140 | mA |

HSTL

| Symbol | Parameter | T _A = 0°C | | | T _A = +25°C | | | T _A = +85°C | | | Unit |
|-----------------|------------------------------------|----------------------|------|----------------------|------------------------|------|----------------------|------------------------|------|----------------------|------|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| V _{OH} | Output HIGH Voltage ⁽¹⁾ | 1.0 | — | 1.2 | 1.0 | — | 1.2 | 1.0 | — | 1.2 | V |
| V _{OL} | Output LOW Voltage ⁽¹⁾ | 0.2 | — | 0.4 | 0.2 | — | 0.4 | 0.2 | — | 0.4 | V |
| V _{IH} | Input HIGH Voltage | V _X + 0.1 | — | 1.6 | V _X + 0.1 | — | 1.6 | V _X + 0.1 | — | 1.6 | V |
| V _{IL} | Input LOW Voltage | -0.3 | — | V _X - 0.1 | -0.3 | — | V _X - 0.1 | -0.3 | — | V _X - 0.1 | V |
| V _X | Input Crossover Voltage | 0.68 | — | 0.9 | 0.68 | — | 0.9 | 0.68 | — | 0.9 | V |
| I _{IH} | Input HIGH Current | +20 | — | -350 | +20 | — | -350 | +20 | — | -350 | μA |
| I _{IL} | Input LOW Current | — | — | -500 | — | — | -500 | — | — | -500 | μA |

NOTE:

1. Outputs loaded with 50Ω to ground.

LVPECL

| Symbol | Parameter | T _A = 0°C | | T _A = +25°C | | T _A = +85°C | | Unit |
|-----------------|--------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| V _{IH} | Input HIGH Voltage | V _{CCI} - 1.165 | V _{CCI} - 0.880 | V _{CCI} - 1.165 | V _{CCI} - 0.880 | V _{CCI} - 1.165 | V _{CCI} - 0.880 | V |
| V _{IL} | Input LOW Voltage | V _{CCI} - 1.810 | V _{CCI} - 1.475 | V _{CCI} - 1.810 | V _{CCI} - 1.475 | V _{CCI} - 1.810 | V _{CCI} - 1.475 | V |
| I _{IH} | Input HIGH Current | — | +150 | — | +150 | — | +150 | μA |
| I _{IL} | Input LOW Current | 0.5 | — | 0.5 | — | 0.5 | — | μA |

LVC MOS/LVTTL

| Symbol | Parameter | T _A = 0°C | | | T _A = +25°C | | | T _A = +85°C | | | Unit |
|-----------------|--------------------|----------------------|------|------|------------------------|------|------|------------------------|------|------|------|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| V _{IH} | Input HIGH Voltage | 2.0 | — | — | 2.0 | — | — | 2.0 | — | — | V |
| V _{IL} | Input LOW Voltage | — | — | 0.8 | — | — | 0.8 | — | — | 0.8 | V |
| I _{IH} | Input HIGH Current | +20 | — | -250 | +20 | — | -250 | +20 | — | -250 | μA |
| I _{IL} | Input LOW Current | — | — | -600 | — | — | -600 | — | — | -600 | μA |

AC ELECTRICAL CHARACTERISTICS⁽¹⁾

| Symbol | Parameter | T _A = 0°C | | | T _A = +25°C | | | T _A = +85°C | | | Unit |
|----------------------------------|--|----------------------|------|------|------------------------|------|------|------------------------|------|------|------|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| t _{PD} | Propagation Delay ⁽²⁾ | — | 1.0 | — | — | 1.0 | — | — | 1.0 | — | ns |
| t _{SKEW} | Within-Device Skew ⁽³⁾ | — | — | 50 | — | — | 50 | — | — | 50 | ps |
| t _{SKPP} | Part-to-Part Skew ⁽⁴⁾ | — | — | 200 | — | — | 200 | — | — | 200 | ps |
| V _{PP} | Minimum Input Swing ⁽⁵⁾ LVPECL_CLK | 600 | — | — | 600 | — | — | 600 | — | — | mV |
| V _{CMR} | Common Mode Range ⁽⁶⁾ LVPECL_CLK | -1.5 | — | -0.4 | -1.5 | — | -0.4 | -1.5 | — | -0.4 | V |
| t _S | OE Set-Up Time ⁽⁷⁾ | 1.0 | — | — | 1.0 | — | — | 1.0 | — | — | ns |
| t _H | OE Hold Time | 0.5 | — | — | 0.5 | — | — | 0.5 | — | — | ns |
| t _r t _f | Output Rise/Fall Time (20% – 80%) | 300 | — | 700 | 300 | — | 700 | 300 | — | 700 | ps |

NOTES:

1. Outputs loaded with 50Ω to ground. Airflow ≥ 300lfpm.
2. Differential propagation delay is defined as the delay from the crossing point of the differential input signals to the crossing point of the differential output signals.
3. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device operating at the same voltage and temperature.
4. The part-to-part skew is defined as the absolute worst case difference between any two delay paths on any two devices operating at the same voltage and temperature.
5. The V_{PP}(min.) is defined as the minimum input differential voltage which will cause no increase in the propagation delay.
6. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The numbers in the table are referenced to V_{CCI}. The V_{IL} level must be such that the peak-to-peak voltage is less than 1.0V and greater than or equal to V_{PP}(min.). The lower end of the CMR range varies 1:1 with V_{CCI}. The V_{CMR}(min) will be fixed at 3.3V – |V_{CMR}(min)|.
7. OE set-up time is defined with respect to the rising edge of the clock. OE HIGH to LOW transition ensures outputs remain disabled during the next clock cycle. OE LOW to HIGH transition enables normal operation of the next input clock.

WAVEFORMS

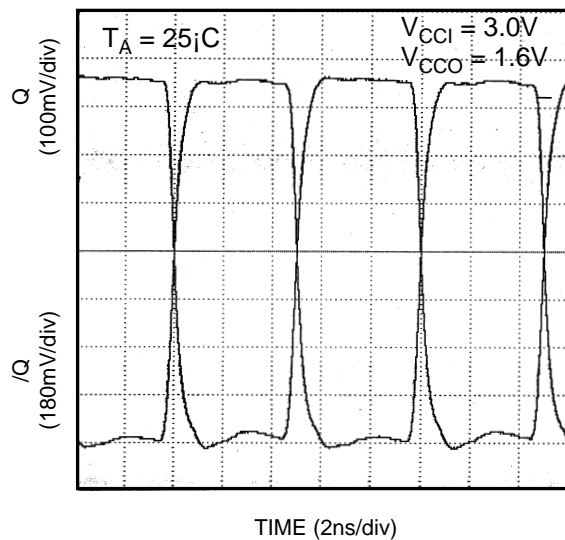


Figure 1. 100MHz Output Waveform

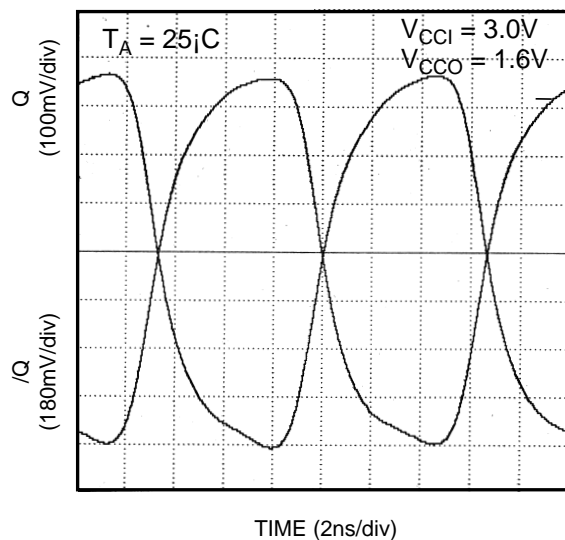
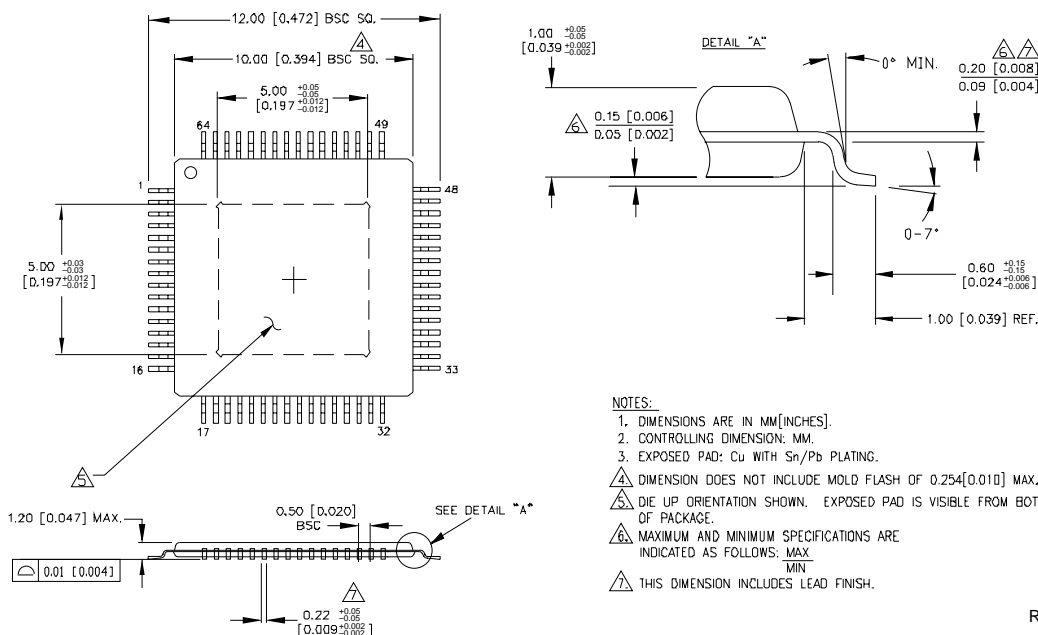
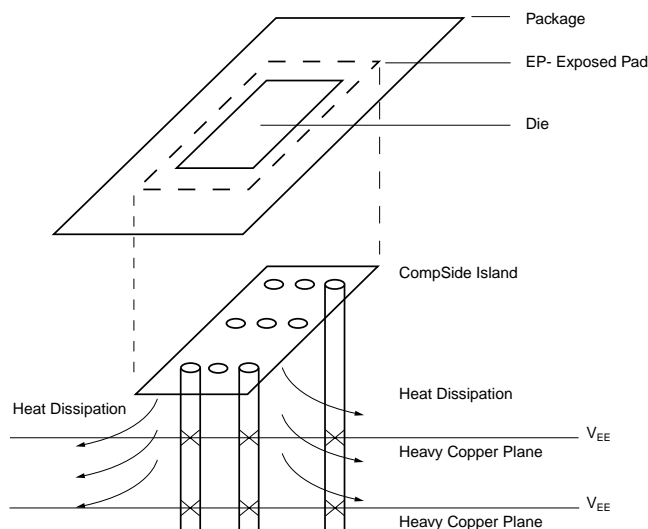


Figure 2. 300MHz Output Waveform

64-PIN EPAD-TQFP (DIE UP) (H64-1)



Rev. 02



**PCB Thermal Consideration for 64-Pin EPAD-TQFP Package
(Always solder, or equivalent, the exposed pad to the PCB)**

Package Notes:

- Note 1.** Package meets Level 2 qualification.
- Note 2.** All parts are 100% baked and dry-packaged before shipment.
- Note 3.** Exposed pads must be soldered to a ground for proper thermal management.

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