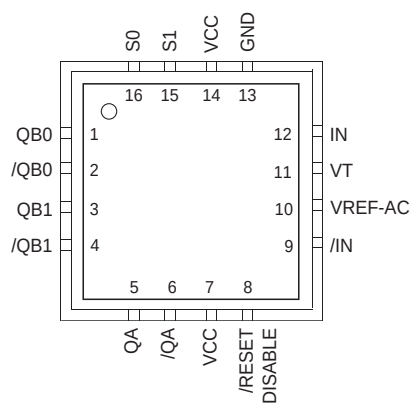




PACKAGE/ORDERING INFORMATION



16-Pin MLF® (MLF-16)

Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89873LMI	MLF-16	Industrial	873L	Sn-Pb
SY89873LMITR ⁽²⁾	MLF-16	Industrial	873L	Sb-Pb
SY89873LMG ⁽³⁾	MLF-16	Industrial	873L with Pb-Free bar line indicator	NiPdAu Pb-Free
SY89873LMGTR ^(2, 3)	MLF-16	Industrial	873L with Pb-Free bar line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25^\circ\text{C}$, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
1, 2, 3, 4	QB0, /QB0 QB1, /QB1	Differential Buffered Output Clocks: Divide by 2, 4, 8, 16. LVDS compatible.
5, 6	QA, /QA	Differential Buffered Undivided Output Clock: LVDS compatible.
7, 14	VCC	Positive Power Supply: Bypass with 0.1 μF /0.01 μF low ESR capacitors.
8	/RESET, /DISABLE	TTL/CMOS Compatible Output Reset and Disable: Internal 25k Ω pull-up. Input threshold is $V_{CC}/2$. Logic LOW will reset the divider select, and align Bank A and Bank B edges. In addition, when LOW, Banks A and B will be disabled.
12, 9	IN, /IN	Differential Input: Internal 50 Ω termination resistors to V_T input. See "Input Interface Applications" section.
10	VREF-AC	Reference Voltage: Equal to $V_{CC}-1.4\text{V}$ (approx.), and used for AC-coupled applications. Maximum sink/source current is 0.5mA. See "Input Interface Applications" section.
11	VT	Termination Center-Tap: For CML and LVDS inputs, leave this pin floating. Otherwise, see "Input Interface Applications" section.
13	GND	Ground: Exposed pad is internally connected to GND and must be connected to a ground plane for proper thermal operation.
16, 15	S0, S1	Select Pins: LVTTL/CMOS logic levels. Internal 25k Ω pull-up resistor. Logic HIGH if left unconnected (divided by 16 mode). S0 = LSB. Input threshold is $V_{CC}/2$.

TRUTH TABLE

/RESET /DISABLE	S1	S0	Bank A Output	Bank B Outputs
1	0	0	Input Clock	Input Clock $\div 2$
1	0	1	Input Clock	Input Clock $\div 4$
1	1	0	Input Clock	Input Clock $\div 8$
1	1	1	Input Clock	Input Clock $\div 16$
0	X	X	QA = LOW, /QA = HIGH ⁽¹⁾	QB0 = LOW, /QB0 = HIGH ⁽²⁾ QB1 = LOW, /QB1 = HIGH ⁽²⁾

Notes:

1. On the next negative transition of the input signal.
2. Asynchronous Reset/Disable function. See "Timing Diagram."

Absolute Maximum Ratings⁽¹⁾

Supply Voltage (V_{CC})	–0.5V to +4.0V
Input Voltage (V_{IN})	–0.5V to $V_{CC}+0.3$
LVDS Output Current (I_{OUT})	±10mA
Input Current I_N , I_{IN} (I_{IN})	±50mA
V_{REF-AC} Input Sink/Source Current ($I_{VREF-AC}$) ⁽³⁾	±2mA
Lead Temperature (soldering, 20 sec.)	260°C
Storage Temperature (T_S)	–65°C to +150°C

Operating Ratings⁽²⁾

Supply Voltage (V_{CC})	+3.3V ±10%
Ambient Temperature (T_A)	–40°C to +85°C
Package Thermal Resistance	
MLF® (θ_{JA})	
Still-Air	60°C/W
500 lfpm	54°C/W
MLF® (Ψ_{JB}) ⁽⁴⁾	
Junction-to-Board	38°C/W

DC ELECTRICAL CHARACTERISTICS⁽⁵⁾

T_A = –40°C to +85°C; Unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply		3.0	3.3	3.6	V
I_{CC}	Power Supply Current	No load, Max V_{CC}		85	115	mA
R_{IN}	Differential Input Resistance (I_N -to- I_{IN})		90	100	110	Ω
V_{IH}	Input High Voltage I_N , I_{IN}	Note 6	0.1		$V_{CC}+0.3$	V
V_{IL}	Input Low Voltage I_N , I_{IN}	Note 6	–0.3		$V_{CC}+0.2$	V
V_{IN}	Input Voltage Swing	Notes 6, 7	0.1		3.6	V
V_{DIFF_IN}	Differential Input Voltage Swing	Notes 6, 7, 8	0.2			V
$ I_{IN} $	Input Current I_N , I_{IN}	Note 6			45	mA
V_{REF-AC}	Reference Voltage	Note 9	$V_{CC}-1.525$	$V_{CC}-1.425$	$V_{CC}-1.325$	V

Notes:

1. Permanent device damage may occur if “*Absolute Maximum Ratings*” are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to “*Absolute Maximum Ratings*” conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Due to the limited drive capability use for input of the same package only.
4. Junction-to-board resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6. Due to the internal termination (see “*Input Buffer Structure*”) the input current depends on the applied voltages at I_N , I_{IN} and V_T inputs. Do not apply a combination of voltages that causes the input current to exceed the maximum limit!
7. See “*Timing Diagram*” for V_{IN} definition. $V_{IN(max)}$ is specified when V_T is floating.
8. See Figures 1c and 1d for V_{DIFF} definition.
9. Operating using V_{IN} is limited to AC-coupled PECL or CML applications only. Connect directly to V_T pin.

LVDS OUTPUT DC ELECTRICAL CHARACTERISTICS⁽¹⁰⁾

$V_{CC} = 3.3V \pm 10\%$; $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$; Unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT}	Output Voltage Swing	Notes 11, 12	250	350	450	mV
V_{OH}	Output High Voltage	Note 11			1.475	V
V_{OL}	Output Low Voltage	Note 11	0.925			V
V_{OCM}	Output Common Mode Voltage	Note 11	1.125		1.275	V
ΔV_{OCM}	Change in Common Mode Voltage		-50		50	mV

LVTTTL/CMOS DC ELECTRICAL CHARACTERISTICS⁽¹⁰⁾

$V_{CC} = 3.3V \pm 10\%$; $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$; Unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current		-125		20	μA
I_{IL}	Input LOW Current				-300	μA

Notes:

10. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

11. Measured as per Figure 1a, 100 Ω across Q and /Q outputs.

12. See Figure 1c.

AC ELECTRICAL CHARACTERISTICS⁽¹³⁾

$V_{CC} = 3.3V \pm 10\%$; $T_A = -40^\circ C$ to $+85^\circ C$; Unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Output Toggle Frequency (Bank A and Bank B)	Output Swing: $\geq 200mV$	2.0			GHz
	Maximum Input Frequency	Note 14	3.2			GHz
t_{PD}	Differential Propagation Delay (IN-to-Q)	Input Swing $< 400mV$	550	660	800	ps
		Input Swing $\geq 400mV$	500	610	750	ps
t_{SKEW}	Within-Device Skew (diff.) (QB0-to-QB1)	Note 15		7	15	ps
	Within-Device Skew (diff.) (Bank A-to-Bank B)	Note 15		12	30	ps
	Part-to-Part Skew (diff.)	Note 15			250	ps
t_{rr}	Reset Recovery Time	Note 16	600			ps
T_{jitter}	Cycle-to-Cycle Jitter	Note 17			1	ps _{RMS}
	Total Jitter	Note 18			10	ps _{pp}
t_r, t_f	Rise / Fall Time (20% to 80%)		60	110	190	ps

Notes:

13. Measured with 400mV input signal, 50% duty cycle. All outputs terminated with 100Ω between Q and /Q, unless otherwise stated.
14. Bank A (pass-through) maximum frequency is limited by the output stage. Bank B (input-to-output +2, +4, +8, +16) can accept an input frequency $> 3GHz$, while Bank A will be slew-rate limited.
15. Skew is measured between outputs under identical transitions.
16. See "Timing Diagram."
17. Cycle-to-cycle jitter definition: the variation in period between adjacent cycles over a random sample of adjacent cycle pairs. $T_{jitter_cc} = T_n - T_{n+1}$, where T is the time between rising edges of the output signal.
18. Total jitter definition: with an ideal clock input, of frequency $\leq f_{MAX}$ (device), no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

LVDS OUTPUT

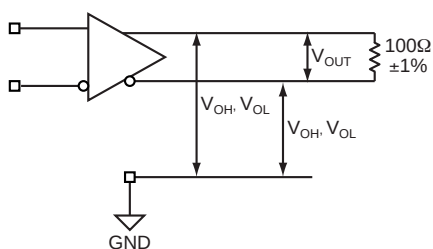


Figure 1a. LVDS Differential Measurement

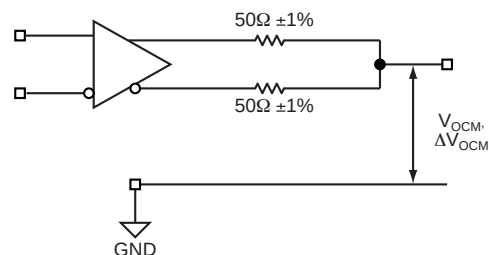


Figure 1b. LVDS Common Mode Measurement

DEFINITION OF SINGLE-ENDED AND DIFFERENTIAL SWING

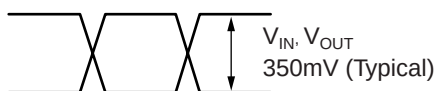


Figure 1c. Single-Ended Swing

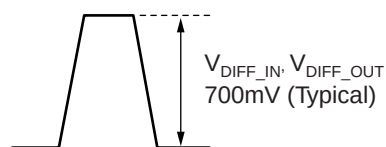
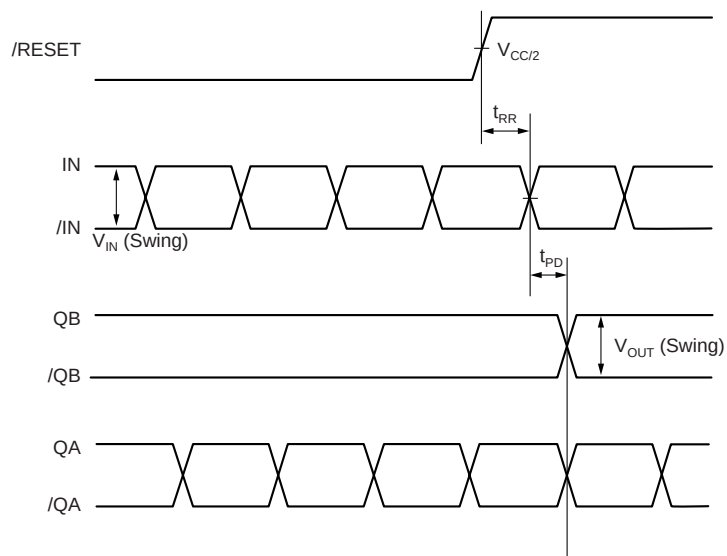


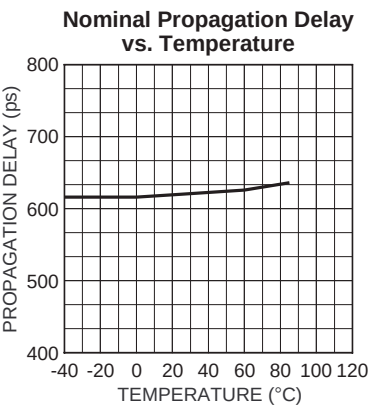
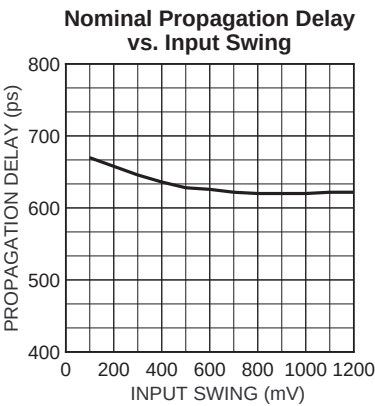
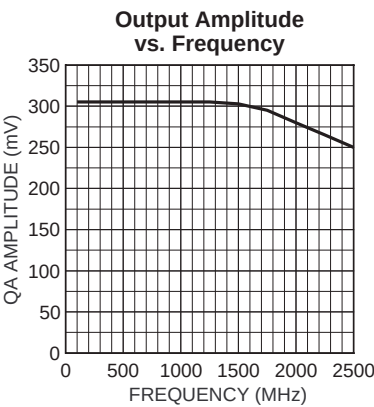
Figure 1d. Differential Swing

TIMING DIAGRAM



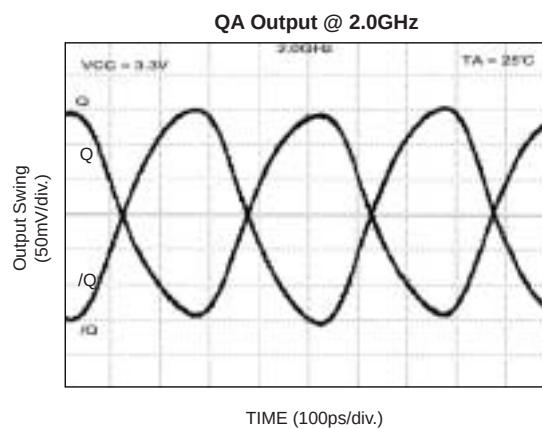
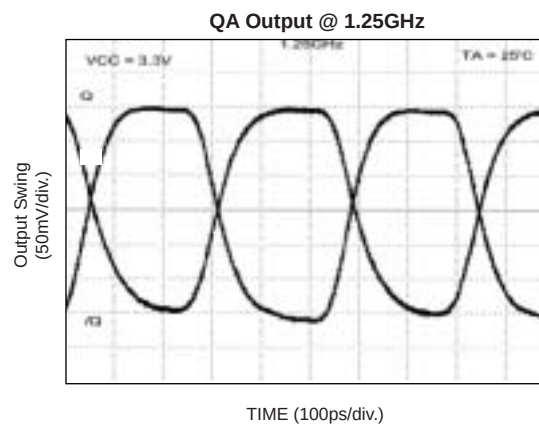
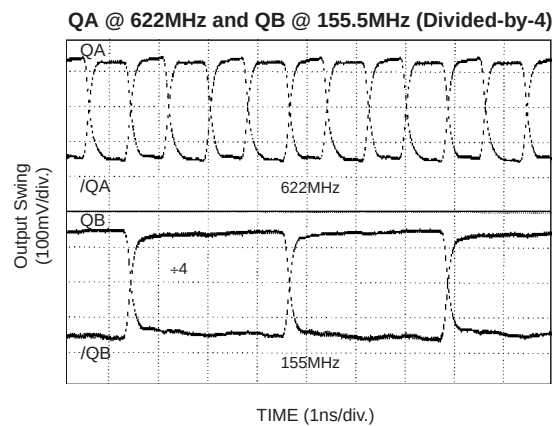
TYPICAL OPERATING CHARACTERISTICS

V_{CC} = 3.3V, V_{IN} = 400mV, T_A = 25°C, unless otherwise stated.



FUNCTIONAL CHARACTERISTICS

Conditions: $V_{CC} = 3.3V$, $T_A = 25^\circ C$, unless otherwise stated.



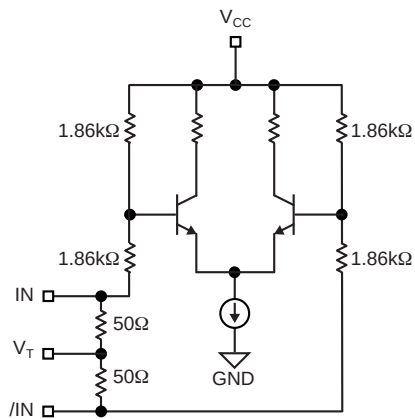
INPUT BUFFER STRUCTURE

Figure 2a. Simplified Differential Input Stage

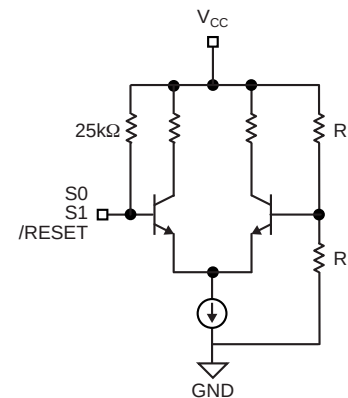


Figure 2b. Simplified TTL/CMOS Input

INPUT INTERFACE APPLICATIONS

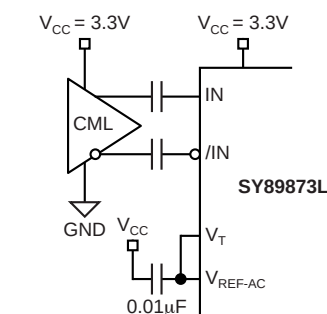


Figure 3b. AC-Coupled CML Input Interface

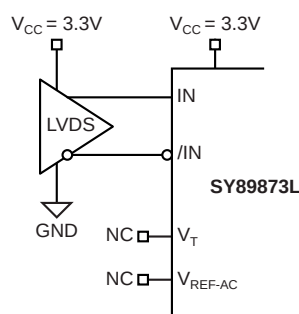
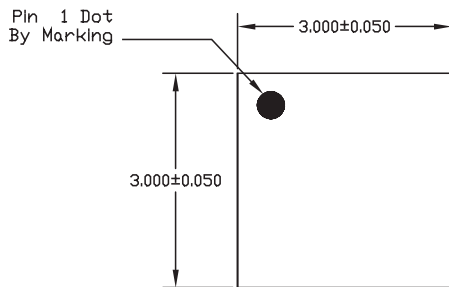


Figure 3e. LVDS Input Interface

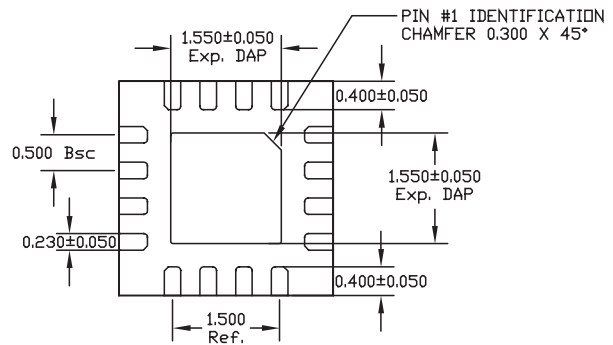
**Figure 3f. HSTL
Input Interface**

RELATED MICREL PRODUCTS AND SUPPORT DOCUMENTATION

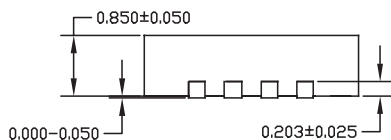
Part Number	Function	Data Sheet Link
SY89871U	2.5GHz Any Diff. In-to-LVPECL Programmable Clock Divider/Fanout Buffer w/Internal Termination	www.micrel.com/product-info/products/sy89871u.shtml
SY89872U	2.5V 2GHz Any Diff. In-to-LVDS Programmable Clock Divider/Fanout Buffer w/Internal Termination	www.micrel.com/product-info/products/sy89872u.shtml
	MLF® Application Note	www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

16-PIN MicroLeadFrame® (MLF-16)

TOP VIEW



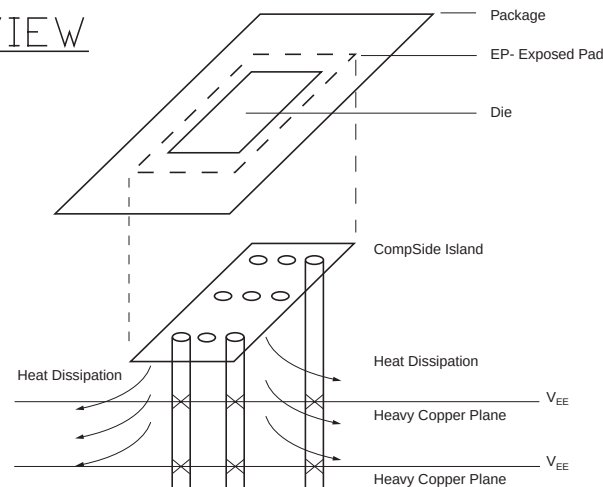
BOTTOM VIEW



SIDE VIEW

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



PCB Thermal Consideration for 16-Pin MLF® Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

1. Package meets Level 2 moisture sensitivity classification, and is shipped in dry-pack form.
2. Exposed pads must be soldered to a ground for proper thermal management.

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