SYA89297U

2.5V/3.3V, 3.2 Gbps, Precision CML Dual-Channel Programmable Delay for Automotive

Features

- Automotive AEC-Q100 Qualified
- Automotive Grade 3 Temperature Range: –40°C to +85°C
- Dual-Channel, Programmable Delay Line
- Serial Programming Interface (SDATA, SCLK, SLOAD)
- Guaranteed AC Performance over Temperature and Voltage:
  - >3.2 Gbps/1.6 GHz f_{MAX}
- Programming Accuracy:
  - Linearity: –15 ps to +15 ps INL
  - Monotonic: –5 ps to +25 ps
  - Resolution: 5 ps Programming Increments
- Low-Jitter Design: 1 ps_{RMS} Typical Random Jitter
- Programmable Delay Range: 5 ns Delay Range
- Cascade Capability for Increased Delay
- Flexible Voltage Operation:
  - V_{CC} = 2.5V ±5% or 3.3V ±10%
- Available in 24-Lead (4 mm x 4 mm) Wettable Flank VQFN Package

Applications

- Clock De-Skewing
- Timing Adjustments
- Aperture Centering
- System Calibration

Markets

- Automotive

General Description

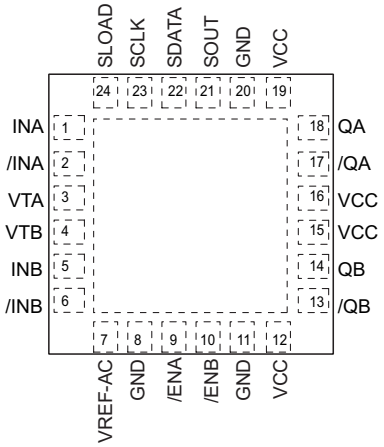
The SYA89297U is a DC-3.2 Gbps programmable, two-channel delay line for automotive applications. Each channel has a delay range from 2 ns to 7 ns (5 ns delta delay) in programmable increments as small as 5 ps. The delay step is extremely linear and monotonic over the entire programming range, with 15 ps INL over temperature and voltage.

The delay varies in discrete steps based on a serial control word provided by the 3-pin serial control (SDATA, SCLK, and SLOAD). The control word for each channel is 10-bits. Both channels are programmed through a common serial interface. For increased delay, multiple SYA89297U delay lines can be cascaded together.

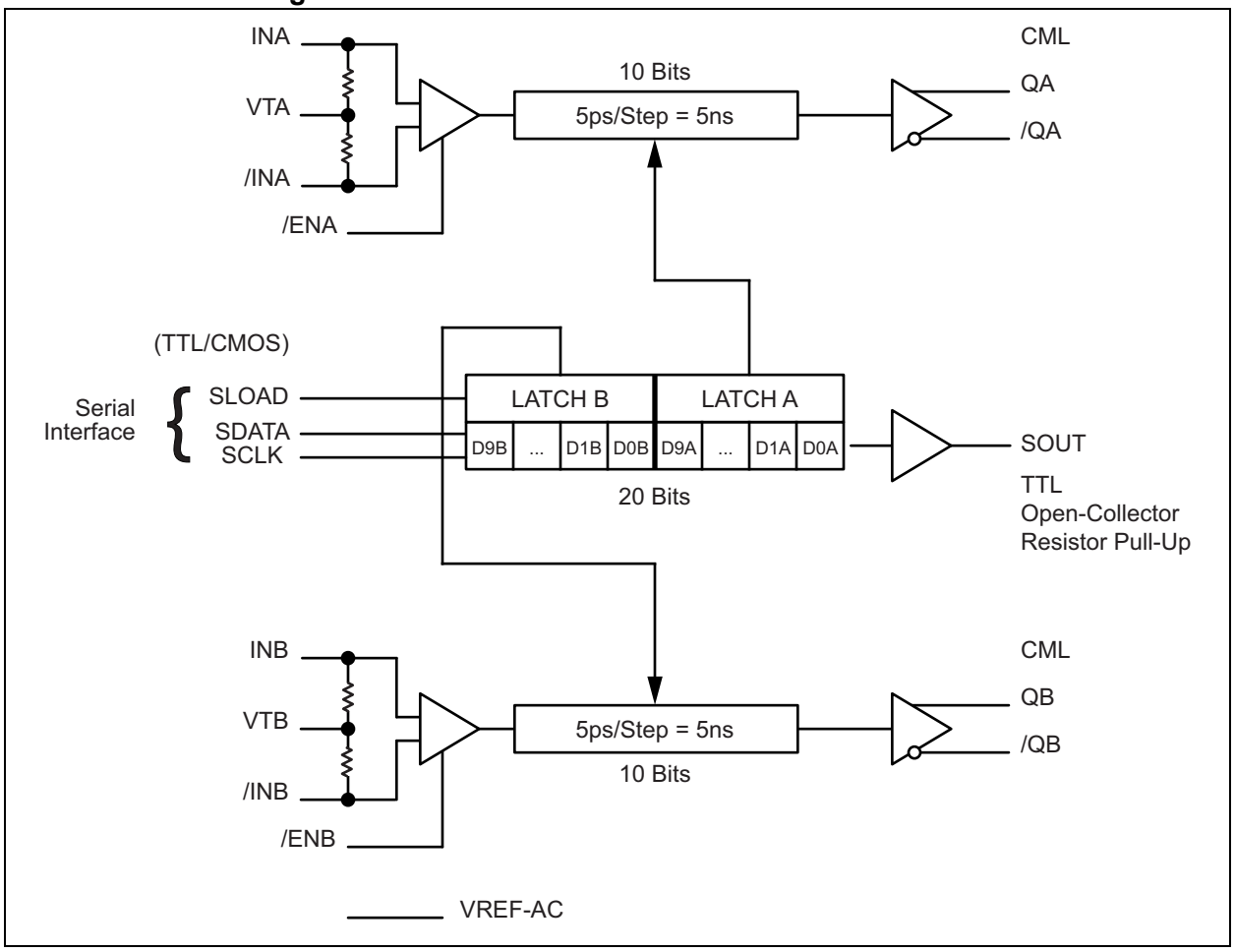
The SYA89297U provides two independent 3.2 Gbps delay lines in an ultra-small 4 mm x 4 mm, 24-lead wettable flank VQFN package.

Package Type

SYA89297U
24-Lead 4x4 VQFN (M)



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
CML Output Voltage (V_{OUT}) ..... V_{CC} – 1.0V to V_{CC} + 0.5V
Current (Source or Sink Current on V_T) ..... ±70 mA
Input Current (Source or Sink Current on IN, /IN) ..... ±35 mA
Current (V_{REF}, Source or Sink Current on V_{REF-AC}) (Note 1) ..... ±0.5 mA

Operating Ratings ‡

Supply Voltage (V_{CC} for T_A = –40°C to +85°C) ..... +2.375V to +2.625V
Supply Voltage (V_{CC} for T_A = –40°C to +75°C) ..... +3.0V to +3.6V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: Due to the limited drive capability, use for input of the same package only.

TABLE 1-1: DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: T_A = –40°C to +85°C, Channels A and B, unless noted. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Voltage Range	V_{CC}	2.375	2.5	2.625	V	T_A = –40°C to +85°C
		3.0	3.3	3.6		T_A = –40°C to +75°C
		3.0	3.3	3.6		T_A = –40°C to +85°C, Airflow = 500 lfpm
Power Supply Current	I_{CC}	—	195	250	mA	Maximum V_{CC}, Both Channels Combined, Output Load Included
Input Resistance (IN-to-VT, /IN-to-VT)	R_{IN}	45	50	55	Ω	—
Differential Input Resistance (IN-to-/IN)	R_{DIFF_IN}	90	100	110	Ω	—
Input HIGH Voltage (IN, /IN)	V_{IH}	1.2	—	V_{CC}	V	—
Input LOW Voltage (IN, /IN)	V_{IL}	0	—	V_{IH} – 0.1	V	—
Input Voltage Swing (IN, /IN)	V_{IN}	0.1	—	1.0	V	See Figure 5-1
Differential Input Voltage Swing (|IN - /IN|)	V_{DIFF_IN}	0.2	—	—	V	See Figure 5-2
Output Reference Voltage	V_{REF-AC}	V_{CC} – 1.3	V_{CC} – 1.2	V_{CC} – 1.1	V	—
Voltage from Input to V_T	V_{T_IN}	—	—	1.28	V	—

Note 1: The circuit is designed to meet the DC specifications show in the table above after thermal equilibrium has been established.

TABLE 1-2: CML OUTPUTS DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = +2.5V +5% or +3.3V ±10%, R_L = 100Ω across the outputs; T_A = –40°C to +85°C, unless otherwise stated. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output HIGH Voltage	V_{OH}	V_{CC} – 0.02	V_{CC} – 0.01	V_{CC}	V	R_L = 50Ω to V_{CC}
Output Voltage Swing	V_{OUT}	325	400	—	mV	See Figure 5-1
Differential Output Voltage Swing	V_{DIFF_OUT}	650	800	—	mV	See Figure 5-2
Output Source Impedance	R_{OUT}	45	50	55	Ω	—

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

TABLE 1-3: LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A = –40°C to +85°C; unless otherwise stated. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input High Voltage	V_{IH}	2.0	—	—	V	—
Input Low Voltage	V_{IL}	—	—	0.8	V	—
Input High Current	I_{IH}	—	—	150	µA	V_{IH} = V_{CC}
Input Low Current	I_{IL}	—	—	50	µA	V_{IL} = 0.8V
Output LOW Voltage	V_{OL}	—	—	0.55	V	SOUT Pin; I_{OL} = 1 mA
Output High Leakage Current		—	—	100	µA	SOUT = V_{CC}

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

TABLE 1-4: AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: T_A = –40°C to +85°C, Channels A and B, unless otherwise stated. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Maximum Operating Frequency	f_{MAX}	1.6	—	—	GHz	Clock: V_{OUT} Swing >200 mV_{pk}
		3.2	—	—	Gbps	NRZ Data
Propagation Delay	t_{pd}	1000	—	2000	ps	IN to Q; D[0-9] = 0
		5500	—	7500		IN to Q; D[0-9] = 1023
		1000	—	2500		/EN to Q: D[0-9] = 0; $V_{TH} = V_{CC}/2$
		2000	—	4500		SDATA to SOUT (D0-D9 = Low), No load
Programmable Range	t_{RANGE}	4150	5115	—	ps	$t_{pd(MAX)} – t_{pd(MIN)}$
Step Delay	Δt	—	5	—	ps	D0 High
		—	10	—		D1 High
		—	20	—		D2 High
		—	40	—		D3 High
		—	80	—		D4 High
		—	160	—		D5 High
		—	320	—		D6 High
		—	640	—		D7 High
		—	1280	—		D8 High
		—	2560	—		D9 High
		—	5115	—		D0-D9 High
		–5	—	25		Monotonic
Integral Non-Linearity	INL	–15	—	15	ps	Note 2
Set-Up Time	t_S	400	—	—	ps	SDATA to SCLK
		400	—	—		SCLK to SLOAD, Note 3
		300	—	—		/EN to IN, Note 4
Hold Time	t_H	300	—	—	ps	SLOAD to SCLK, Note 5
		–100	—	—		IN to /EN, Note 6
		200	—	—		SCLK to SDATA

TABLE 1-4: AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: T_A = –40°C to +85°C, Channels A and B, unless otherwise stated. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Pulse Width	t_{PW}	1000	—	—	ps	SLOAD
Release Time	t_R	800	—	—	ps	/EN to IN, Note 7
Cycle-to-Cycle Jitter	t_{JITTER}	—	—	2	ps_{RMS}	Note 8
Total Jitter		—	—	20	ps_{PP}	Note 9
Random Jitter		—	—	2	ps_{RMS}	Note 10
Output Rise/Fall Time	t_r/t_f	30	55	80	ps	20% to 80% (Q)
Duty Cycle	—	45	—	55	%	Input frequency = 1.6 GHz

Note 1: High frequency AC electricals are guaranteed by design and characterization.

2: INL (Integral Non-Linearity) is defined from its corresponding point on the ideal delay versus D[9:0] curve as the deviation from its ideal delay. The maximum difference is the INL. Theoretical Ideal Linearity (TIL) = (measured maximum delay – measured minimum delay) ÷ 1023. INL = measured delay – (measured minimum delay + (step number x TIL)).

3: SCLK has to transition L-H a setup time before the SLOAD H-L transition to ensure the valid data is properly latched. See Figure 4-2.

4: This setup time is the minimum time that /EN must be asserted prior to the next transition of IN / /IN to prevent an output response greater than ±75 mV to that IN or /IN transition. See Figure 4-3.

5: SCLK has to transition L-H a hold time after the SLOAD H-L transition to ensure that the valid data is properly latched before starting to load new data. See Figure 4-2.

6: This hold time is the minimum time that /EN must remain asserted after a negative going transition of IN to prevent an output response greater than ±75 mV to the IN transition. See Figure 4-3.

7: This release time is the minimum time that /EN must be de-asserted prior to the next IN / /IN transition to affect the propagation delay of IN to Q less than 1 ps. See Figure 4-3.

8: Cycle-to-cycle jitter definition: The variation of periods between adjacent cycles over a random sample of adjacent cycle pairs $T_{jitter\_cc} = T_n – T_n+1$, where T is the time between rising edges of the output signal.

9: Total jitter definition: With an ideal clock input, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

10: Random jitter definition: Jitter that is characterized by a Gaussian distribution, unbounded and is quantified by its standard deviation and mean. Random jitter is measured with a K28.7 comma detect pattern, measured at 1.5 Gbps.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Operating Temperature	T_J	—	—	+125	°C	—
Storage Temperature Range	T_S	–65	—	+150	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 20s
Ambient Temperature Range	T_A	–40	—	+85	°C	—
Package Thermal Resistances, Note 2						
Thermal Resistance VQFN-24	θ_{JA}	—	43	—	°C/W	Still-Air
	Ψ_{JB}	—	30.5	—	°C/W	Junction-to-Board

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2: Thermal performance on VQFN packages assumes exposed pad is soldered (or equivalent) to the device most negative potential (GND).

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

V_{CC} = +2.5V, GND = 0V, V_{IN} = 100 mV, R_L = 100Ω across the outputs, T_A = +25°C for Figure 2-1.

V_{CC} = 2.5V or 3.3V, GND = 0V, V_{IN} = 100 mV, R_L = 100Ω across the outputs, T_A = +25°C, Maximum Delay (D0-D9 = High) for Figure 2-2 through Figure 2-5.

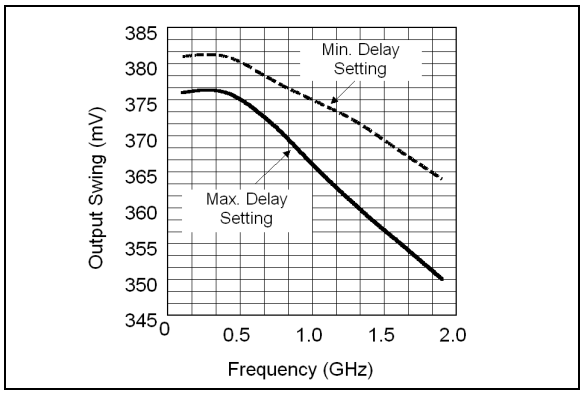


FIGURE 2-1: *Output Swing vs. Frequency.*

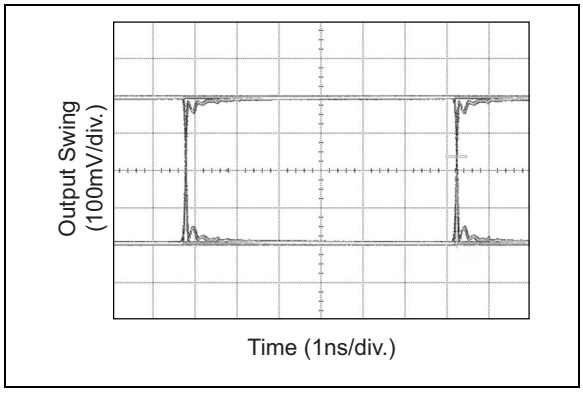


FIGURE 2-2: *155 Mbps Clock.*

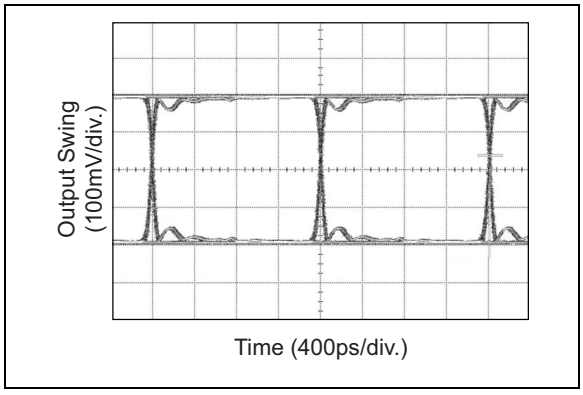


FIGURE 2-3: *622 Mbps Clock.*

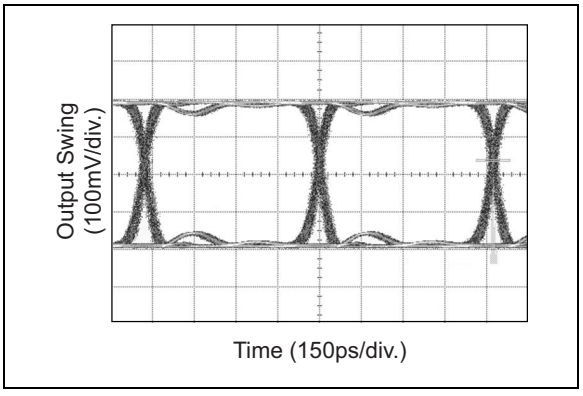


FIGURE 2-4: *1.6 Gbps Clock.*

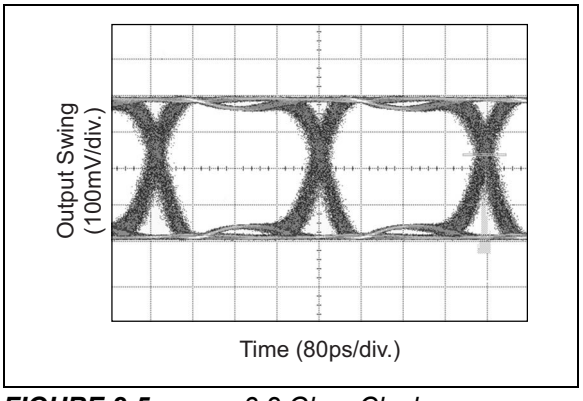


FIGURE 2-5: *3.2 Gbps Clock.*

2.1 Phase Noise Chart

V_{CC} = +2.5V, GND = 0V, V_{IN} = 100 mV, R_L = 100Ω across the outputs, T_A = +25°C.

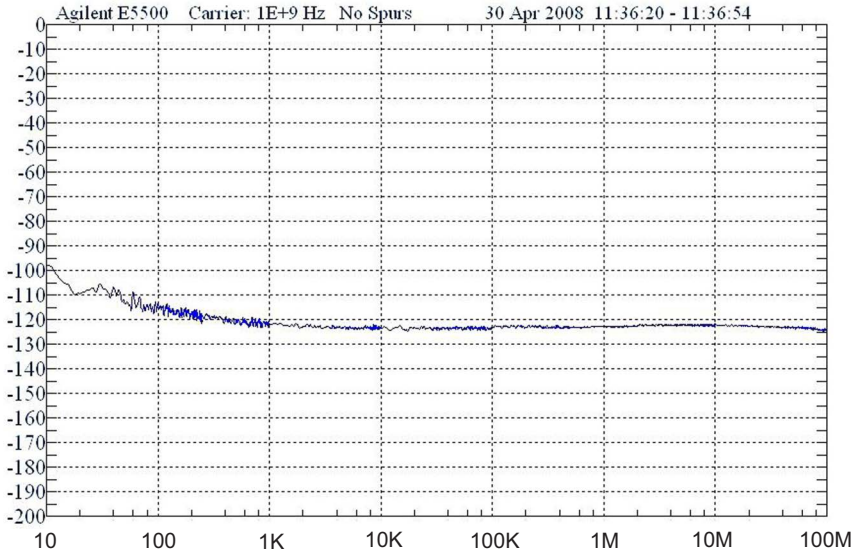


FIGURE 2-6: *f_C: 1 GHz. Delay Setting: 00001 00110 (2 ns).*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1, 2	INA, /INA	Channel A Differential Input: INA and /INA pins receive the Channel A data. QA and /QA are the delayed product of INA and /INA. Each input is internally terminated to VTA through a 50Ω resistor (100Ω across INA and /INA).
3	VTA	Input A Termination Center-Tap: Each side of the differential input pair terminates to this pin. This pin provides a center-tap to a termination network for maximum interface flexibility. See the Input Interface Applications section.
4	VTB	Input B Termination Center-Tap: Each side of the differential input pair terminates to this pin. This pin provides a center-tap to a termination network for maximum interface flexibility. See the Input Interface Applications section.
5, 6	INB, /INB	Channel B Differential Input: INB and /INB pins receive the Channel B data. QB and /QB are the delayed product of INB and /INB. Each input is internally terminated to VTB through a 50Ω resistor (100Ω across INB and /INB).
7	VREF-AC	Reference Voltage Output: For AC-coupled input signals, this pin can bias the inputs IN and /IN. Connect VREF-AC directly to the VT input pin for each channel. De-couple to V_{CC} using a 0.01 µF capacitor. Maximum sink/source current is ±0.5 mA. For DC-coupled input applications, leave VREF-AC pin floating.
8, 11, 20	GND, Exposed Pad	Negative Supply: Exposed pad must be connected to a ground plane that is the same potential as the ground pins.
9	/ENA	CMOS/TTL-Compatible Enable Input: When the /ENA pin is pulled HIGH, QA is held LOW and /QA goes HIGH after the programmed delay propagates through the part. /ENA contains a 67 kΩ pull-down resistor and defaults LOW when left floating. Logic threshold level is $V_{CC}/2$
10	/ENB	CMOS/TTL-Compatible Enable Input: When the /ENB pin is pulled HIGH, QB is held LOW and /QB goes HIGH after the programmed delay propagates through the part. /ENB contains a 67 kΩ pull-down resistor and defaults LOW when left floating. Logic threshold level is $V_{CC}/2$
12, 15, 16, 19	VCC	Power Supply: Bypass each supply pin with 0.1 µF//0.01 µF low-ESR capacitors. See Table 1-1 for more details. 2.5V ±5% or 3.3V ±10%.
13, 14	/QB, QB	CML Differential Output: QB and /QB are the delayed product of INB, /INB. CML outputs are terminated at the destination with 100Ω across the pair. See the CML Output Termination section.
17, 18	/QA, QA	CML Differential Output: QA and /QA are the delayed product of INA, /INA. CML outputs are terminated at the destination with 100Ω across the pair. See the CML Output Termination section.
21	SOUT	CMOS/TTL-compatible output: This pin is used to support cascading multiple SYA89297U delay lines. Serial data is clocked into the SDATA input and is clocked out of SOUT into the next SYA89297U delay line. SOUT pin includes an internal 550Ω pull-up resistor.
22, 23	SDATA, SCLK	CMOS/TTL-compatible 3-pin serial programming control inputs: The 3-pin serial control sets each channel's IN to Q delay. DA(0:9) control channel A delay. DB(0:9) control channel B. To program the two channels, insert a 20-bit word (DA0:DA9 and DB0:DB9) into SDATA and clock in the control bits with SCLK. Maximum input frequency to SCLK is 40 MHz. Data is loaded into the serial registers on the L-H transition of SCLK. After all 20-bits are clocked in, SLOAD latches the new delay bits. These pins have internal pull-downs at the inputs. See Table 1-4 for delay values. Logic threshold level is $V_{CC}/2$. SCLK and SDATA contain a 67 kΩ pull-down resistor and default LOW when left floating.

TABLE 3-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
24	SLOAD	CMOS/TTL-compatible 3-pin serial programming control input: SLOAD controls the latches that transfer scanned data to the delay line. These latches are transparent when SLOAD is high. Data transfers from the latch to the delay line on a L-H transition of SLOAD. SLOAD has to transition H-L before new data is loaded in the scan chain. When SLOAD is high, the latches are transparent and SCLK cannot switch. Otherwise, new data will immediately transfer to the scan chain. Logic threshold level is $V_{CC}/2$. SLOAD contains a 67 kΩ pull-down resistor and defaults LOW when left floating.

3.1 Truth Tables

TABLE 3-2: INPUTS/OUTPUTS

Inputs		Outputs	
INA, INB	/INA, /INB	QA, QB	/QA, /QB
0	1	0	1
1	0	1	0

TABLE 3-3: INPUT ENABLE (LATCHES OUTPUTS)

/ENA, /ENB	Q, /Q (A, B)
1	Q = Low, /Q = HIGH
0	IN, /IN Delayed (normal operation)

4.0 TIMING DIAGRAMS

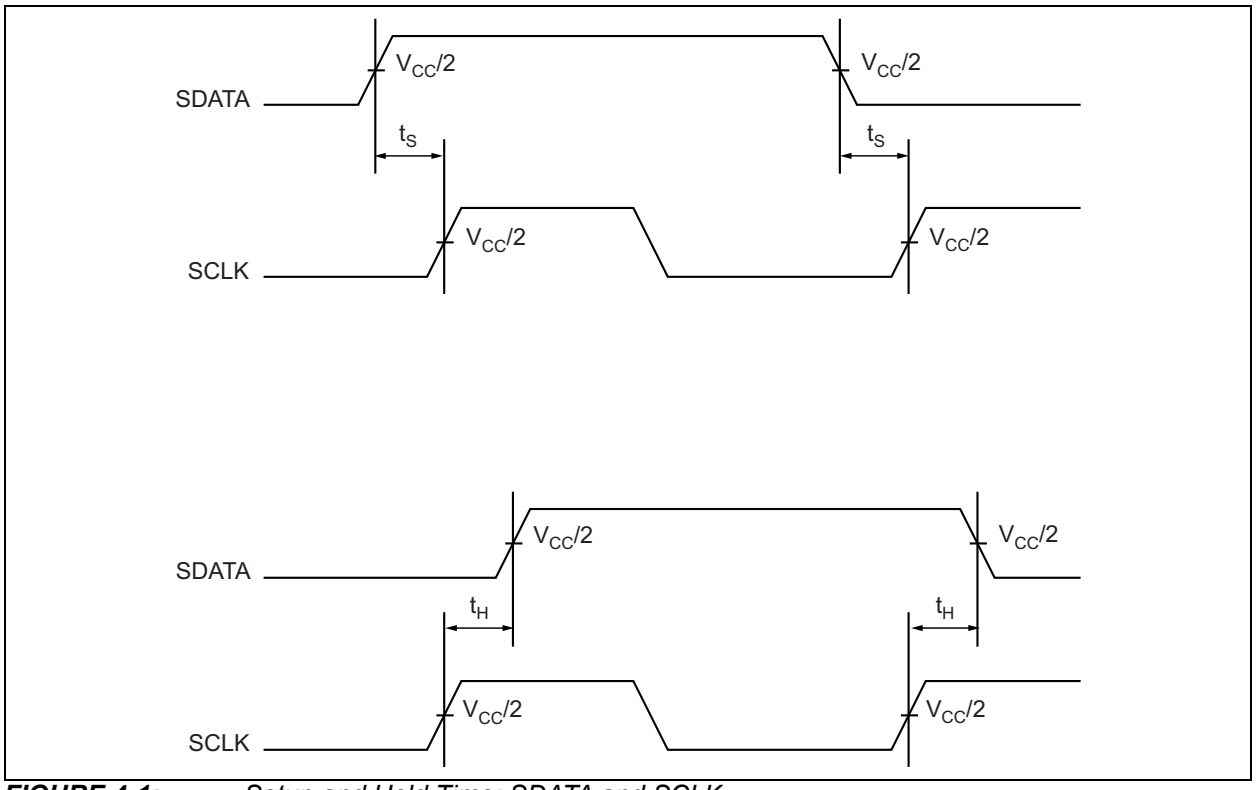


FIGURE 4-1: *Setup and Hold Time: SDATA and SCLK.*

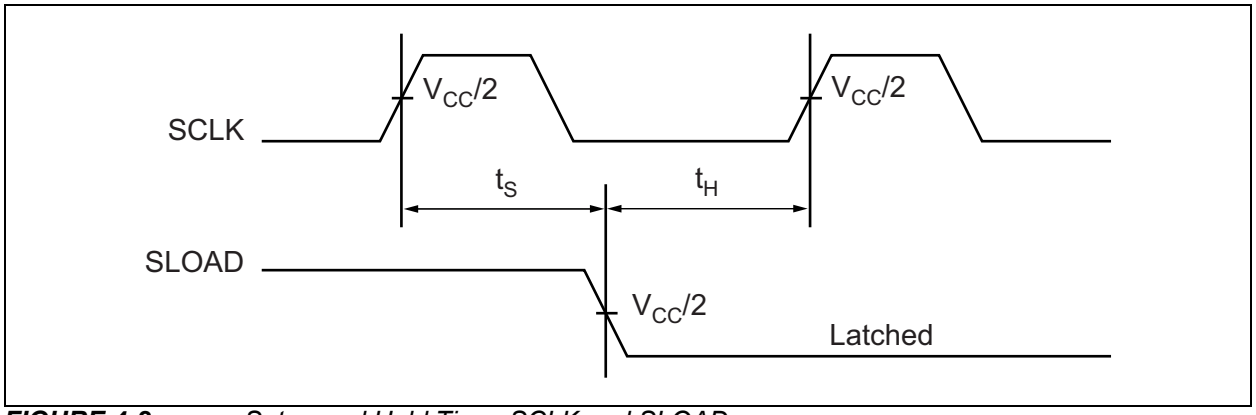


FIGURE 4-2: *Setup and Hold Time: SCLK and SLOAD.*

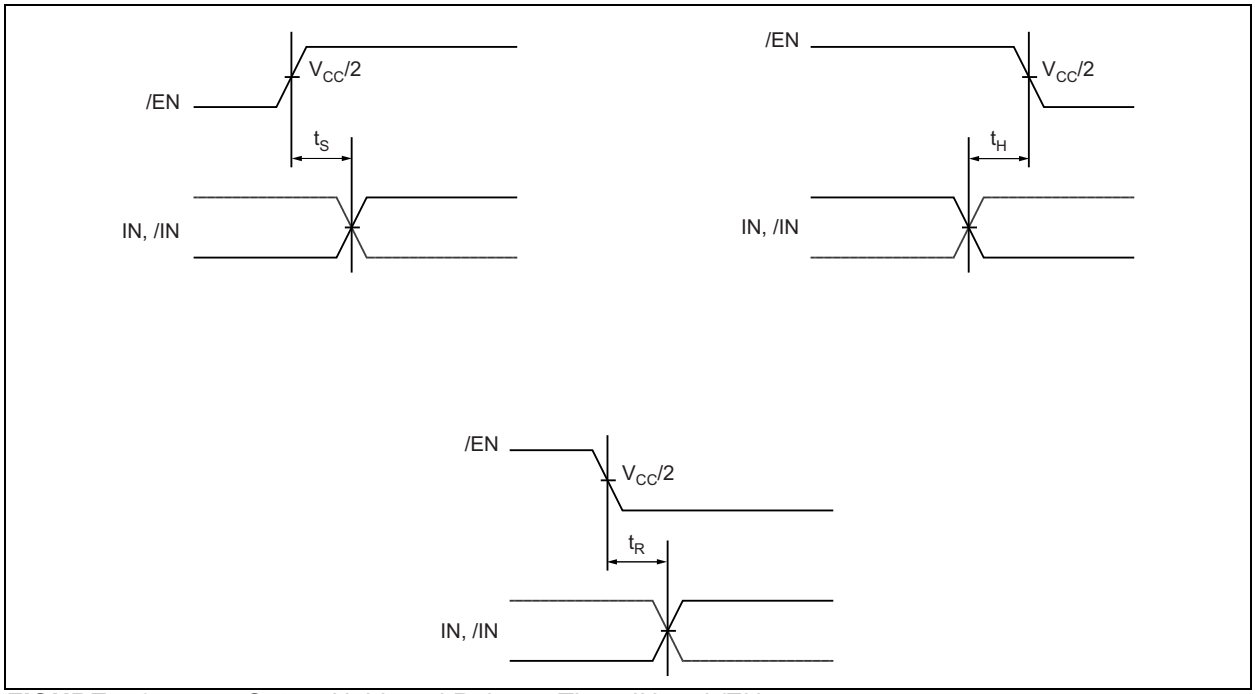


FIGURE 4-3: *Setup, Hold, and Release Time: IN and /EN.*

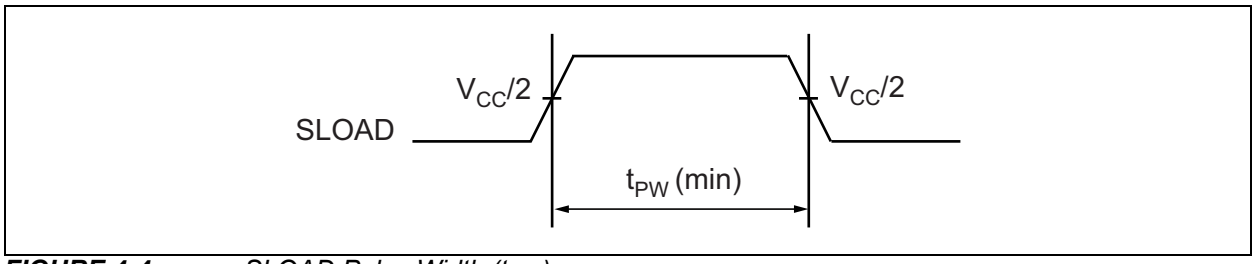


FIGURE 4-4: *SLOAD Pulse Width (t_{PW}).*

5.0 VOLTAGE SWINGS

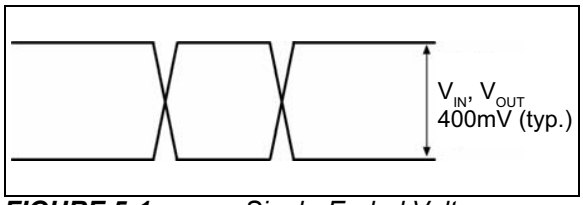


FIGURE 5-1: *Single-Ended Voltage Swing.*

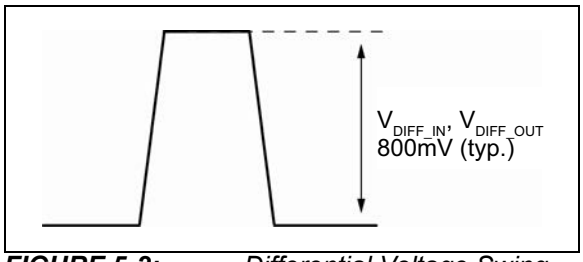


FIGURE 5-2: *Differential Voltage Swing.*

6.0 INPUT AND OUTPUT STAGES

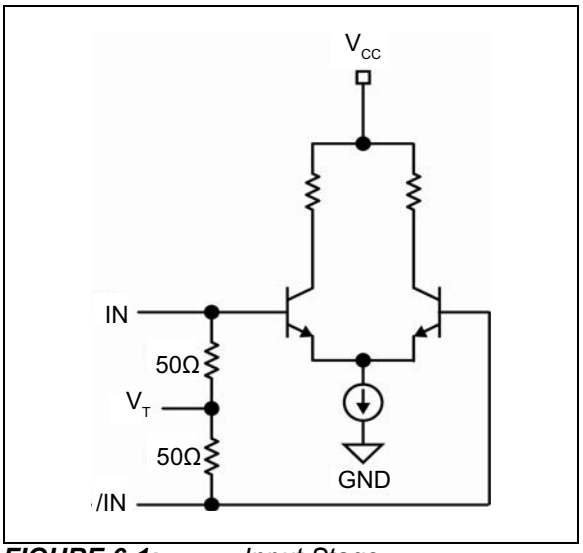


FIGURE 6-1: *Input Stage.*

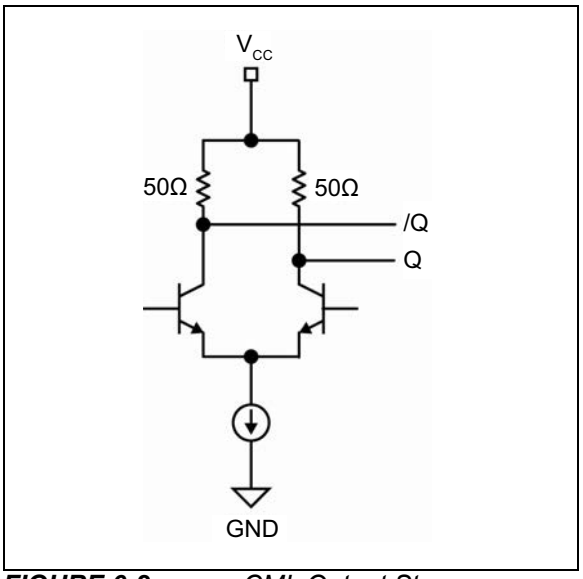


FIGURE 6-2: *CML Output Stage.*

7.0 INPUT INTERFACE APPLICATIONS

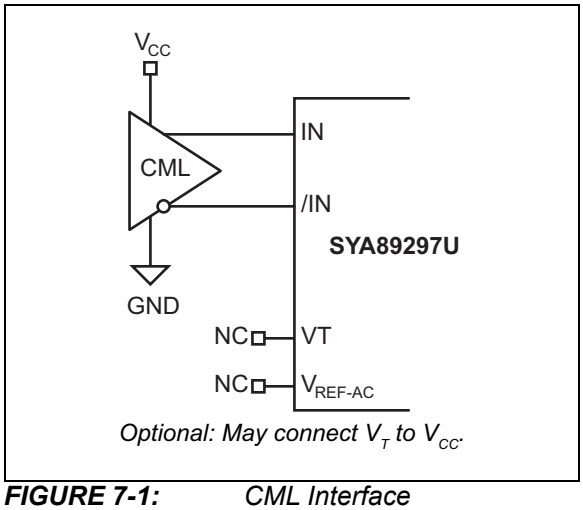


FIGURE 7-1: *CML Interface (DC-Coupled).*

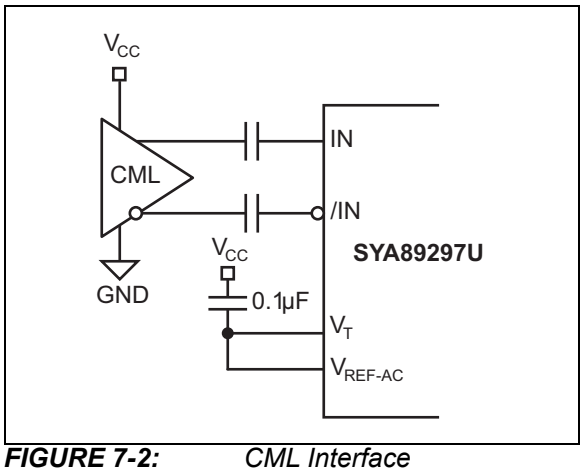


FIGURE 7-2: *CML Interface (AC-Coupled).*

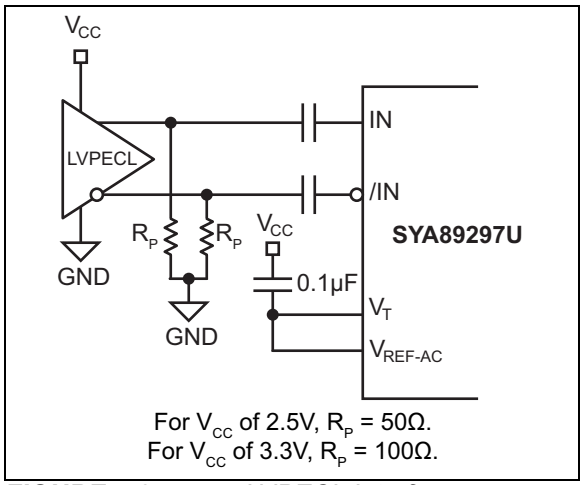


FIGURE 7-3: *LVPECL Interface (AC-Coupled).*

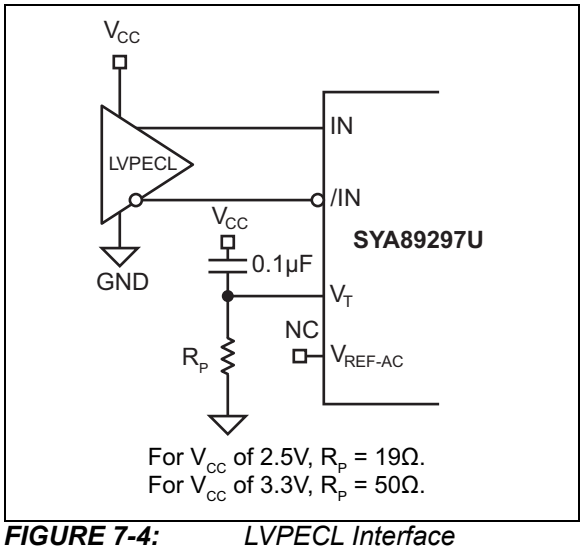


FIGURE 7-4: *LVPECL Interface (DC-Coupled).*

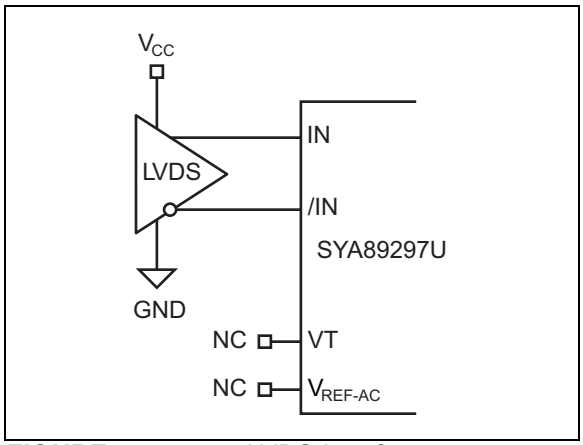


FIGURE 7-5: *LVDS Interface (DC-Coupled).*

8.0 CML OUTPUT TERMINATION

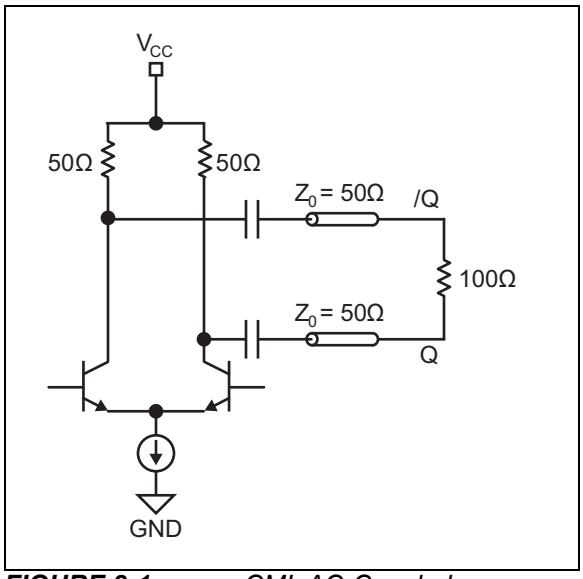


FIGURE 8-1: *CML AC-Coupled Termination – 100Ω Differential.*

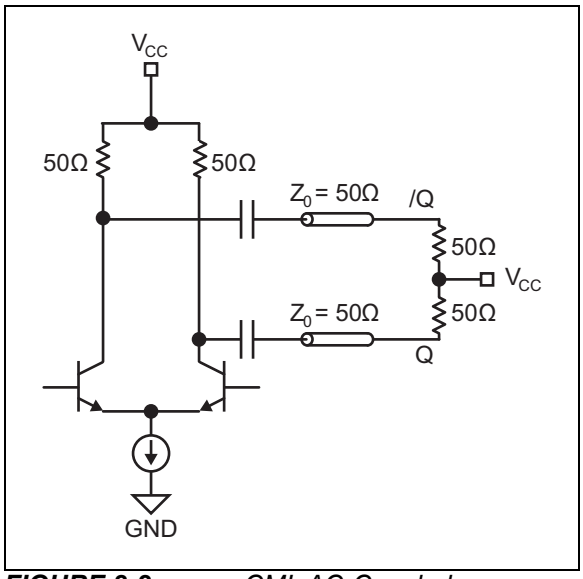


FIGURE 8-2: *CML AC-Coupled Termination – 50Ω to V_{CC}.*

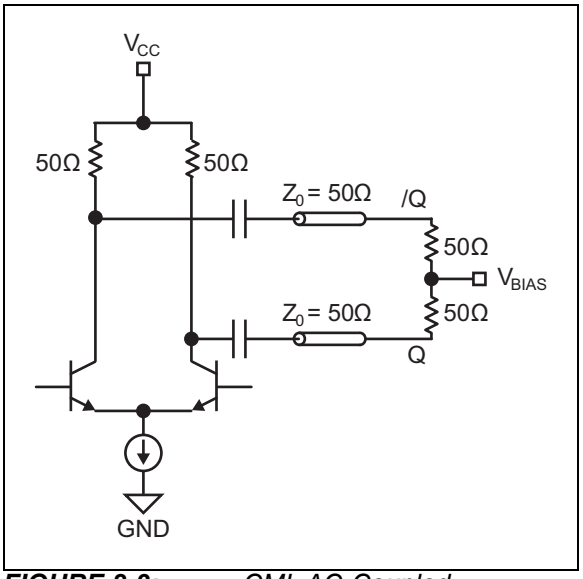


FIGURE 8-3: *CML AC-Coupled Termination – 50Ω to V_{BIAS}.*

9.0 MULTIDEVICE CASCADING

Two or more SYA89297U devices can be cascaded to extend the delay. Each additional device will add its intrinsic delay (propagation delay with all control bits low) and the programmed delay through the control lines. Below is a diagram showing how to cascade three devices, but more devices can be added following the same structure build. The cross switch (SY58040U shown here) offers the option to get the same signal with different delays available at the same time at the switch outputs.

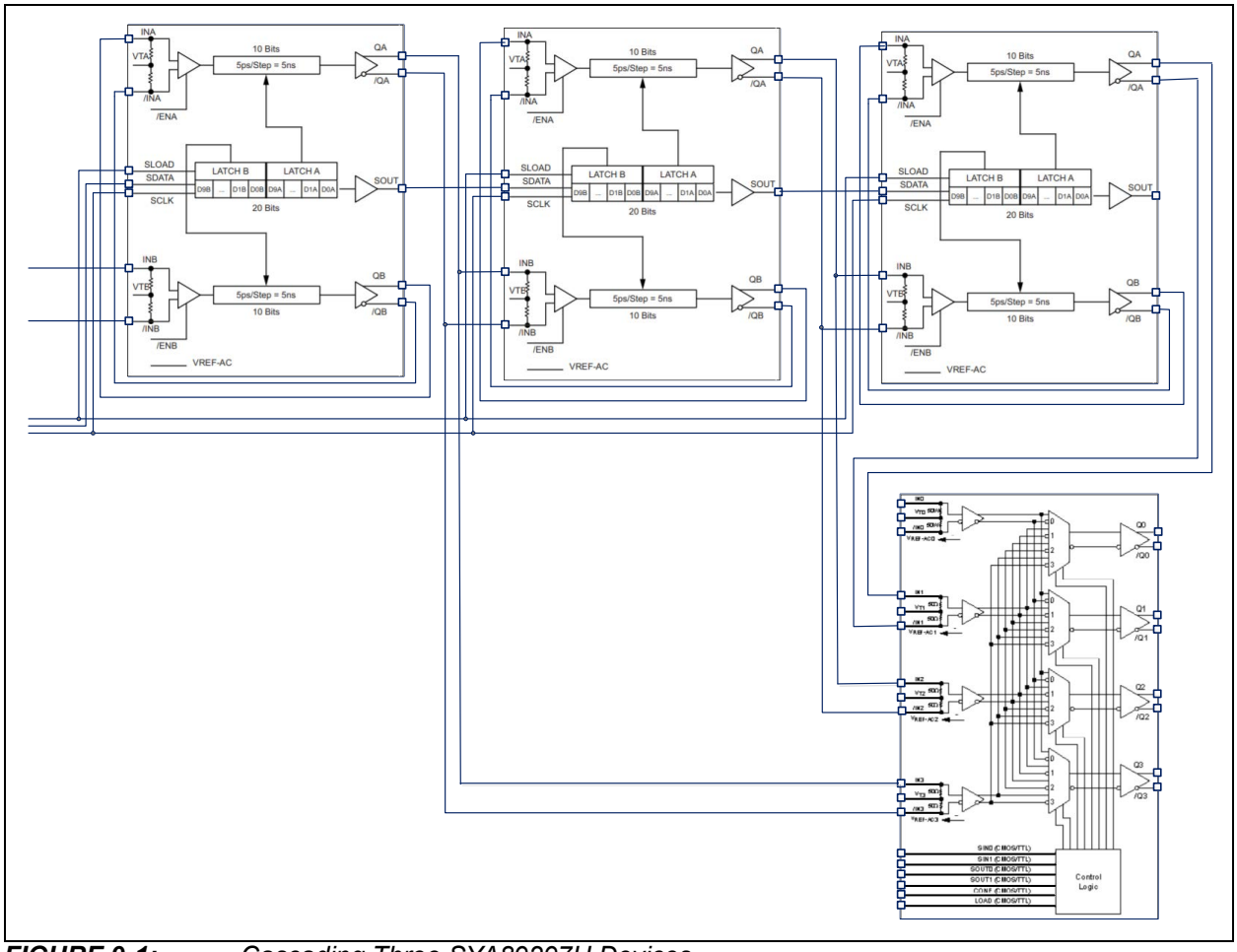
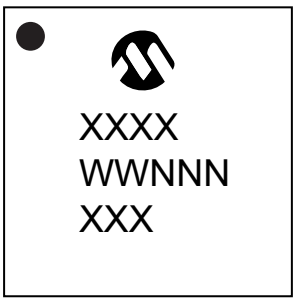


FIGURE 9-1: *Cascading Three SYA89297U Devices.*

10.0 PACKAGING INFORMATION

10.1 Package Marking Information

24-Lead WFS VQFN*



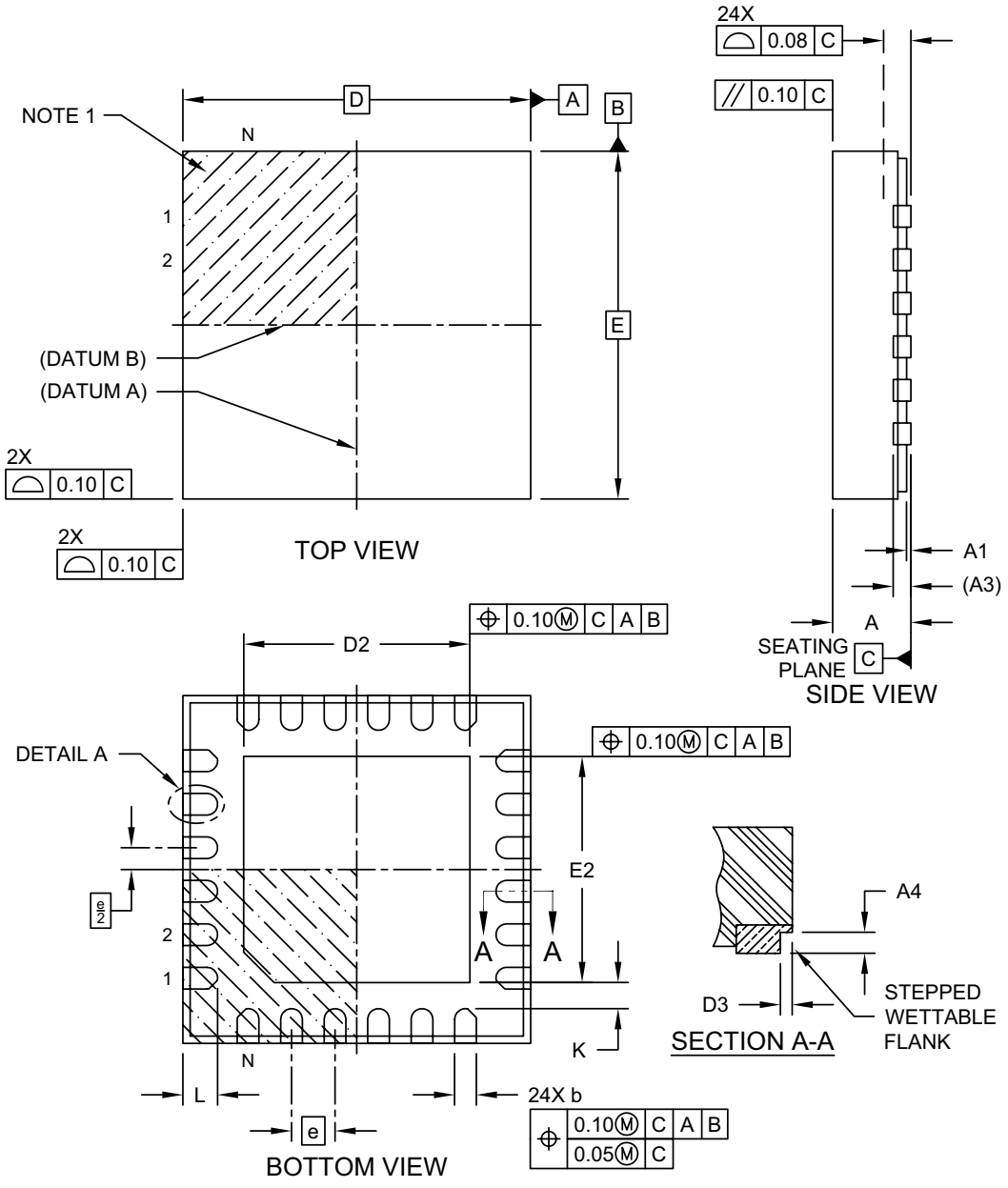
Example

Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	COO	Country of Origin
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

24-Lead 4 mm x 4 mm WFS VQFN Package Outline and Recommended Land Pattern

24-Lead Very Thin Plastic Quad Flat, No Lead Package (U3B) - 4x4 mm Body [VQFN] With 2.6mm Exposed Pad and Stepped Wettable Flanks; Atmel Legacy ZCY

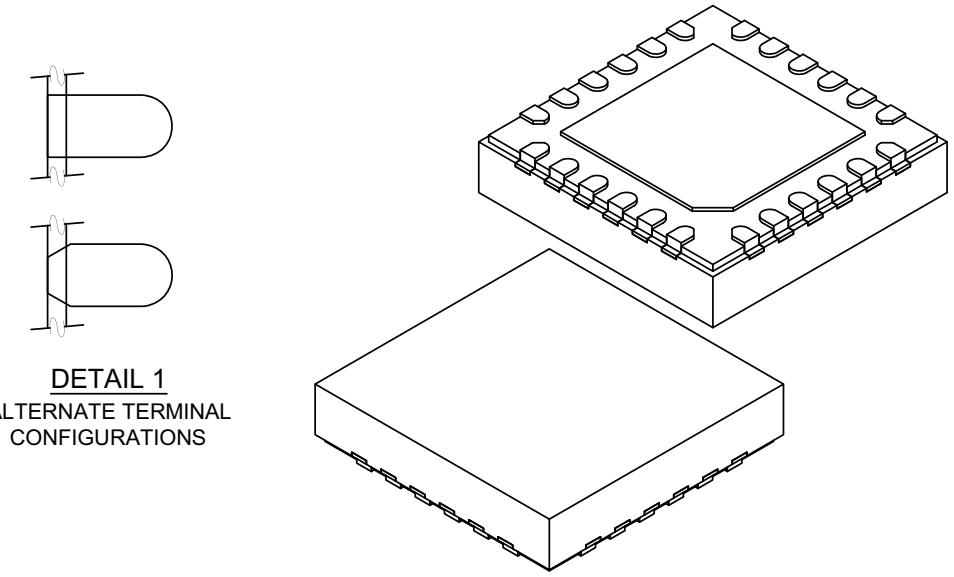
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-21483 Rev A Sheet 1 of 2

24-Lead Very Thin Plastic Quad Flat, No Lead Package (U3B) - 4x4 mm Body [VQFN] With 2.6mm Exposed Pad and Stepped Wettable Flanks; Atmel Legacy ZCY

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL 1
ALTERNATE TERMINAL CONFIGURATIONS

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		24	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.035	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.50	2.60	2.70
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.50	2.60	2.70
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-
Wettable Flank Step Length	D3	-	-	0.085
Wettable Flank Step Height	A4	0.10	-	0.19

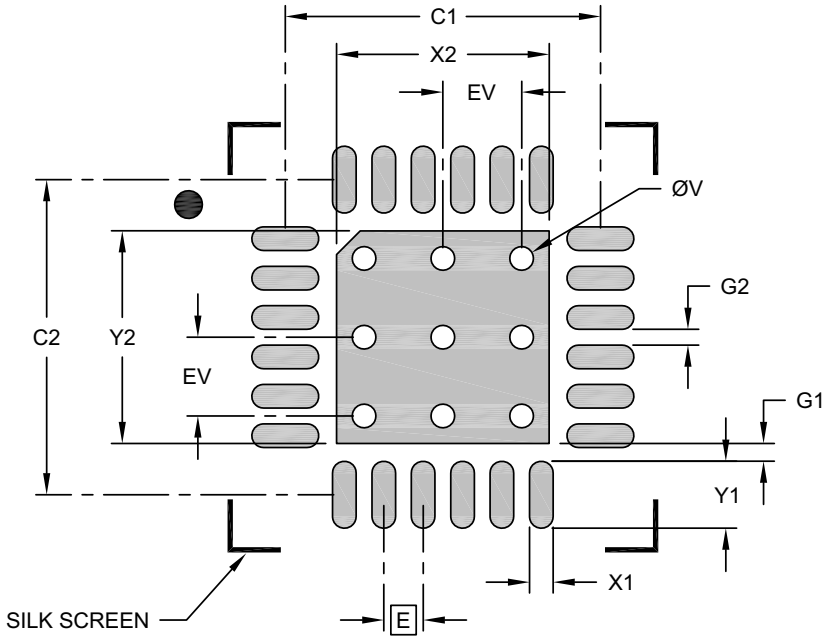
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21483 Rev A Sheet 2 of 2

24-Lead Very Thin Plastic Quad Flat, No Lead Package (U3B) - 4x4 mm Body [VQFN] With 2.6mm Exposed Pad and Stepped Wettable Flanks; Atmel Legacy ZCY

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			2.70
Optional Center Pad Length	Y2			2.70
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (X24)	X1			0.30
Contact Pad Length (X24)	Y1			0.85
Contact Pad to Center Pad (X24)	G1	0.23		
Contact Pad to Contact Pad (20)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23483 Rev A Sheet 1 of 2

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (October 2021)

- Initial release of SYA89297U as Microchip data sheet DS20006595A.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART No.	X	X	X	-XX	VXX
Device	Voltage Option	Package	Temp. Range	Media Type	Automotive Suffix

Device:	SYA89297:		2.5V/3.3V, 3.2 Gbps Precision CML Dual-Channel Programmable Delay for Automotive
Voltage Option:	U	=	2.5V/3.3V
Package:	W	=	24-Lead 4 mm x 4 mm WFS VQFN
Temperature Range:	G	=	Automotive Grade 3 –40°C to +85°C (Pb-Free NiPdAu)
Media Type:	<blank>=		75/Tube
	TR	=	1,000/Reel
Automotive Suffix:	VXX	=	Automotive suffix in which “XX” is assigned by Microchip. Default value is “AO” for standard automotive part.

Examples:

a) SYA89297UWGVAO: 2.5V/3.3V, 3.2Gbps Precision CML Dual-Channel Programmable Delay for Automotive, 24-Lead 4 mm x 4 mm WFS VQFN, Automotive Grade 3 –40°C to +85°C Temp. Range, 75/Tube, Standard Automotive

b) SYA89297UWG-TRVAO: 2.5V/3.3V, 3.2Gbps Precision CML Dual-Channel Programmable Delay for Automotive, 24-Lead 4 mm x 4 mm WFS VQFN, Automotive Grade 3 –40°C to +85°C Temp. Range, 1,000/Reel, Standard Automotive

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

For information regarding Microchip’s Quality Management Systems, please visit www.microchip.com/quality.

Trademarks

ISBN: 978-1-5224-9009-8

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
Tel: 61-2-9868-6733

China - Beijing
Tel: 86-10-8569-7000

China - Chengdu
Tel: 86-28-8665-5511

China - Chongqing
Tel: 86-23-8980-9588

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115

China - Hong Kong SAR
Tel: 852-2943-5100

China - Nanjing
Tel: 86-25-8473-2460

China - Qingdao
Tel: 86-532-8502-7355

China - Shanghai
Tel: 86-21-3326-8000

China - Shenyang
Tel: 86-24-2334-2829

China - Shenzhen
Tel: 86-755-8864-2200

China - Suzhou
Tel: 86-186-6233-1526

China - Wuhan
Tel: 86-27-5980-5300

China - Xian
Tel: 86-29-8833-7252

China - Xiamen
Tel: 86-592-2388138

China - Zhuhai
Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444

India - New Delhi
Tel: 91-11-4160-8631

India - Pune
Tel: 91-20-4121-0141

Japan - Osaka
Tel: 81-6-6152-7160

Japan - Tokyo
Tel: 81-3-6880- 3770

Korea - Daegu
Tel: 82-53-744-4301

Korea - Seoul
Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906

Malaysia - Penang
Tel: 60-4-227-8870

Philippines - Manila
Tel: 63-2-634-9065

Singapore
Tel: 65-6334-8870

Taiwan - Hsin Chu
Tel: 886-3-577-8366

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600

Thailand - Bangkok
Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4485-5910
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-72400

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7288-4388

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820