



# SCSI Bus Expander Family

**SYM53C120 SCSI Bus Expander**

**SYM20101 Extender Board**

**SYM20102 Converter Board**

Supports Single-Ended(SE)-to-SE or

(SE)-to-Differential Modes

**PRELIMINARY**

**Data Manual and User's Guide**

**Version 3.0**



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## Preface

This manual provides description and electrical characteristics of the SYM53C120 SCSI Bus Expander chip which supports single-ended to single-end SCSI bus expansion (Extender) or single-ended to differential SCSI bus conversion (Converter). This manual also provides a description of and how to install the SYM20101 Extender board and the SYM20102 Converter board. Both boards use the SYM53C120 SCSI Bus Expander chip.

This manual assumes some prior knowledge of current and proposed SCSI standards. For background information, please contact:

### ANSI

11 West 42nd Street  
New York, NY 10036  
(212) 642-4900  
Ask for document number X3.131-1994 (SCSI-2) (SCSI-3)

### Global Engineering Documents

15 Inverness Way East  
Englewood, CO 80112  
(800) 854-7179 or (303) 792-2181 (outside U.S.)  
Ask for document number X3.131-1994 (SCSI-2) or X3.253 (*SCSI-3 Parallel Interface*)

### ENDL Publications

14426 Black Walnut Court  
Saratoga, CA 95070  
(408) 867-6642  
Document names: *SCSI Bench Reference*, *SCSI Encyclopedia*

### Prentice Hall

Englewood Cliffs, NJ 07632  
(201) 767-5937  
Ask for document number ISBN 0-13-796855-8, *SCSI: Understanding the Small Computer System Interface*

### Symbios Logic Electronic Bulletin Board

(719) 573-3562

### SCSI Electronic Bulletin Board

(719) 574-0424

### Symbios Logic World Wide Web

<http://www.symbios.com>  
(See EPI (Enhanced Parallel Interface) Specification for expander configurations)

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## Revision Record

| Page No.            | Date  | Version | Remarks  |
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| All                 | 10/96 | 1.0     | Preliminary Data Manual  |
| All                 | 11/96 | 2.0     | Complete Data Manual   |
| All                 | 1/97  | 2.1     | Changed DIFF_MODE to DIFF_MODE/<br>and modified SCSI Interface Timings   |
| All                 | 2/97  | 2.2     | Title changed to SYM53C120 SCSI Bus<br>Expander. DC Characteristics, TolerANT<br>Technology Electrical Characteristics and<br>Differential Wiring Diagram changed. |
| Manual Title        | 6/97  | 3.0     | This manual now includes the SYM2010x<br>boards  |
| 4-1, 2, 3, 4, and 8 |       |         | Timing changes in Chapter 4  |
| All of Chapter 5    |       |         | Added Chapter 5, SYM2010x SCSI Boards  |

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# Chapter 1 Introduction

## General Description

The SYM53C120 SCSI Bus Expander is a single chip solution allowing the extension of device connectivity and/or cable length limits of the SCSI bus. The SYM53C120 operates as a SCSI bus expander when multiple single-ended to single-ended cables are connected together while being electrically isolated from each other. The SYM53C120 also operates as a SCSI bus converter when single-ended to differential cables are connected together while being electrically isolated from each other.

The SYM53C120 operates in two modes: single-ended to single-ended (Extender Mode) or single-ended to differential (Converter Mode). For applications requiring SE to Low Voltage Differential (LVD), use the SYM53C141 Bus Expander. Table 1-1 shows all modes of operation.

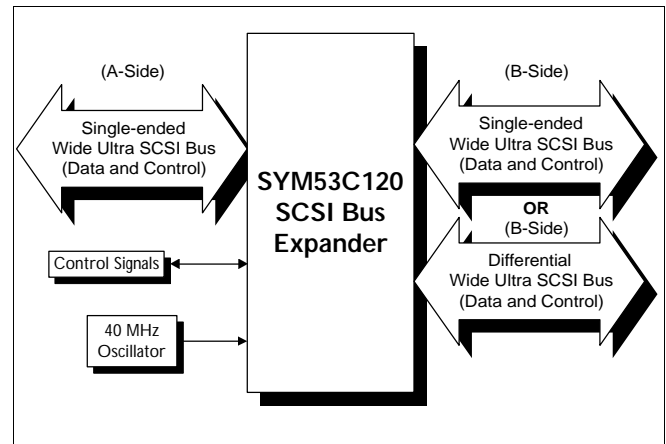
**Table 1-1: Mode of Operation**

| Symbios Product | Extender | Converter |
|-----------------|----------|-----------|
| SYM53C120       | SE to SE | SE to HVD |
| SYM5353C141     | SE to SE | SE to LVD |

In both SCSI Bus Extender and Converter modes, cable segments are electrically isolated from each other. This feature maintains the signal integrity of each cable segment. For bus isolation applications, the SYM53C120 is ideally suited for the SYM53C875 Ultra SCSI controller.

The SYM53C120 provides additional control capability through the pin level electrical isolation mode. This feature permits logical disconnection of both the A-side bus and the B-side bus without disrupting SCSI transfers currently in progress. For example, devices on the logically disconnected B-side can be swapped out while the A-side bus remains active.

The SYM53C120 is based upon bus expander technology resulting in some signal filtering and re-timing to maintain signal skew budgets. In addition, the SYM53C120 has no programmable registers, therefore, it does not require any software.



**Figure 1-1: SYM53C120 SCSI Bus Device**

### Features

- Accepts any asynchronous or synchronous data transfer rates up to the 40 MB/s rate of Wide Ultra SCSI
- Targets and initiators can connect to either the SCSI A- or SCSI B-side of the SYM53C120
- Does not consume a SCSI ID
- Can cascade up to three SYM53C120s in series
- Requires 40 MHz input clock
- Supports two modes of operation
  - Single-ended to Single-ended Mode
  - Single-ended to Differential Mode (with external transceivers)
- Connects two wide and/or narrow SCSI buses

- Extends Ultra SCSI cable lengths in certain applications
- Extends total number of connected Ultra SCSI devices supported
- Supports TolerANT® active negation technology
- Complete support for SCSI-1, -2, and -3
- Completely independent of software
- Pin level SCSI bus disable mode
- Packaged in a 128 PQFP

The SYM53C120 SCSI Bus Expander works with Symbios Logic's extensive SYM53C7xx and SYM53C8xx family of SCSI products. It also works with other industry SCSI controllers, disk drives, and SCSI peripherals. Advantages of the SYM53C120 are that it does not require any software or consume a SCSI ID. This allows for easy integration and maximum bus utilization. Adding the SYM53C120 to a SCSI bus environment creates a low risk solution for applications requiring scalable device connectivity and SCSI bus electrical isolation.

Figure 1-1 illustrates the connectivity of the SYM53C120 SCSI Bus Expander device. A SCSI single-ended(SE) bus connects directly to the SCSI A-side. The interface signals are SCSI bus compatible driver and receiver signals with no internal termination. The SCSI B-side has the single-ended capable driver and receiver and also provides the individual driver controls

for external differential transceivers.

The SYM53C120 provides additional control capability through the pin level SCSI bus disable mode. This feature allows logical disconnection of both the A-side bus and B-side bus without disrupting transfers currently in progress. For example, this feature allows electrical disconnection of devices on the B-side to be swapped out while the A-side bus remains active.

As with all of Symbios Logic's SYM53C7xx and SYM53C8xx SCSI products, the SYM53C120 features TolerANT® technology. The benefits of TolerANT include increased immunity to noise, better performance due to balanced duty cycles, and improved SCSI transfer rates.

## Application Examples

The following examples are typical applications for the SYM53C120 SCSI Bus Expander. Many other configurations are possible and are only limited by the imagination of the system architect.

### Scalable Device Connectivity

Figure 1-2 illustrates how to use the SYM53C120 to increase the number of devices to 15 on a 3 meter Ultra SCSI bus cable.

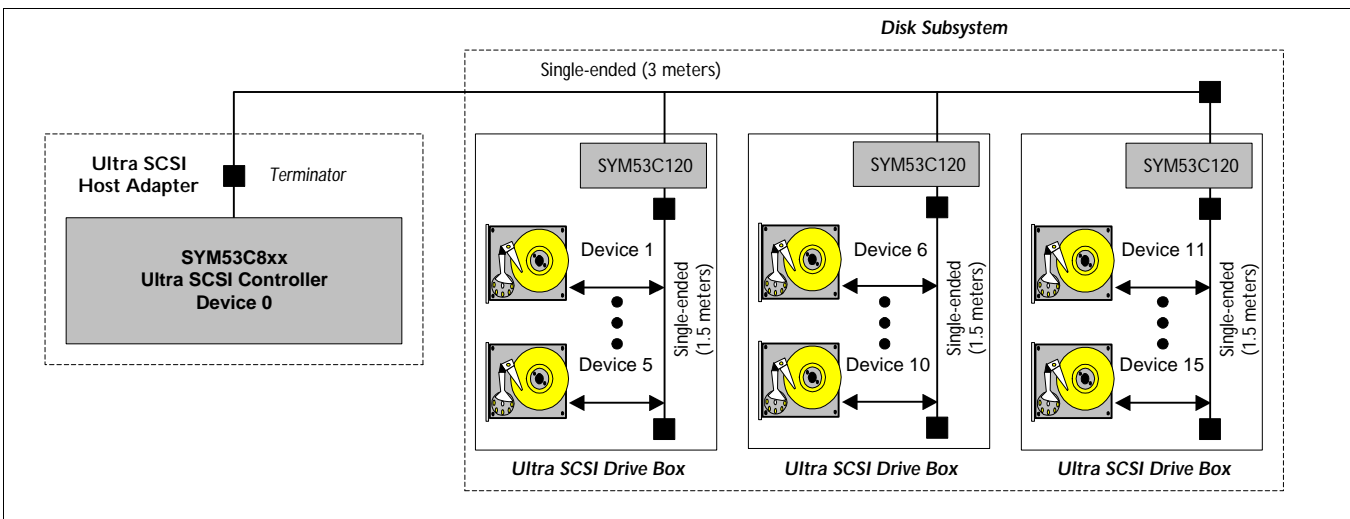


Figure 1-2: SCSI Extender Application (Single-Ended to Single-Ended Mode of Operation)

Figure 1-3 illustrates both single-ended to single-ended, and single-ended to differential modes of the

SYM53C120 to create a redundant remote storage configuration.

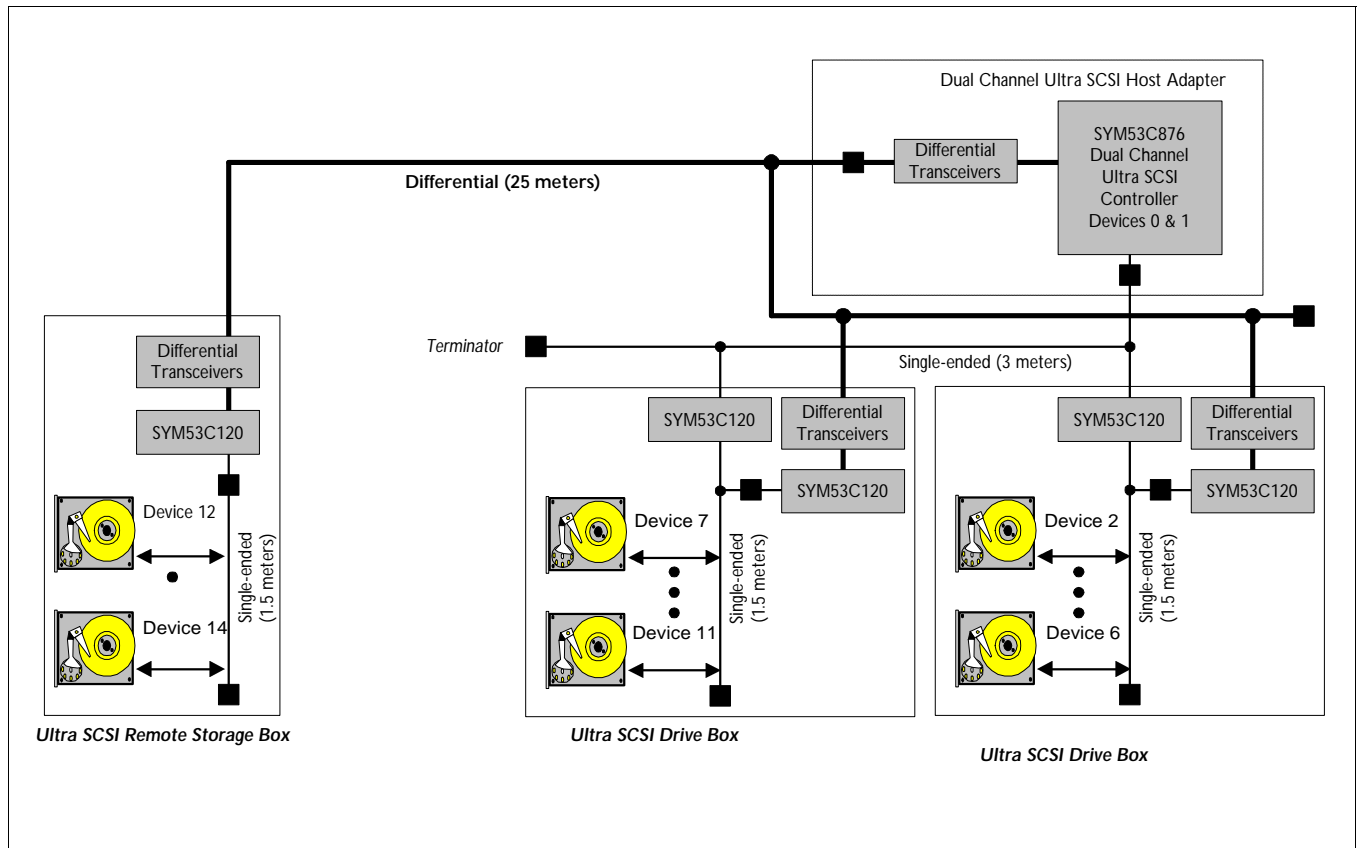


Figure 1-3: SCSI Extender or Converter Application (Single-Ended to Differential Mode of Operation)

## SCSI Bus Electrical Isolation

Figure 1-4 illustrates how to use the SYM53C120 to electrically isolate an external SCSI bus from an internal SCSI bus. This configuration ensures externally attached peripherals will not affect the operation of internal peripherals.

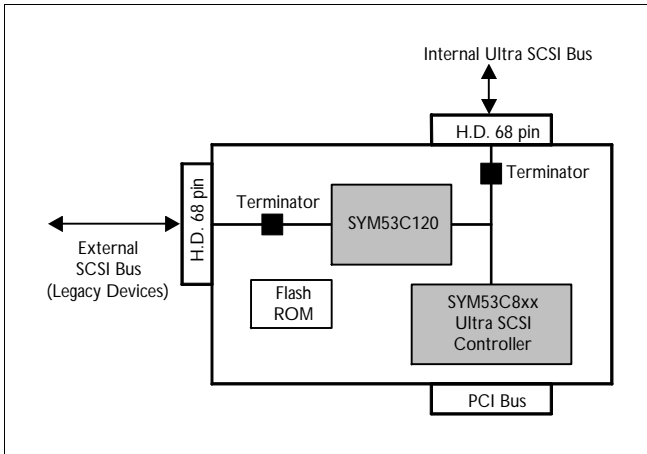


Figure 1-4: SCSI Bus Electrical Isolation

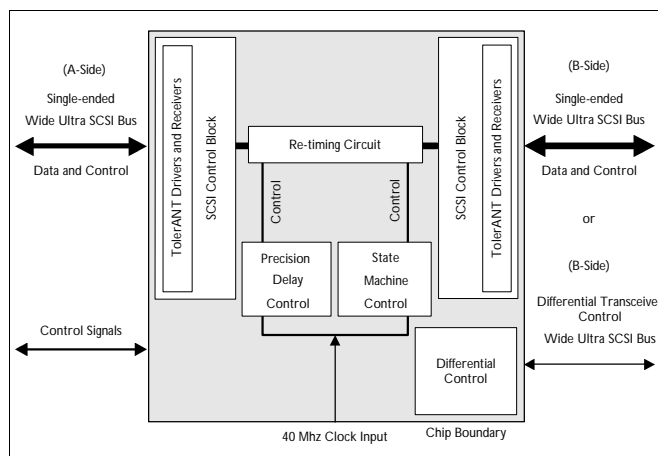
## Chapter 2

# Functional Description

## Interface Signal Descriptions

The SYM53C120 has no programmable registers; therefore, no software requirements. SCSI control signals control all SYM53C120 functions. This chapter describes all signals, their groupings and functions. Following is a diagram of the SYM53C120 device divided into the following blocks:

- SCSI A-Side and B-Side Single-Ended Control Blocks that contain TolerANT® Drivers and Receivers
- Re-timing Circuit
- Precision Delay Control
- State Machine Control
- Differential Control



**Figure 2-1: SYM53C120 Block Diagram**

In its simplest form, the SYM53C120 passes data and parity from a source bus to a load bus. The side asserting, de-asserting or releasing the SCSI signals is the source side. The simplest model is that the SYM53C120 is just pieces of wire that allow corresponding SCSI signals to flow from side to side. In reality, the

SYM53C120 needs to know which side is driving the signals so it can enable the proper drivers to pass the signals along. In addition, the SYM53C120 does some signal re-timing to maintain the signal skew budget from source bus to load bus as if the source was a local bus member.

### SCSI A-Side and B-Side Single-Ended Control Blocks

In the single-ended to single-ended mode, the SCSI A-side pins are connected internally to the corresponding SCSI B-side pins, forming bi-directional connections to the SCSI bus.

The SCSI A-side and B-side single-ended control blocks connect to both targets and initiators and accept any asynchronous or synchronous data transfer rates up to the 40 MB/s rate of Wide Ultra SCSI. TolerANT technology is part of the SCSI A-side and B-side single-ended control blocks.

### TolerANT® Drivers and Receivers

The SYM53C120 features TolerANT technology, which includes active negation on the SCSI drivers and input signal filtering on the SCSI receivers. Active negation causes the SCSI Request, Acknowledge, Data, and Parity signals to be actively driven high rather than passively pulled up by terminators.

TolerANT receiver technology improves data integrity in unreliable cabling environments, where other devices would be subject to data corruption. TolerANT receivers filter the SCSI bus signals to eliminate unwanted transitions, without the long signal delay associated with RC-type input filters. This improved driver and receiver technology helps eliminate double clocking of data, the single biggest reliability issue with SCSI operations.

The benefits of TolerANT include increased immunity to noise on the de-asserting signal edge, better performance due to balanced duty cycles, and improved SCSI transfer rates. In addition, TolerANT SCSI devices prevent glitches on the SCSI bus at power-up or power-down, so other devices on the bus are also protected from data corruption.

### Re-timing Logic

The SCSI signals, as they propagate from one side of the SYM53C120 to the other side, are processed by logic that re-times the bus signals as needed to guarantee or improve required SCSI timings. This logic is governed by the state machine controls that keep track of SCSI phases, the location of initiator and target devices, and various timing functions. In addition, this logic contains numerous precision delay elements that are periodically calibrated by the precision delay control block in order to guarantee specified timings such as output pulse widths, setup and hold times, and other timings.

### Precision Delay Control

The precision delay control block provides calibration information to the precision delay elements in the re-timing logic block in order to maintain precise timings as signals propagate through the device. As the SYM53C120's operating conditions, such as voltage and temperature, vary over time, the precision delay control block will periodically update the delay settings in the re-timing logic to maintain constant and precise control over bus timings.

### State Machine Control

The state machine controls keep track of the SCSI bus phase protocol and other internal operating conditions. This block provides signals to the re-timing logic that identifies how to properly handle SCSI bus signal re-timing and protocol, based on observed bus conditions.

### Differential Control

In the SCSI converter (single-ended to differential) mode, the SCSI A-side pins are connected internally to the corresponding SCSI B-side differential pins, forming bi-directional connections to the SCSI bus.

### Signal Descriptions

Figure 2-2 illustrates the signal groupings of the SYM53C120. A description the of signals follows but for specific signal timings, see *AC Characteristics* in Chapter 4, *Electrical Characteristics*.

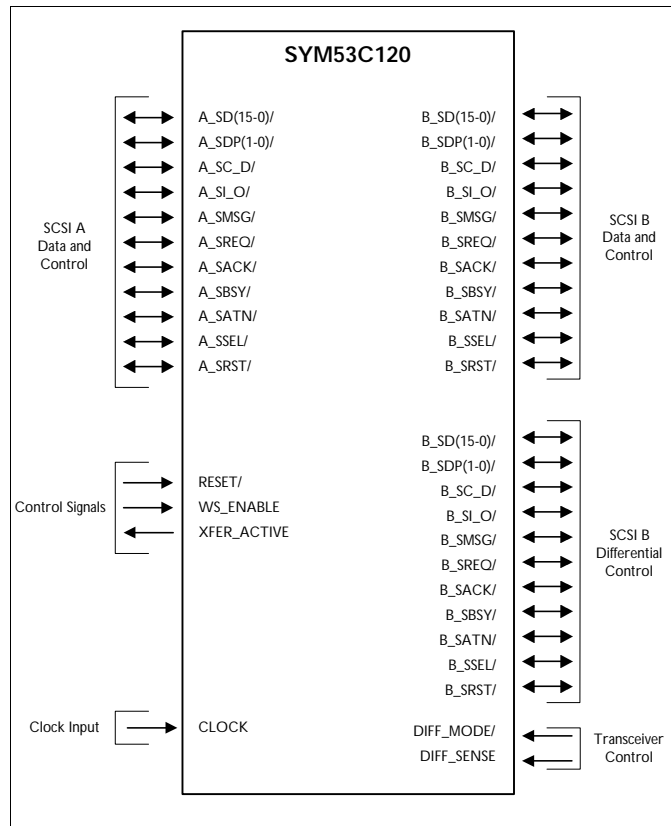


Figure 2-2: SYM53C120 Signal Grouping

### Data and Parity

The signals named A\_SD/(15-0, P0, P1) are the data and parity signals from the A-side and B\_SD/(15-0, P0, P1) are the data and parity signals from the B-side of the SYM53C120. These signals are sent and received from the SYM53C120 via SCSI compatible driver and

receiver logic designed into the SYM53C120 interface. This logic provides the necessary drive, sense thresholds, and input hysteresis to function correctly in a SCSI bus environment as defined in ANSI Standard for SCSI-1, SCSI-2 and SCSI-3.

The SYM53C120 receives data and parity signals and passes them from the source bus to the load bus and provides any necessary edge shifting to guarantee the skew budget for the load bus. Either side of the SYM53C120 can be the source bus or the load bus. The side asserting, de-asserting or releasing the SCSI signals is the source side. The following steps are a part of the SYM53C120 data path.

- Asserted data is accepted from the receiver logic as soon as it is received. Once the clock signal has been received, data is gated from the receiver latch.
- The path is next tested to ensure data was not driven by the SYM53C120. Valid data needs to be generated by another node on the source bus to be passed through the SYM53C120 to the load bus.
- The data is then leading edge filtered. The assertion edge is held for a specified time to prevent any signal bounce. The duration is then controlled by the input signal.
- The next stage is a latch that samples the signal. This provides a stable data window for the load bus.
- The final stage develops pull-up and pull-down controls for the SCSI I/O logic, including tri-state controls for the pull-up.
- A parallel function ensures that bus (transmission line) recovery is ensured for a specified time after the last signal de-assertion on each signal line.

### Busy (BSY) Control

A\_SBSY/ and B\_SBSY/ signals are propagated from the source bus to the load bus. These signals go through the following processing.

- The path is tested to be sure the data was not driven by the SYM53C120. Because valid data needs to be generated by another node on the source bus to be passed through the SYM53C120 to the load bus.
- The data is then leading edge filtered. The assertion

edge is held for a specified time to prevent any signal bounce. The duration is then controlled by the input signal.

- The next stage has two modes. One mode simply passes data through. The other mode behaves like a large filter. The mode is selected by the current state in the SYM53C120 state machine which tracks SCSI phases. The large filter mode is used where the Busy (BSY) and Select (SEL) sources may switch from side to side. This output is then fed to the output driver which is a pull-down open collector only.
- A parallel function ensures that bus (transmission line) recovery is ensured for a specified time after the last signal de-assertion on each signal line.

### Request (REQ)/Acknowledge (ACK) Control

A\_SACK/, B\_SACK/, A\_SREQ/ and B\_SREQ/ are clock and control signals. Their signal paths contain controls to guarantee minimum pulse width, filter edges, and does some re-timing when used as data transfer clocks. Each signal, REQ and ACK, has paths from A to B and B to A. The received signal goes through the following processing steps before being sent to the opposite bus.

- The asserted input signal is sensed and forwarded to the next stage if the direction control permits it. The direction controls are developed from state machines that are driven by the sequence of bus control signals.
- The signal must then pass the test of not being generated by the SYM53C120.
- In the A to B bus direction, the next stage is a leading edge filter. This ensures that the output will not switch during the specified hold time after the leading edge. The duration of the input signal determines the duration of the output after the hold time. In the B to A direction, the circuit guarantees a minimum pulse.
- The next stage passes the signal if it is not a data clock. If REQ or ACK is a data clock, it delays the leading edge to improve data output setup times. The duration is again controlled by the input signal.
- The following stage is a trailing edge signal filter.

When the signal de-asserts, the filter will not permit any signal bounce. The output signal de-asserts at the first de-asserted edge of the input signal.

- The last stage develops pull-up and pull-down signals with drive and tri-state control.
- A parallel function ensures that bus (transmission line) recovery is ensured for a specified time after the last signal de-assertion on each signal line.

### Reset (RST) Control

A\_SRST/ and B\_SRST/ are also passed from the source to the load bus. These reset signals are processed in the following steps.

- The input signal is blocked if it is already being driven by the SYM53C120.
- The next stage is a leading edge filter. This ensures that the output will not switch for a specified time after the leading edge. The duration of the input signal then determines the duration of the output.
- A parallel function ensures that bus (transmission line) recovery is ensured for a specified time after the last signal de-assertion on each signal line.

### Control/Data (C/D), Input/Output (I/O), Message (MSG) and Attention (ATN) Controls

A\_SCD/, A\_SIO/, A\_SMSG/, A\_SATN/, B\_SCD/, B\_SIO/, B\_SMSG/ and B\_SATN/ are control signals that have the following processing steps.

- The input signal is blocked if it is being driven by the SYM53C120.
- The next stage is a leading edge filter. This ensures that the output will not switch for a specified time after the leading edge. The duration of the input signal then determines the duration of the output.
- The final stage develops pull-up and pull-down controls for the SCSI I/O logic, including tri-state controls for the pull-up.
- A parallel function ensures that bus (transmission line) recovery is ensured for a specified time after the last signal de-assertion on each signal line.

### Select (SEL) Control

A\_SSEL/ and B\_SSEL/ are control signals used during bus arbitration and selection. Whichever bus asserts SEL propagates it to the other side. If both signals are asserted at the same time, the A-side receives SEL and sends it to the B-side. The signal goes through the following processing steps.

- The input signal is blocked if it is being driven by the SYM53C120.
- The next stage is a leading edge filter. This ensures that the output will not switch for a specified time after the leading edge. The duration of the input signal then determines the duration of the output.
- A parallel function ensures that bus (transmission line) recovery is ensured for a specified time after the last signal de-assertion on each signal line.

### Differential Direction Controls

B\_SDIR(15-0, P0, P1), B\_BSYDIR, B\_SELDIR, B\_CD\_DIR, B\_IO\_DIR, B\_MSGDIR, B\_REQDIR, B\_ACKDIR, B\_ATNDIR and B\_RSTDIR are all differential direction control signals on the B-side of the SYM53C120. When the B-side is used in single-ended mode, these signals are not used and should be left unconnected. When the B-side is used in differential mode, these signals are used to control the direction of each external differential transceiver on the B-side interface.

Every B-side signal requires a driver enable control to allow for all the possible signal conditions including SCAM support. The data bits require individual controls for the selection phase of SCSI bus protocol.



**Table 2-1:** Direction Control Signals (B\_SDIR(15-0, P0, P1), B\_BSYDIR, B\_SELDIR, B\_CD\_DIR, B\_IO\_DIR, B\_MSGDIR, B\_REQDIR, B\_ACKDIR, B\_ATNDIR and B\_RSTDIR) Polarities

| Signal Level | State       | Effect                             |
|--------------|-------------|------------------------------------|
| High = 1     | Asserted    | Drive SYM53C120 signals onto Bus B |
| Low = 0      | De-asserted | Input Bus B signals to SYM53C120   |

### Differential Mode (DIFF\_MODE/)

This input informs the SYM53C120 that external differential transceivers are used in this particular application. In addition, this input causes internal logic to adjust for external differential control.

Table 2-2: DIFF\_MODE/ Control Signal Polarity

| Signal Level | State       | Effect   |
|--------------|-------------|--|
| Low = 0      | Asserted    | Differential Signals and Controls are enabled from the SYM53C120 |
| High = 1     | De-asserted | SYM53C120 Bus B drivers function in single-ended mode            |

### Differential Sense (DIFF\_SENSE)

This input signal determines if a single-ended device is placed on the differential bus. If a single-ended source is detected, the differential B-side is disabled and no differential B-side signals are driven. This mechanism prevents potential damage to the differential transceivers.

Table 2-3: DIFF\_SENSE Control Signal Polarity

| Signal Level | State       | Effect                                       |
|--------------|-------------|--|
| High = 1     | Asserted    | The B-side drivers and receivers are enabled |
| Low = 0      | De-asserted | B-side Drivers and Receivers are disabled    |

### Clock (CLOCK)

This is the 40 MHz oscillator input to the SYM53C120. This is the clock source for protocol control state machines and timing generation logic. This clock is not used in any bus signal transfer paths.

### Chip Reset (RESET/)

This general chip reset is intended to force all the internal elements of the SYM53C120 into a known state. This will bring all state machines to an idle state and force all controls to a passive state. The minimum RESET input asserted pulse width is 100 nanoseconds.

The SYM53C120 also contains an internal Power On Reset (POR) function that is wire ORed with the chip reset pin which eliminates the need for an external chip reset.

Table 2-4: RESET/ Control Signal Polarity

| Signal Level | State       | Effect   |
|--------------|-------------|--|
| Low = 0      | Asserted    | Reset is forced to all internal SYM53C120 elements |
| High = 1     | De-asserted | SYM53C120 is not in a forced reset state           |

**Warm Start Enable and Transfer Active  
 (WS\_ENABLE and XFER\_ACTIVE)**

These two pins provide additional control capability for the SYM53C120. They allow both the SCSI A-side bus and the SCSI B-side bus to be logically disconnected. The XFER\_ACTIVE output changes state only with the detection of a SCSI bus free state; this guarantees that transfers currently in progress will not be disrupted by the assertion or de-assertion of the WS\_ENABLE pin.

Assertion or de-assertion of the WS\_ENABLE pin may not be effective immediately since it may take several milliseconds for a bus free state to be detected and then indicated by a change in state of the XFER\_ACTIVE output signal.

Table 2-5: WS\_ENABLE Signal Polarity

| Signal Level | State       | Effect  |
|--------------|-------------|---|
| High = 1     | Asserted    | The SYM53C120 will start transfers through the device once the next SCSI bus free is detected until de-assertion. |
| Low = 0      | De-asserted | The SYM53C120 will stop transfers through the device when the next SCSI bus free is detected.                     |

Table 2-6: XFER\_ACTIVE Signal Polarity

| Signal Level | State       | Effect   |
|--------------|-------------|--|
| High = 1     | Asserted    | Normal operation, transfers through the SYM53C120 are enabled  |
| Low = 0      | De-asserted | The SYM53C120 has detected a bus free phase while WS_ENABLE is low disabling transfers through the device. |

# Chapter 3 Signal Descriptions

The SYM53C120 is packaged in a 128 pin Plastic Quad Flat Pack (PQFP). Detailed descriptions follow, grouped by function. The decoupling capacitor arrangement shown below is recommended to maximize the benefits of the internal split ground system. Capacitor values should be between 0.01 and 0.1 uF.

## SYM53C120 Pin Diagram

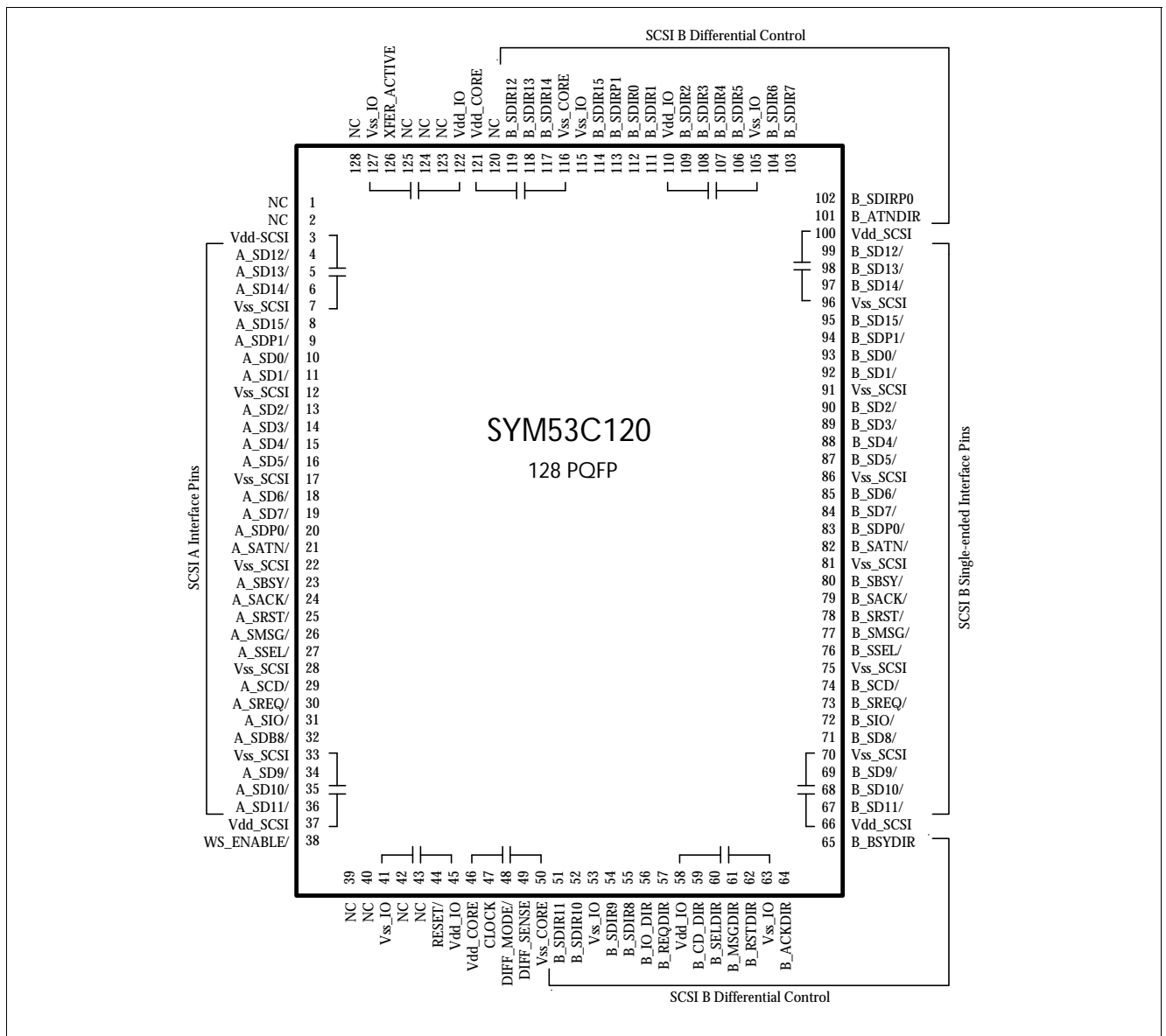
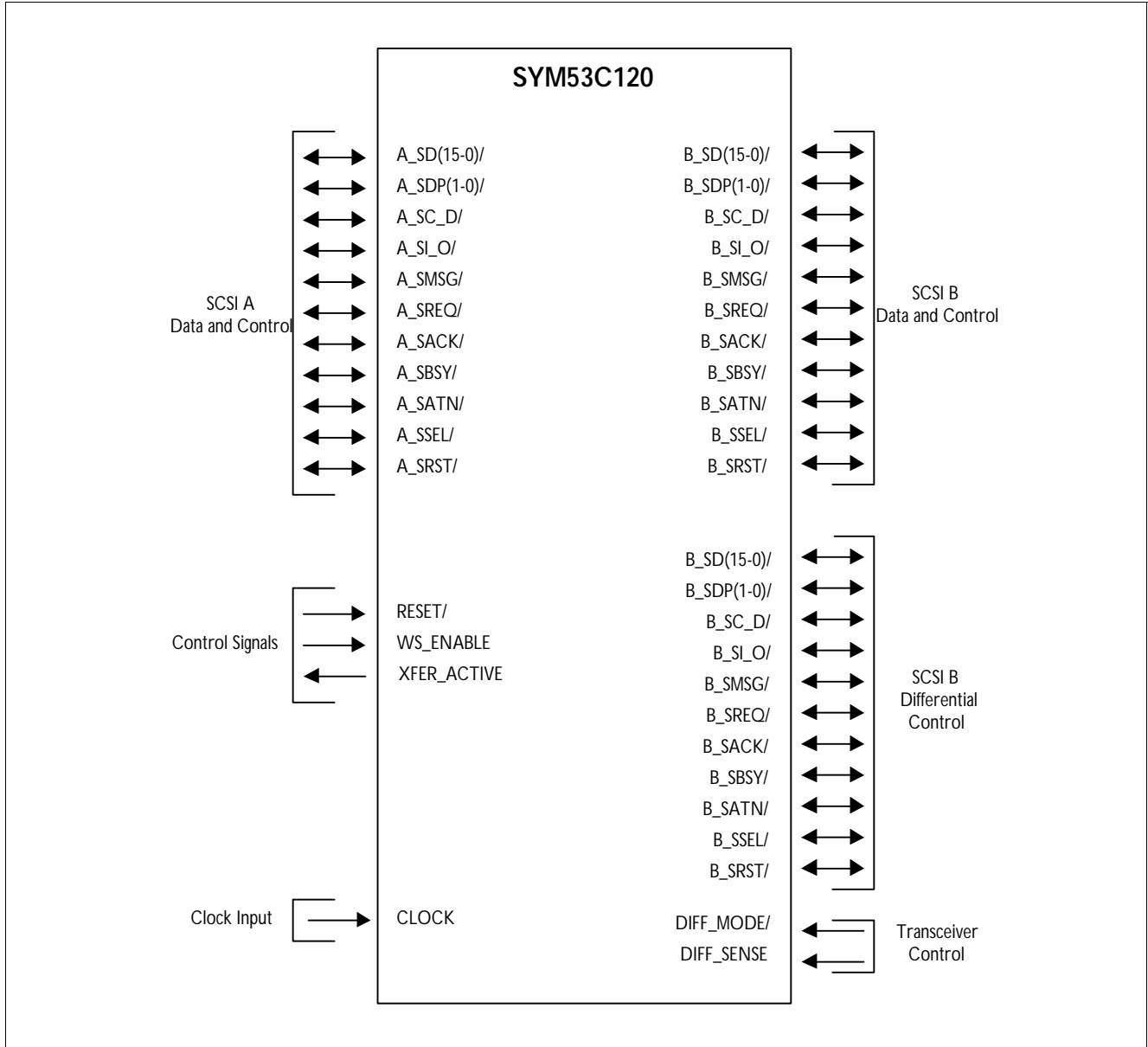


Figure 3-1: SYM53C120 Pin Diagram

# SYM53C120 Signal Grouping



**Figure 3-2: SYM53C120 Functional Signal Grouping**

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## SCSI A Interface Pins

**Table 3-1: SCSI A Signal Description**

| SCSI A      | Pin  | Type | Strength | Description  |
|-------------|--|------|----------|--|
| A_SD/(15-0) | 8, 6, 5, 4, 36,<br>35, 34, 32,<br>19, 18, 16,<br>15, 14, 13,<br>11, 10 | I/O  | 48 mA    | Data (16-bit SCSI bus)                                     |
| A_SDP/(1-0) | 9, 20  | I/O  | 48 mA    | Data parity bits   |
| A_SCD/      | 29   | I/O  | 48 mA    | Phase line, command/data                                   |
| A_SIO/      | 31   | I/O  | 48 mA    | Phase line, input/output                                   |
| A_SMSG/     | 26   | I/O  | 48 mA    | Phase line, message  |
| A_SREQ/     | 30   | I/O  | 48 mA    | Data handshake signal from target device                   |
| A_SACK/     | 24   | I/O  | 48 mA    | Data handshake signal from initiator device                |
| A_SBSY/     | 23   | I/O  | 48 mA    | Bus arbitration signal, busy                               |
| A_SATN/     | 21   | I/O  | 48 mA    | Attention, the initiator is requesting a message out phase |
| A_SSEL/     | 27   | I/O  | 48 mA    | Bus arbitration signal, select device                      |
| A_SRST/     | 25   | I/O  | 48 mA    | Bus Reset  |

---

## SCSI B Single-ended Interface Pins

**Table 3-2: SCSI B Signal Description**

| SCSI B      | Pin   | Type | Strength | Description  |
|-------------|---|------|----------|--|
| B_SD/(15-0) | 95, 97, 98,<br>99, 67, 68,<br>69, 71, 84,<br>85, 87, 88,<br>89, 90, 92,<br>93 | I/O  | 48 mA    | Data (16-bit SCSI bus)                                     |
| B_SDP/(1-0) | 94, 83  | I/O  | 48 mA    | Data parity bits   |
| B_SCD/      | 74  | I/O  | 48 mA    | Phase line, command/data                                   |
| B_SIO/      | 72  | I/O  | 48 mA    | Phase line, input/output                                   |
| B_SMSG/     | 77  | I/O  | 48 mA    | Phase line, message  |
| B_SREQ/     | 73  | I/O  | 48 mA    | Data handshake signal from target device                   |
| B_SACK/     | 79  | I/O  | 48 mA    | Data handshake signal from initiator device                |
| B_SBSY/     | 80  | I/O  | 48 mA    | Bus arbitration signal, busy                               |
| B_SATN/     | 82  | I/O  | 48 mA    | Attention, the initiator is requesting a message out phase |
| B_SSEL/     | 76  | I/O  | 48 mA    | Bus arbitration signal, select device                      |
| B_SRST/     | 78  | I/O  | 48 mA    | Bus Reset  |

## SCSI B Differential Interface Pins

**Table 3-3: SCSI B Differential Signal Description**

| SCSI B Differential | Pin  | Type | Strength | Description                                      |
|---------------------|--|------|----------|--|
| B_SDIR(15-0)        | 114, 117, 118,<br>119, 51, 52, 54,<br>55, 103, 104,<br>106, 107, 108,<br>109, 111, 112 | O    | 4 mA     | Driver direction control for SCSI data line      |
| B_SDIRP(1-0)        | 113, 102   | O    | 4 mA     | Driver direction control for SCSI parity signals |
| B_CD_DIR            | 59   | O    | 4 mA     | Driver direction control for CD/                 |
| B_IO_DIR            | 56   | O    | 4 mA     | Driver direction control for IO/                 |
| B_MSGDIR            | 61   | O    | 4 mA     | Driver direction control for MSG/                |
| B_REQDIR            | 57   | O    | 4 mA     | Driver direction control for REQ/                |
| B_ACKDIR            | 64   | O    | 4 mA     | Driver direction control for ACK/                |
| B_BSYDIR            | 65   | O    | 4 mA     | Driver direction control for BSY/                |
| B_ATNDIR            | 101  | O    | 4 mA     | Driver direction control for ATN/                |
| B_SELDIR            | 60   | O    | 4 mA     | Driver direction control for SEL/                |
| B_RSTDIR            | 62   | O    | 4 mA     | Driver direction control for RST/                |

## Control Interface Pins

**Table 3-4: Chip Control Signal Description**

| Control     | Pin | Type | Strength | Description  |
|-------------|-----|------|----------|--|
| RESET/      | 44  | I    |          | Master reset, active low                             |
| WS_ENABLE   | 38  | I    |          | Enable/disable SCSI transfers through SYM53C120      |
| XFER_ACTIVE | 126 | O    | 16 mA    | Transfers through the SYM53C120 are enabled/disabled |

**Table 3-5: SCSI Control Signal Description**

| SCSI Control | Pin | Type | Description   |
|--------------|-----|------|---|
| CLOCK        | 47  | I    | 40 MHz input clock  |
| DIFF_MODE/   | 48  | I    | SCSI B-side bus mode control  |
| DIFF_SENSE   | 49  | I    | The DIFF_SENSE pin detects the presence of a single-ended device on a differential system. This pin should be tied low during single-ended operation and pulled high during differential operation. |

**Table 3-6: Power and Ground Signal Description**

| Power and Ground | Pin   | Type | Description                             |
|------------------|---|------|---|
| VDD-SCSI         | 3, 37, 66, 100                                | I/O  | Power supplies to the SCSI bus I/O pins |
| VSS-SCSI         | 7, 12, 17, 22, 28, 33, 70, 75, 81, 86, 91, 96 | I/O  | Power supplies to the SCSI bus I/O pins |
| VSS_IO           | 41, 53, 63, 105, 115, 127                     | I/O  | Power supplies to the I/O pins          |
| VDD_IO           | 45, 58, 110, 122                              | I/O  | Power supplies to the I/O pins          |
| VDD_CORE         | 46, 121                                       | CORE | Power supplies to the CORE logic        |
| VSS_CORE         | 50, 116                                       | CORE | Power supplies to the CORE logic        |

**Table 3-7: No Connect Pins**

| No Connects      | Pin                           | Type | Description                                 |
|------------------|-------------------------------|------|---|
| NC               | 39, 40, 42, 43, 120, 123, 124 |      | No external connection required.            |
| Require pullups  | 1, 2, 128                     |      | Requires a pullup.                          |
| Require pulldown | 125                           |      | Requires a pulldown with a 1K ohm resistor. |



## Chapter 4

# Electrical Characteristics

## DC Characteristics

**Table 4-1: Absolute Maximum Stress Ratings**

| Symbol     | Parameter               | Min            | Max            | Unit | Test Conditions                |
|------------|-------------------------|----------------|----------------|------|--------------------------------|
| $T_{STG}$  | Storage temperature     | -55            | 150            | °C   | -                              |
| $V_{DD}$   | Supply voltage          | -0.5           | 7.0            | V    | -                              |
| $V_{IN}$   | Input Voltage           | $V_{SS} - 0.5$ | $V_{DD} + 0.5$ | V    | -                              |
| $I_{LP}^*$ | Latch-up current        | $\pm 150$      | -              | mA   | -                              |
| ESD**      | Electrostatic discharge | -              | 2K             | V    | MIL-STD 883C,<br>Method 3015.7 |

*Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the Operating Conditions section of the manual is not implied.*

\*  $-2V < V_{PIN} < 8V$

\*\* SCSI pins only

**Table 4-2: Operating Conditions**

| Symbol        | Parameter                                       | Min  | Max  | Unit | Test Conditions |
|---------------|---|------|------|------|-----------------|
| $V_{DD}$      | Supply voltage                                  | 4.75 | 5.25 | V    | -               |
| $I_{DD}$      | Supply current (dynamic)                        | -    | 80   | mA   | -               |
|               | Supply current (static)                         | -    | 1    | mA   | -               |
| $T_A$         | Operating free air                              | 0    | 70   | °C   | -               |
| $\theta_{JA}$ | Thermal resistance<br>(junction to ambient air) | -    | 41.3 | °C/W | -               |

*Conditions that exceed the operating limits may cause the device to function incorrectly*

**Table 4-3: SCSI Signals - A\_SD(15-0)/, A\_SDP(1-0)/, A\_SREQ/, A\_SACK/, B\_SD(15-0)/, B\_SDP(1-0)/, B\_SREQ/, B\_SACK/**

| Symbol            | Parameter           | Min                   | Max                   | Unit | Test Conditions |
|-------------------|---------------------|-----------------------|-----------------------|------|-----------------|
| V <sub>IH</sub>   | Input high voltage  | 1.9                   | V <sub>DD</sub> + 0.5 | V    | -               |
| V <sub>IL</sub>   | Input low voltage   | V <sub>SS</sub> - 0.5 | 1.0                   | V    | -               |
| V <sub>OH</sub> * | Output high voltage | 2.4                   | 3.5                   | V    | 2.5 mA          |
| V <sub>OL</sub>   | Output low voltage  | V <sub>SS</sub>       | 0.4                   | V    | 48 mA           |
| I <sub>OZ</sub>   | Tri-state leakage   | -10                   | 10                    | μA   | -               |

\*TolerANT active negation enabled

**Table 4-4: SCSI Signals - A\_SMSG, A\_SI\_O/, A\_SC\_D/, A\_SATN/, A\_SBSY/, A\_SSEL/, A\_SRST/, B\_SMSG, B\_SI\_O/, B\_SC\_D/, B\_SATN/, B\_SBSY/, B\_SSEL/, B\_SRST/**

| Symbol          | Parameter                         | Min                   | Max                   | Unit | Test Conditions |
|-----------------|-----------------------------------|-----------------------|-----------------------|------|-----------------|
| V <sub>IH</sub> | Input high voltage                | 1.9                   | V <sub>DD</sub> + 0.5 | V    | -               |
| V <sub>IL</sub> | Input low voltage                 | V <sub>SS</sub> - 0.5 | 1.0                   | V    | -               |
| V <sub>OL</sub> | Output low voltage                | V <sub>SS</sub>       | 0.5                   | V    | 48 mA           |
| I <sub>OZ</sub> | Tri-state leakage<br>(SRST/ only) | -10<br>-500           | 10<br>-50             | μA   | -               |

**Table 4-5: Input Signals - CLOCK, DIFF\_SENSE, DIFF\_MODE/\*, WS\_ENABLE\***

| Symbol          | Parameter          | Min                   | Max                   | Unit | Test Conditions |
|-----------------|--------------------|-----------------------|-----------------------|------|-----------------|
| V <sub>IH</sub> | Input high voltage | 2.0                   | V <sub>DD</sub> + 0.5 | V    | -               |
| V <sub>IL</sub> | Input low voltage  | V <sub>SS</sub> - 0.5 | 0.8                   | V    | -               |
| I <sub>IN</sub> | Input leakage      | -10*                  | 10                    | μA   | -               |

\* The minimum (I<sub>IN</sub>) Input leakage for DIFF\_MODE/ and WS\_ENABLE is -100 μA.

**Table 4-6: Capacitance**

| Symbol   | Parameter                       | Min | Max | Unit | Test Conditions |
|----------|---------------------------------|-----|-----|------|-----------------|
| $C_I$    | Input capacitance of input pads | -   | 7   | pF   | -               |
| $C_{IO}$ | Input capacitance of I/O pads   | -   | 10  | pF   | -               |

**Table 4-7: Differential Signals - B\_SDIR(15-0), B\_SDIRP0, B\_SDIRP1, B\_CD\_DIR, B\_IO\_DIR, B\_MSGDIR, B\_REQDIR, B\_B\_ACKDIR, B\_BSYDIR, B\_SELDIR, B\_SELDIR, B\_RSTDIR**

| Symbol   | Parameter           | Min      | Max      | Unit    | Test Conditions |
|----------|---------------------|----------|----------|---------|-----------------|
| $V_{OH}$ | Output high voltage | 2.4      | $V_{DD}$ | V       | -4 mA           |
| $V_{OL}$ | Output low voltage  | $V_{SS}$ | 0.4      | V       | 4 mA            |
| $I_{OZ}$ | Tri-state leakage   | -10      | 10       | $\mu A$ | -               |

**Table 4-8: Control Signals - RESET/**

| Symbol   | Parameter          | Min            | Max            | Unit    | Test Conditions |
|----------|--------------------|----------------|----------------|---------|-----------------|
| $V_{IH}$ | Input high voltage | 3.5            | $V_{DD} + 0.5$ | V       | -               |
| $V_{IL}$ | Input low voltage  | $V_{SS} - 0.5$ | 1.5            | V       | -               |
| $I_{OZ}$ | Tristate leakage   | -10            | 10             | $\mu A$ | -               |

**Table 4-9: Control Signals - XFER\_ACTIVE**

| Symbol   | Parameter           | Min      | Max      | Unit    | Test Conditions |
|----------|---------------------|----------|----------|---------|-----------------|
| $V_{OH}$ | Output high voltage | 2.4      | $V_{DD}$ | V       | 16 mA           |
| $V_{OL}$ | Output low voltage  | $V_{SS}$ | 0.4      | V       | 16 mA           |
| $I_{OZ}$ | Tri-state leakage   | -10      | 10       | $\mu A$ | -               |

## TolerANT Technology Electrical Characteristics

**Table 4-10: TolerANT Technology Electrical Characteristics**

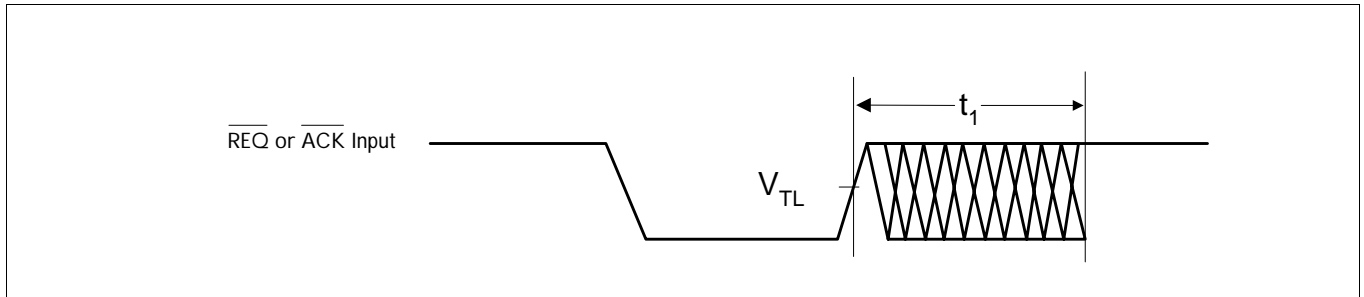
| Symbol          | Parameter                         | Min   | Max   | Units      | Test Conditions   |
|-----------------|-----------------------------------|-------|-------|------------|---|
| $V_{OH}^1$      | Output high voltage               | 2.5   | 3.5   | V          | $I_{OH} = 2.5$ mA   |
| $V_{OL}$        | Output low voltage                | 0.1   | 0.5   | V          | $I_{OL} = 48$ mA  |
| $V_{IH}$        | Input high voltage                | 1.9   | 7.0   | V          | -   |
| $V_{IL}$        | Input low voltage                 | -0.5  | 1.0   | V          | Referenced to $V_{SS}$  |
| $V_{IK}$        | Input clamp voltage               | -0.66 | -0.77 | V          | $V_{DD} = 4.75$ ;<br>$I_I = -20$ mA                             |
| $V_{TH}$        | Threshold, high to low            | 1.1   | 1.3   | V          | -   |
| $V_{TL}$        | Threshold, low to high            | 1.5   | 1.7   | V          | -   |
| $V_{TH}-V_{TL}$ | Hysteresis                        | 200   | 400   | mV         | -   |
| $I_{OH}^1$      | Output high current               | 2.5   | 24    | mA         | $V_{OH} = 2.5$ V  |
| $I_{OL}$        | Output low current                | 100   | 200   | mA         | $V_{OL} = 0.5$ V  |
| $I_{OSH}^1$     | Short-circuit output high current | -     | 625   | mA         | Output driving low, pin shorted to $V_{DD}$ supply <sup>2</sup> |
| $I_{OSL}$       | Short-circuit output low current  | -     | 95    | mA         | Output driving high, pin shorted to $V_{SS}$ supply             |
| $I_{LH}$        | Input high leakage                | -     | 10    | $\mu$ A    | $-0.5 < V_{DD} < 5.25$<br>$V_{PIN} = 2.7$ V                     |
| $I_{LL}$        | Input low leakage                 | -     | -10   | $\mu$ A    | $-0.5 < V_{DD} < 5.25$<br>$V_{PIN} = 0.5$ V                     |
| $R_I$           | Input resistance                  | 20    | -     | M $\Omega$ | SCSI pins <sup>3</sup>  |
| $C_P$           | Capacitance per pin               | -     | 10    | pF         | PQFP  |
| $t_R^1$         | Rise time, 10% to 90%             | 9.7   | 18.5  | ns         | Figure 7-1  |
| $t_F$           | Fall time, 90% to 10%             | 5.2   | 14.7  | ns         | Figure 7-1  |
| $dV_H/dt$       | Slew rate, low to high            | 0.15  | 0.49  | V/ns       | Figure 7-1  |
| $dV_L/dt$       | Slew rate, high to low            | 0.19  | 0.67  | V/ns       | Figure 7-1  |
| ESD             | Electrostatic discharge           | 2     | -     | KV         | MIL-STD-883C;<br>3015-7   |
|                 | Latch-up                          | 100   | -     | mA         | -   |
|                 | Filter delay                      | 10    | 15    | ns         | Figure 4-1  |

Note: These values are guaranteed by periodic characterization; they are not 100% tested on every device.

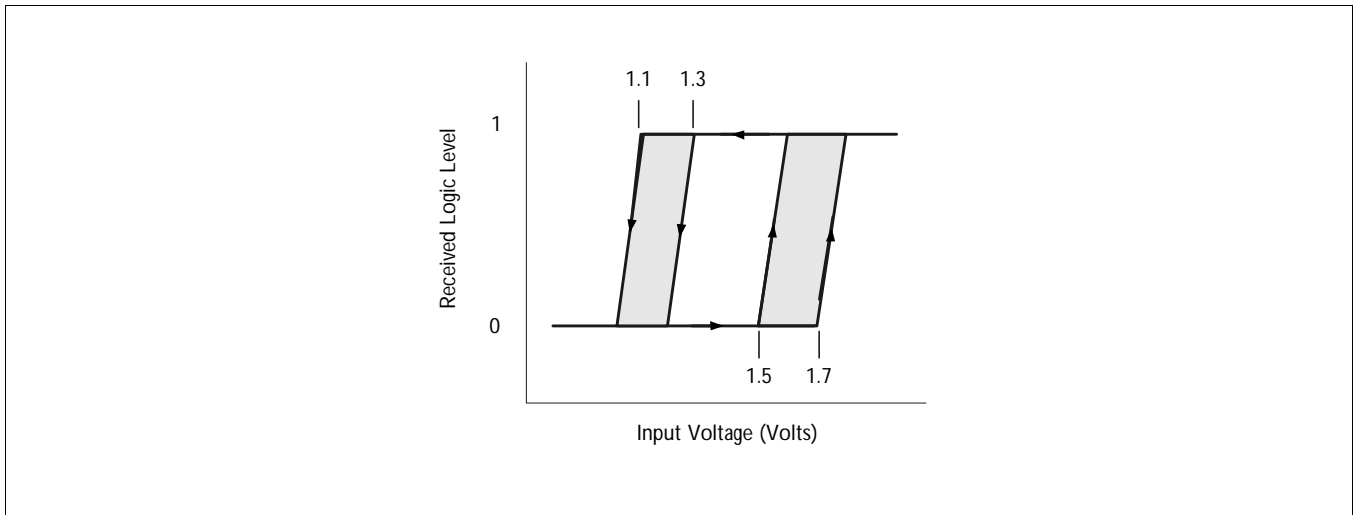
<sup>1</sup> Active negation outputs only: Data, Parity, SREQ/, SACK/

<sup>2</sup> Single pin only; irreversible damage may occur if sustained for one second

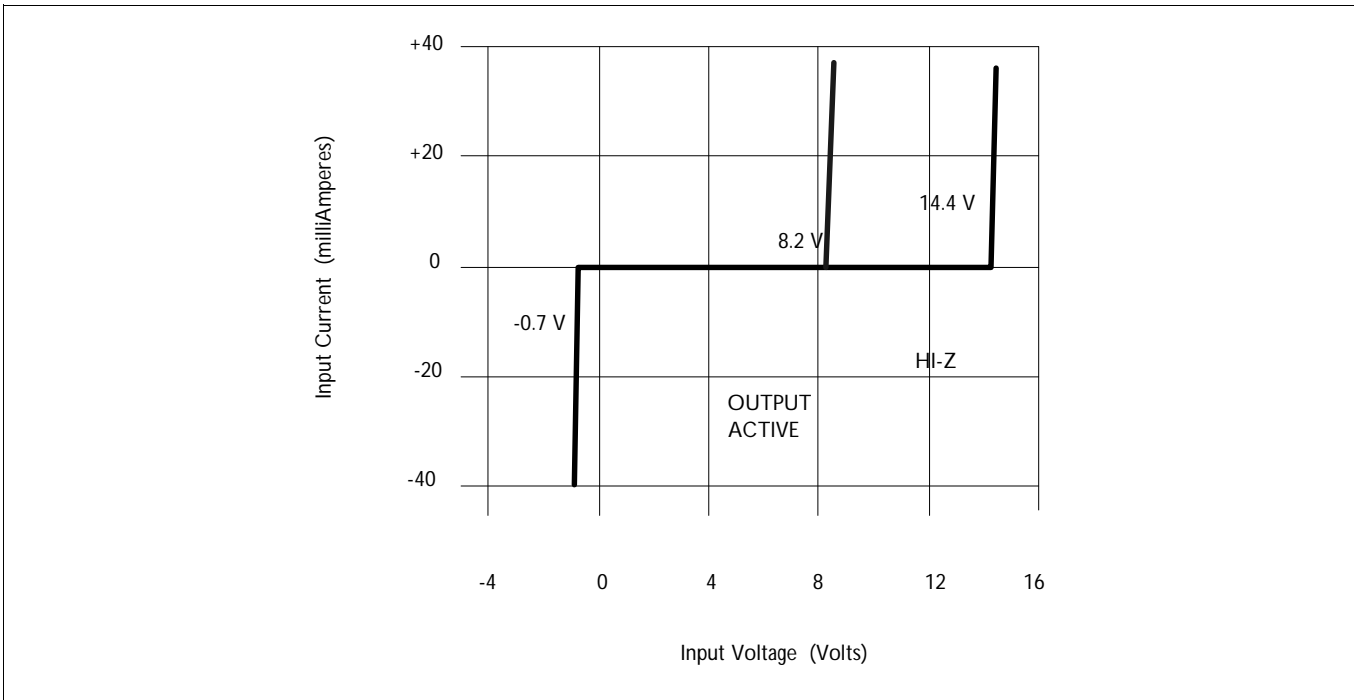
<sup>3</sup> SCSI RESET pin has 10 k $\Omega$  pull-up resistor



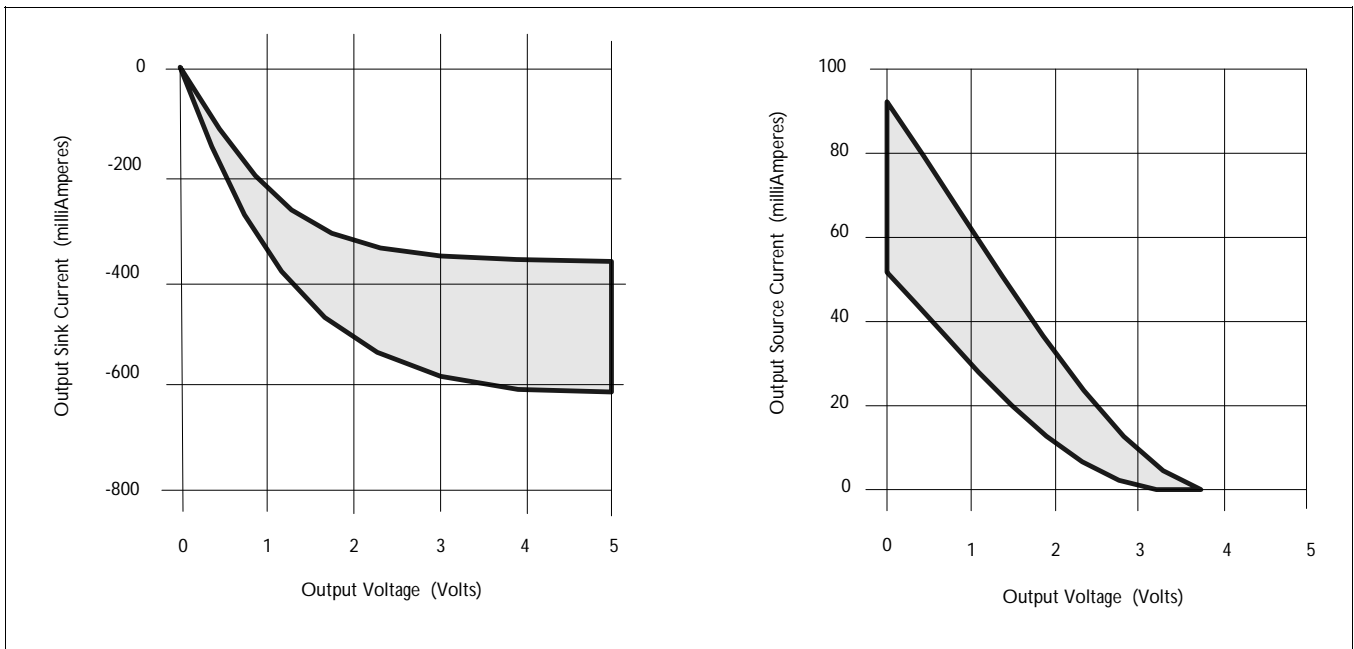
**Figure 4-1: Rise and Fall Time Test Conditions**



**Figure 4-2: Hysteresis of SCSI Receiver**



**Figure 4-3: Input Current as a Function of Input Voltage**



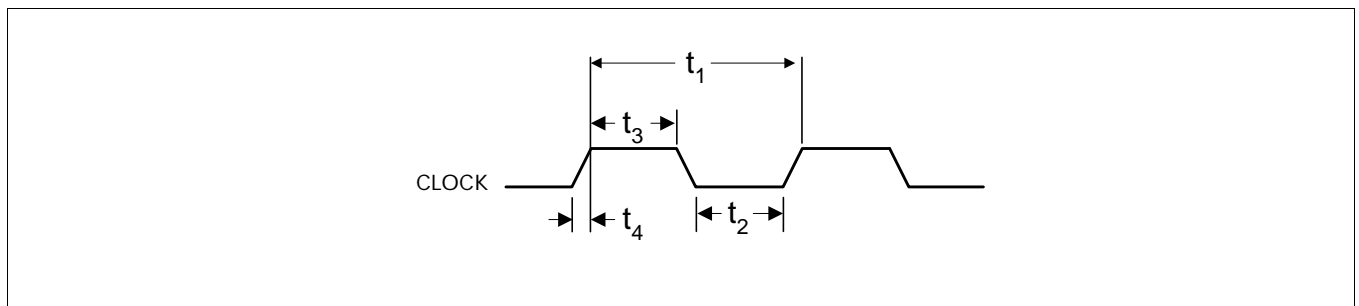
**Figure 4-4: Output Current as a Function of Output Voltage**

## AC Characteristics

The AC characteristics described in this section apply over the entire range of operating conditions (refer to the DC Characteristics section). Chip timings are based on simulation at worst case voltage, temperature, and processing. The SYM53C120 requires a 40 MHz clock input.

**Table 4-11: Clock Timing**

| Symbol | Parameter       | Min  | Max  | Units |
|--------|-----------------|------|------|-------|
| $t_1$  | Clock period    | 24.5 | 25.5 | ns    |
| $t_2$  | Clock low time  | 10   | 15   | ns    |
| $t_3$  | Clock high time | 10   | 15   | ns    |
| $t_4$  | Clock rise time | 1    | -    | V/ns  |



**Figure 4-5: Clock Timing**

## SCSI Interface Timings

**Table 4-12: Input Timings**

| Symbol | Parameter                             | Min | Max | Units |
|--------|---------------------------------------|-----|-----|-------|
| $t_1$  | Input data setup                      | 1   | -   | ns    |
| $t_2$  | Input data hold                       | 6   | -   | ns    |
| $t_3$  | Input REQ/ACK assertion pulse width   | 11  | -   | ns    |
| $t_4$  | Input REQ/ACK deassertion pulse width | 16  | -   | ns    |

**Table 4-13: Output Timings**

| Symbol | Parameter                  | Min  | Max  | Units |
|--------|----------------------------|--|--|-------|
| $t_5$  | Output data setup          | $\min [t_1 + 17\text{ns}, t_4 + 5]$                    | -  | ns    |
| $t_6$  | Output data hold           | $\max [24, (t_2 - 20), t_3]$                           | -  | ns    |
| $t_7$  | Output REQ/ACK pulse width | $\max [20 \text{ ns}, t_3 - 5]$                        | $\max [30 \text{ ns}, t_3 + 5]$                        | ns    |
| $t_8$  | REQ/ACK transport delay    | 25 ns if REQ/ACK is clock for input data, 10 ns if not | 50 ns if REQ/ACK is clock for input data, 30 ns if not | ns    |
| $t_9$  | Data transport delay       | 6  | $[t_3 + 35]$   | ns    |



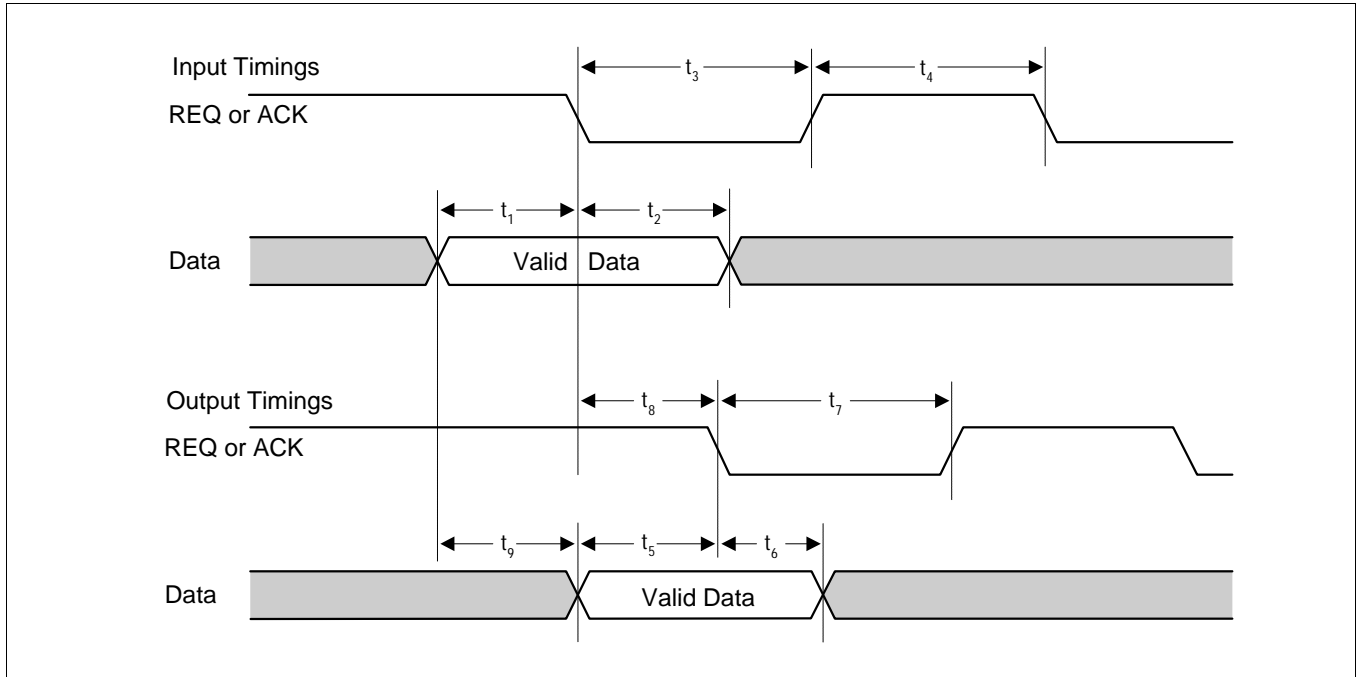


Figure 4-6: Input /Output Timings



## Chapter 5

# SYM20101/2 SCSI Bus Boards

## SYM20101/2 Circuit Board Description

This chapter describes the SYM20101/2 family of SCSI boards based on the SYM53C120 SCSI Bus Expander chip. The SYM20101 Extender and the SYM20102 Converter are wide (16-bit) SCSI Bus boards. The SYM20101 board connects a single-ended SCSI bus to another single-ended bus. The SYM20102 board connects a single-ended SCSI bus to a differential SCSI bus. These boards provide electrical isolation between two SCSI buses, allowing for increased device connectivity and greater cable distances. The board attaches directly to the SCSI bus; target and initiator devices can be located on either the A bus or the B bus. Supporting SCSI-1, -2 and -3 standards, the boards work with any Symbios Logic SCSI products, as well as any other industry-standard SCSI controllers and devices up to Wide Ultra SCSI with transfer rates of 40 Mbytes/second. The following describes the functions of the circuitry on the SYM20101/2.

The heart of the SYM20101 and SYM20102 boards is the SYM53C120 SCSI Bus Expander chip, which is described in Chapters 1 through 4 of this manual. The SYM53C120 chip provides the capability to check SCSI signal tolerances as signals are received and, if necessary, realign them to the SCSI specification. This includes re-timing logic, precision delay control, state machine control and differential control for the SCSI signals. The additional circuitry on the SYM20101/2 boards provide electrical isolation, termination and buffering of the signals. The first part of this chapter describes the common characteristics both boards. The end of this chapter describes the unique characteristics of each board.

### Features

- SCSI Interface
  - Two 16-bit SCSI interfaces logically connected through the SYM53C120 Bus Expander chip
  - Active termination on the single-ended buses
  - Remote termination control
  - 68-pin high density connectors
  - Configuration switches and connector for enabling termination power
  - LEDs indicating busy and termination fault
  - Wide Ultra SCSI data transfer capability
- Board Dimensions
  - SYM20101 SCSI Bus Extender board 4.00" X 3.00"
  - SYM20102 SCSI Bus Converter board 3.95" X 4.50"

### Physical Characteristics

The SYM20101/2 boards are palm-size rectangular boards each with opposing 68-pin connectors, a disk drive type power connector, and a subsystem interface to control termination and indicate busy. The boards are designed to be mounted in an enclosure.

### Electrical Characteristics

The SYM20101/2 boards maximum power requirements, including SCSI TERMPWR, under normal operation is:

- +5V DC  $\pm 5\%$  1.1A over the operating range of 5°C to 55°C

Under abnormal conditions such as a short on SCSI TERMPWR, +5V current may be higher. At temperatures of at least 25°C a current of 4.0A is sustained no longer than 30 seconds before the self-resetting TERM-PWR short circuit protection device opens.

---

### Thermal, Atmospheric Characteristics

The boards are designed to operate in an environment defined by the following parameters:

- Temperature range: 5°C to 55°C (dry bulb)
- Relative humidity range: 5% to 90% non-condensing
- Maximum dew point temperature: 32°C
- Storage Temperature:
  - Temperature range: -45°C to +105°C (dry bulb)  $\Delta$  10°C per hour
  - Relative Humidity range: 0% to 90% non-condensing

---

### Electromagnetic Compliance

The boards are designed and implemented to minimize electromagnetic emissions, susceptibility, and the effects of electromagnetic discharge. The boards meet the emission requirements of CISPR II, VCCI and FCC Class B as well as the immunity requirements for CE mark and carries the CE logo.

---

### Safety Characteristics

The bare boards meet or exceed the requirements of UL flammability rating 94V0. The bare boards are also marked with the supplier's name or trademark, type, and UL flammability rating. All voltages these boards use are below the SELV 42.4V limit.

---

### Performance Characteristics

The SCSI interface operates at a burst transfer rate of up to 40 MBytes per second for wide SCSI. Actual transfer rates are a function of the subsystem.

---

### Compatibility

The SCSI interface is compatible with the AMSI standard X3T9.2.

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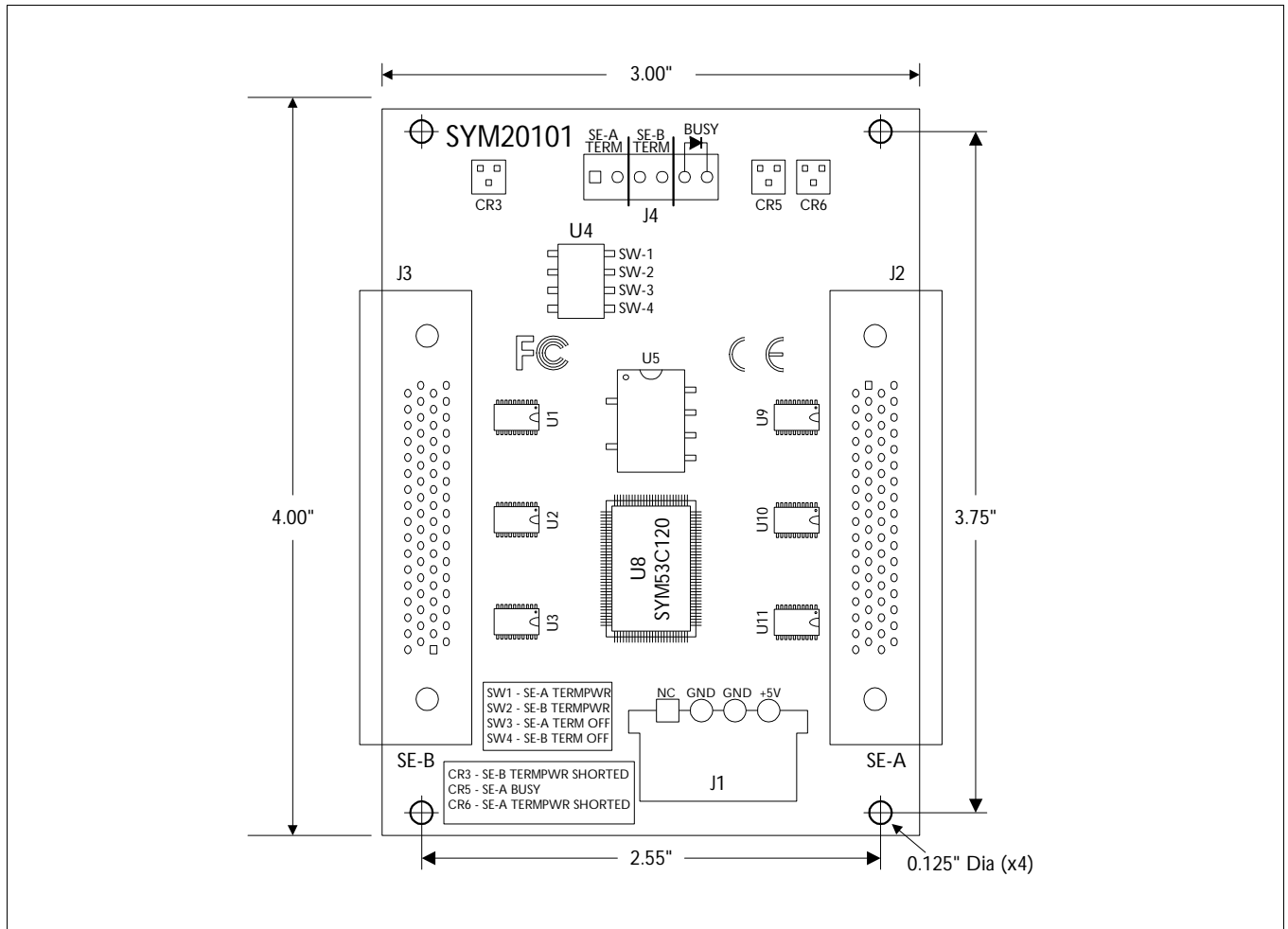
### Operational Characteristics

The SYM20101/2 boards are designed for use in computer systems needing electrical isolation via extension or conversion of the SCSI bus. The operation is logically transparent to software, data, and bus protocol operations. It uses no software code and does not use a SCSI ID. In its simplest form, the SYM53C120 based boards passes data and parity from a source bus to a load bus. The simplest model is that the SYM53C120 is just pieces of wire that allow corresponding SCSI signals to flow from side to side.

# SYM20101 SCSI Bus Extender Board

The SCSI functionality for the SYM20101 Extender board is contained within the SYM53C120 SCSI Bus Expander chip. The SYM20101 physically and electrically connects two single-ended SCSI buses as one logi-

cal SCSI bus, re-generates timing, and passes bus protocol in compliance with the SCSI standard. The SYM20101 board is designed for use in computer systems needing isolation, and/or extension of the SCSI bus. The board requires no software code and does not use a SCSI ID. Figure 5-1 illustrates the component location on the SYM20101 board.



**Figure 5-1: SYM20101 SCSI Bus Extender Board**

## Connectors

- J1 is a standard disk drive power connector. (AMP 641737-1 or equivalent)
- J2 and J3 are 68-pin, high density, shielded, latching, right-angle SCSI connectors. (AMP 787171-7 or equivalent)
- J4 is a 6-pin unshrouded header. (AMP 104427-4 or equivalent)

## Physical Characteristics

The dimensions of the SYM20101 SCSI Bus Extender board are 3.00" x 4.00". Power connection is made through connector J1. SCSI connection is made through high density connectors J2 and J3. Board mounted LEDs or external LED connected to J4 display SCSI bus activity and Termination Power status. Switch pack U4 is combination with external switches connected to J4 control termination. The component height on the top of the board is not greater than 0.5".

## Board Mounting

The SYM20101 SCSI Bus Extender board is designed to be mounted in an enclosure or computer cabinet. The SYM20101 mounting holes are 0.125 inch in diameter. They are located 2.55" by 3.75" apart in relation to the 3.00" by 4.00" size of the board. The mounting holes are spaced equal distance from the edges of the board.

## Board Connectors

There are four connectors on the SYM20101 board:

- Power Connector J1
- SCSI Connectors J2 and J3
- LED and SCSI Terminators Signals J4

### Power Connector J1

The DC power interface is designed to receive a standard disk drive type power plug. The Termination Power (TERMPWR) circuitry has a +5V connection through a diode and a vendor-recommended capacitance value of 0.1µF. There is a fuse between the +5V connector and the SCSI bus TERMPWR connectors.

**Table 5-1: Power Connector J1**

| J1-Pin Number | Signal Name |
|---------------|-------------|
| 1             | Open        |
| 2             | Ground      |
| 3             | Ground      |
| 4             | +5 Volts    |

## SCSI Connectors J2 and J3

The single-ended SCSI interface on the SYM20101 board operates as either an 8-bit or 16-bit, synchronous or asynchronous SCSI bus. The signal definitions conform to the SCSI-2 single-ended standard. The SCSI interface connectors J2 and J3 are both 68-pin high density latching right angle receptacles and the pin definitions conform to the X3T9.2/90-048 single-ended P cable recommendation. SCSI termination power can also be supplied by the board. The following table shows the signal assignments for J2 and J3.

**Table 5-2: SE SCSI 68-pin Connectors J2 & J3**

| Pin | Signal Name | Pin | Signal Name |
|-----|-------------|-----|-------------|
| 1   | GROUND      | 35  | SD(12)      |
| 2   | GROUND      | 36  | SD(13)      |
| 3   | GROUND      | 37  | SD(14)      |
| 4   | GROUND      | 38  | SD(15)      |
| 5   | GROUND      | 39  | SD(P1)      |
| 6   | GROUND      | 40  | SD(0)       |
| 7   | GROUND      | 41  | SD(1)       |
| 8   | GROUND      | 42  | SD(2)       |
| 9   | GROUND      | 43  | SD(3)       |
| 10  | GROUND      | 44  | SD(4)       |
| 11  | GROUND      | 45  | SD(5)       |
| 12  | GROUND      | 46  | SD(6)       |
| 13  | GROUND      | 47  | SD(7)       |
| 14  | GROUND      | 48  | SD(P0)      |
| 15  | GROUND      | 49  | GROUND      |
| 16  | GROUND      | 50  | GROUND      |
| 17  | TERMPWR     | 51  | TERMPWR     |
| 18  | TERMPWR     | 52  | TERMPWR     |
| 19  | No Connect  | 53  | No Connect  |
| 20  | GROUND      | 54  | GROUND      |
| 21  | GROUND      | 55  | SATN        |
| 22  | GROUND      | 56  | GROUND      |
| 23  | GROUND      | 57  | SBSY        |
| 24  | GROUND      | 58  | SACK        |
| 25  | GROUND      | 59  | SRST        |
| 26  | GROUND      | 60  | SMSG        |

**Table 5-2: SE SCSI 68-pin Connectors J2 & J3**

| Pin | Signal Name | Pin | Signal Name |
|-----|-------------|-----|-------------|
| 27  | GROUND      | 61  | SSEL        |
| 28  | GROUND      | 62  | SC/D        |
| 29  | GROUND      | 63  | SREQ        |
| 30  | GROUND      | 64  | SI/O        |
| 31  | GROUND      | 65  | SD(8)       |
| 32  | GROUND      | 66  | SD(9)       |
| 33  | GROUND      | 67  | SD(10)      |
| 34  | GROUND      | 68  | SD(11)      |

**External Termination Control Connector J4**

A-Side and B-Side single-ended termination circuit provides termination for the SCSI buses. On-board termination for each of the two physical busses is controlled in one of two ways: switches or the termination interface (J4).

**Switches**

The SYM20101 board contains the following four switches at location U4.

**Table 5-3: U4 Switches**

| Switch | Position | Condition | Description              |
|--------|----------|-----------|--------------------------|
| SW1    | ON       | Enable    | A-Side Termination Power |
|        | OFF      | Disabled  |                          |
| SW2    | ON       | Enable    | B-Side Termination Power |
|        | OFF      | Disabled  |                          |
| SW3    | ON       | Disabled  | A-Side Termination       |
|        | OFF      | Enabled   |                          |
| SW4    | ON       | Disabled  | B-Side Termination       |
|        | OFF      | Enabled   |                          |

**Termination Interface**

The termination control on the SYM20101 board permits the connection of a subsystem harness for external control of the on-board active SCSI terminators. Con-

necting the Disable SE-A TERM or Disable SE-B TERM pins on J4 to ground turns-off on-board termination on the indicated physical bus. See the following table.

**Table 5-4: Termination Control Connector J4**

| J4-Pin Number | Signal Name       |
|---------------|-------------------|
| 1             | Disable SE-A TERM |
| 2             | Ground            |
| 3             | Disable SE-B TERM |
| 4             | Ground            |

**LEDs and Connector J4**

The SYM20101 board contains three LEDs: one bus activity LED, and two board status LEDs.

One green LED indicates SCSI Bus Busy.

Two yellow LEDs, one for each bus, indicate when termination power (TERMPWR) is shorted to ground. For instance, if Termination Power is grounded somewhere in the subsystem while Termination power is supplied by the board (when U4 switches SW1 and/or SW2 are enabled).

**Table 5-5: LED Description**

| LED | Color/Condition | Description                          |
|-----|-----------------|--------------------------------------|
| CR3 | Yellow/ON       | B-Side, TERMPWR shorted to ground    |
| CR5 | Green/ON        | A-Side, BUSY (SCSI active on Side-A) |
| CR6 | Yellow/ON       | A-Side, TERMPWR shorted to ground    |

The connector J4, pins 5 and 6, is an LED interface that contains the signal and ground for the SCSI Busy LED. An external LED harness can be connected to the board for external mounting of a SCSI Busy LED.

**Table 5-6: LED Connector J4**

| J4-Pin Number | Signal Name |
|---------------|-------------|
| 5             | BUSY LED+   |
| 6             | BUSY LED-   |

# SYM20101 SCSI Bus Extender Board Installation Instructions

## Software Requirements

There are no software requirements for this board.

## Board Mounting

Mount the board inside the selected enclosure using four fasteners in the 0.125" diameter mounting holes.

## Setting Switches

Use the information under the heading *Switches* or the information on the board to properly set the switches at board location U4.

## Connecting Cables

- Connect power plug to connector J1.
- Connect SCSI cables to connectors J2 and J3.
- Connect optional harness to connector J4 for external control of active SCSI terminators using external switches and to view SCSI bus activity on an LED.

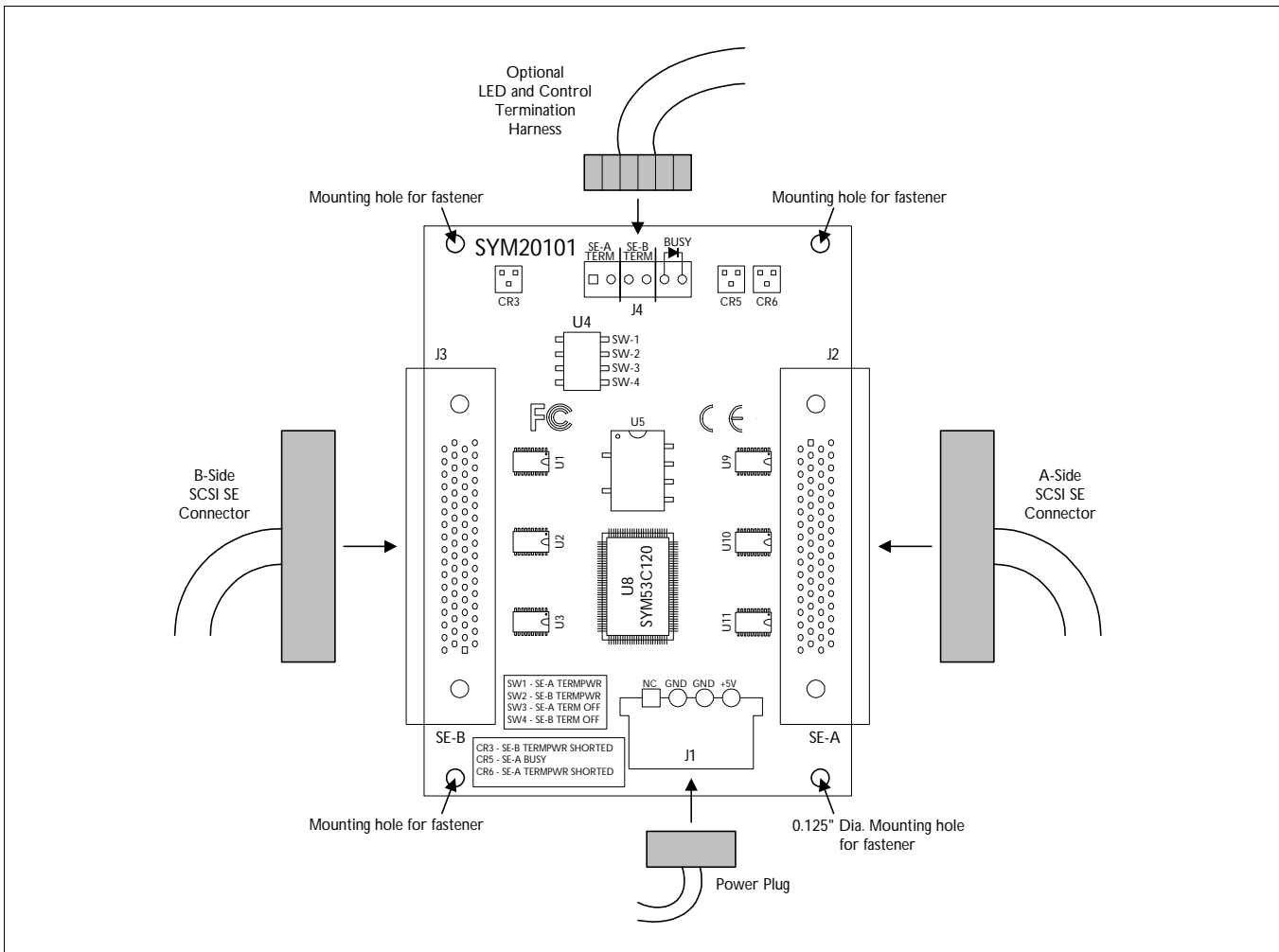


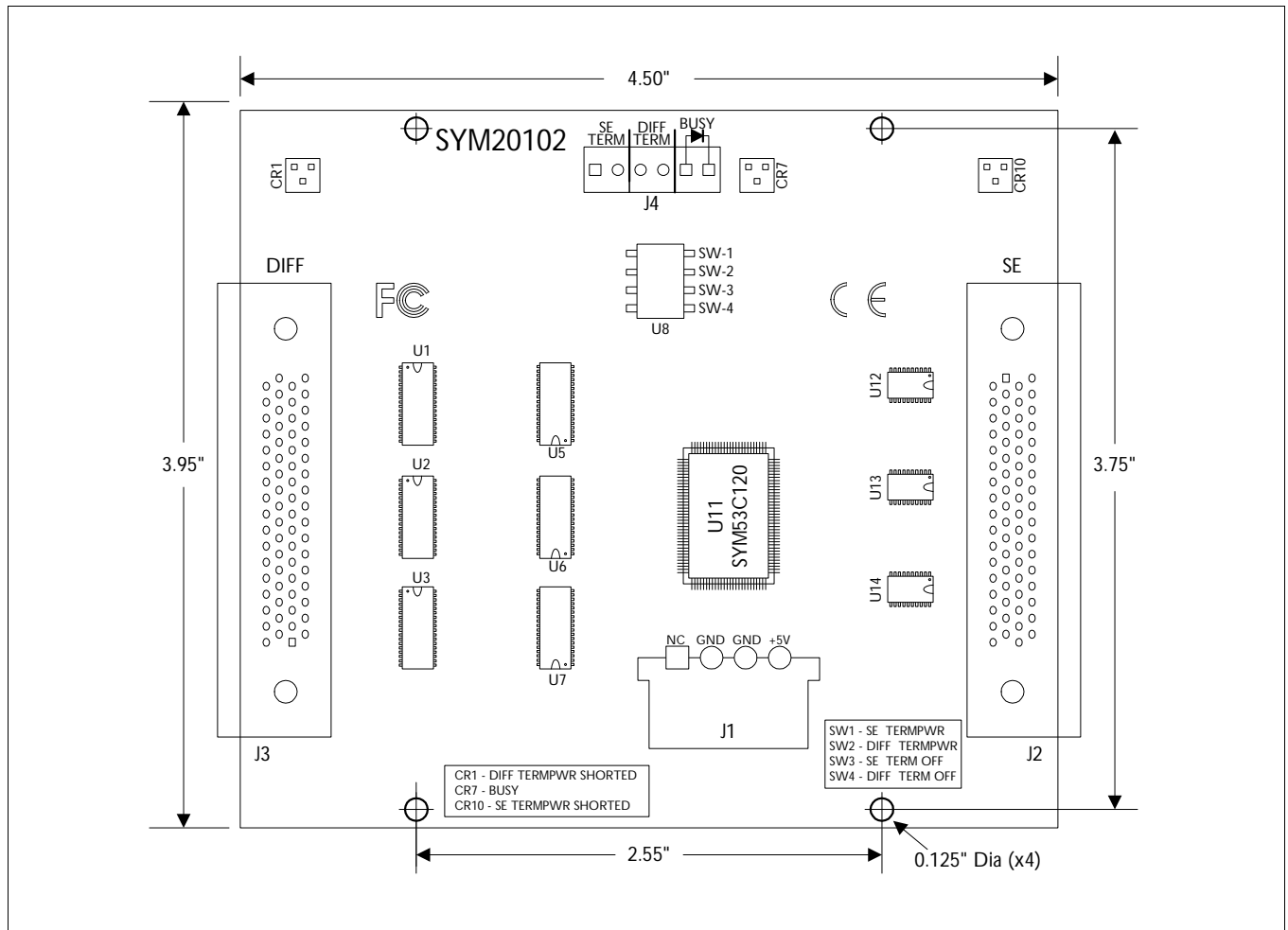
Figure 5-2: SYM20101 Board Installation



# SYM20102 SCSI Bus Converter Board

The SCSI functionality for the SYM20102 Converter board is contained within the SYM53C120 SCSI Bus Expander chip. The SYM20102 physically and electrically connects one single-ended SCSI buses and one differential SCSI bus as one logical SCSI bus, re-gener-

ates timing, and passes bus protocol in compliance with the SCSI standard. The SYM20102 board is designed for use in computer systems needing isolation, and extension or transceiver translation of the SCSI bus. The operation is logically transparent to software and data, uses no software code and does not use a SCSI ID. Figure 5-3 illustrates the component location on the SYM20102 Converter board.



**Figure 5-3: SYM20101 SCSI Bus Converter Board**

## Connectors

- J1 is a standard disk drive power connector. (AMP 641737-1 or equivalent)
- J2 and J3 are 68-pin high density shielded latching

right-angle SCSI connectors. (AMP 787171-7 or equivalent)

- J4 is a 6-pin unshrouded header. (AMP 104427-4 or equivalent)

## Physical Characteristics

The dimensions of the SYM20102 Extender board are 3.95" x 4.50". Power connection is made through connector J1. SCSI connection is made through high density connectors J2 and J3. Board mounted LEDs or external LED connected to J4 display SCSI bus activity and Termination Power status. Switch pack U4 is combination with external switches connected to J4 control termination. The component height on the top of the board is not greater than 0.5".

## Board Mounting

The SYM20102 Converter board is designed to be mounted in an enclosure or computer cabinet. The SYM20102 mounting holes are 0.125 inch in diameter. They are located 2.55" by 3.75" apart in relation to the 3.95" by 4.50" size of the board. The mounting holes are spaced equal distance from the edges of the board.

## Board Connectors

There are four connectors on the SYM20102 board:

- Power Connector J1
- SCSI Connectors J2 and J3
- LED and SCSI Terminators Signals J4

### Power Connector J1

The DC power interface is designed to receive a standard disk drive type power plug. The Termination Power (TERMPWR) circuitry has a +5V connection through a diode and a vendor-recommended capacitance value of 0.1µF. There is a fuse between the +5V connector and the SCSI bus TERMPWR connectors.

**Table 5-7: Power Connector J1**

| J1-Pin Number | Signal Name |
|---------------|-------------|
| 1             | Open        |
| 2             | Ground      |
| 3             | Ground      |
| 4             | +5 Volts    |

## SCSI Connectors J2 and J3

The SCSI interfaces on the SYM20102 board operates as either an 8-bit or 16-bit, synchronous or asynchronous SCSI bus. The SCSI interface connectors J2 and J3 are both 68-pin high density latching right angle receptacles and the pin definitions conform to the X3T9.2/90-048 single-ended P cable recommendation. SCSI termination power can also be supplied by the board. Connector J2 is a single-ended only connector and its pin-out is the same as shown in Table 5-2. The following table shows the signal assignments for J3 which is a single-ended or a differential connection.

**Table 5-8: DIFF SCSI 68-pin Connector J3**

| Pin | Signal Name | Pin | Signal Name |
|-----|-------------|-----|-------------|
| 1   | +DB(12)     | 35  | -DB(12)     |
| 2   | +DB(13)     | 36  | -DB(13)     |
| 3   | +DB(14)     | 37  | -DB(14)     |
| 4   | +DB(15)     | 38  | -DB(15)     |
| 5   | +DB(P1)     | 39  | -DB(P1)     |
| 6   | +DB(0)      | 40  | -DB(0)      |
| 7   | +DB(1)      | 41  | -DB(1)      |
| 8   | +DB(2)      | 42  | -DB(2)      |
| 9   | +DB(3)      | 43  | -DB(3)      |
| 10  | +DB(4)      | 44  | -DB(4)      |
| 11  | +DB(5)      | 45  | -DB(5)      |
| 12  | +DB(6)      | 46  | -DB(6)      |
| 13  | +DB(7)      | 47  | -DB(7)      |
| 14  | +DB(P0)     | 48  | -DB(P0)     |
| 15  | GROUND      | 49  | GROUND      |
| 16  | DIFFSENS    | 50  | GROUND      |
| 17  | TERMPWR     | 51  | TERMPWR     |
| 18  | TERMPWR     | 52  | TERMPWR     |
| 19  | RESERVED    | 53  | RESERVED    |
| 20  | GROUND      | 54  | GROUND      |
| 21  | +ATN        | 55  | -ATN        |
| 22  | GROUND      | 56  | GROUND      |
| 23  | +BSY        | 57  | -BSY        |
| 24  | +ACK        | 58  | -ACK        |
| 25  | +RST        | 59  | -RST        |

**Table 5-8: DIFF SCSI 68-pin Connector J3**

| Pin | Signal Name | Pin | Signal Name |
|-----|-------------|-----|-------------|
| 26  | +MSG        | 60  | -MSG        |
| 27  | +SEL        | 61  | -SEL        |
| 28  | +C/D        | 62  | -C/D        |
| 29  | +REQ        | 63  | -REQ        |
| 30  | +I/O        | 64  | -I/O        |
| 31  | +D(8)       | 65  | -D(8)       |
| 32  | +D(9)       | 66  | -D(9)       |
| 33  | +D(10)      | 67  | -D(10)      |
| 34  | +D(11)      | 68  | -D(11)      |

**External Termination Control Connector J4**

A-Side and B-Side single-ended termination circuit provides termination for the SCSI buses. On-board termination for each of the two physical busses is controlled in one of two ways: switches or the termination interface (J4).

**Switches**

The SYM20102 board contains the following four switches at location U8.

**Table 5-9: U8 Switches**

| Switch | Position | Condition | Description       |
|--------|----------|-----------|-------------------|
| SW1    | ON       | Enable    | A-Side            |
|        | OFF      | Disabled  | Termination Power |
| SW2    | ON       | Enable    | B-Side            |
|        | OFF      | Disabled  | Termination Power |
| SW3    | ON       | Disabled  | A-Side            |
|        | OFF      | Enabled   | Termination       |
| SW4    | ON       | Disabled  | B-Side            |
|        | OFF      | Enabled   | Termination       |

**Termination Interface**

The termination control on the SYM20101 board permits the connection of a subsystem harness for external control of the on-board active SCSI terminators. Con-

necting the Disable SE-A TERM or Disable SE-B TERM pins on J4 to ground turns-off on-board termination on the indicated physical bus. See the following table.

**Table 5-10: Termination Control Connector J4**

| J4-Pin Number | Signal Name       |
|---------------|-------------------|
| 1             | Disable SE-A TERM |
| 2             | Ground            |
| 3             | Disable SE-B TERM |
| 4             | Ground            |

**LEDs and Connector J4**

The SYM20102 board contains three LEDs: one bus activity LED and two board status LEDs.

One green LED indicates SCSI bus busy.

Two yellow LEDs, one for each bus, indicate when termination power (TERMPWR) is shorted to ground. For instance, if Termination Power is grounded somewhere in the subsystem while Termination power is supplied by the board (when U8 switches SW1 and/or SW2 are enabled).

**Table 5-11: LED Description**

| LED  | Color/Condition | Description                          |
|------|-----------------|--------------------------------------|
| CR1  | Yellow/ON       | B-Side, TERMPWR shorted to ground    |
| CR7  | Green/ON        | A-Side, BUSY (SCSI active on Side-A) |
| CR10 | Yellow/ON       | A-Side, TERMPWR shorted to ground    |

The connector J4, pins 5 and 6, is an LED interface that contains the signal and ground for the SCSI Busy LED. An external LED harness can be connected to the board for external mounting of a SCSI Busy LED.

**Table 5-12: LED Connector J4**

| J4-Pin Number | Signal Name |
|---------------|-------------|
| 5             | BUSY LED+   |
| 6             | BUSY LED-   |

# SYM20102 SCSI Bus Converter Board Installation Instructions

## Software Requirements

There are no software requirements for this board.

## Board Mounting

Mount the board inside the selected enclosure using four fasteners in the provided mounting holes. Make sure nothing touches any of the board's electrical components that might short them out.

## Setting Switches

Use the information under the heading *Switches* or the information on the board to properly set the switches at board location U8.

## Connecting Cables

- Connect power plug to connector J1.
- Connect SCSI cables to connectors J2 and J3.
- Connect optional harness to connector J4 for external control of active SCSI terminators using external switches and to view SCSI bus activity on an LED.

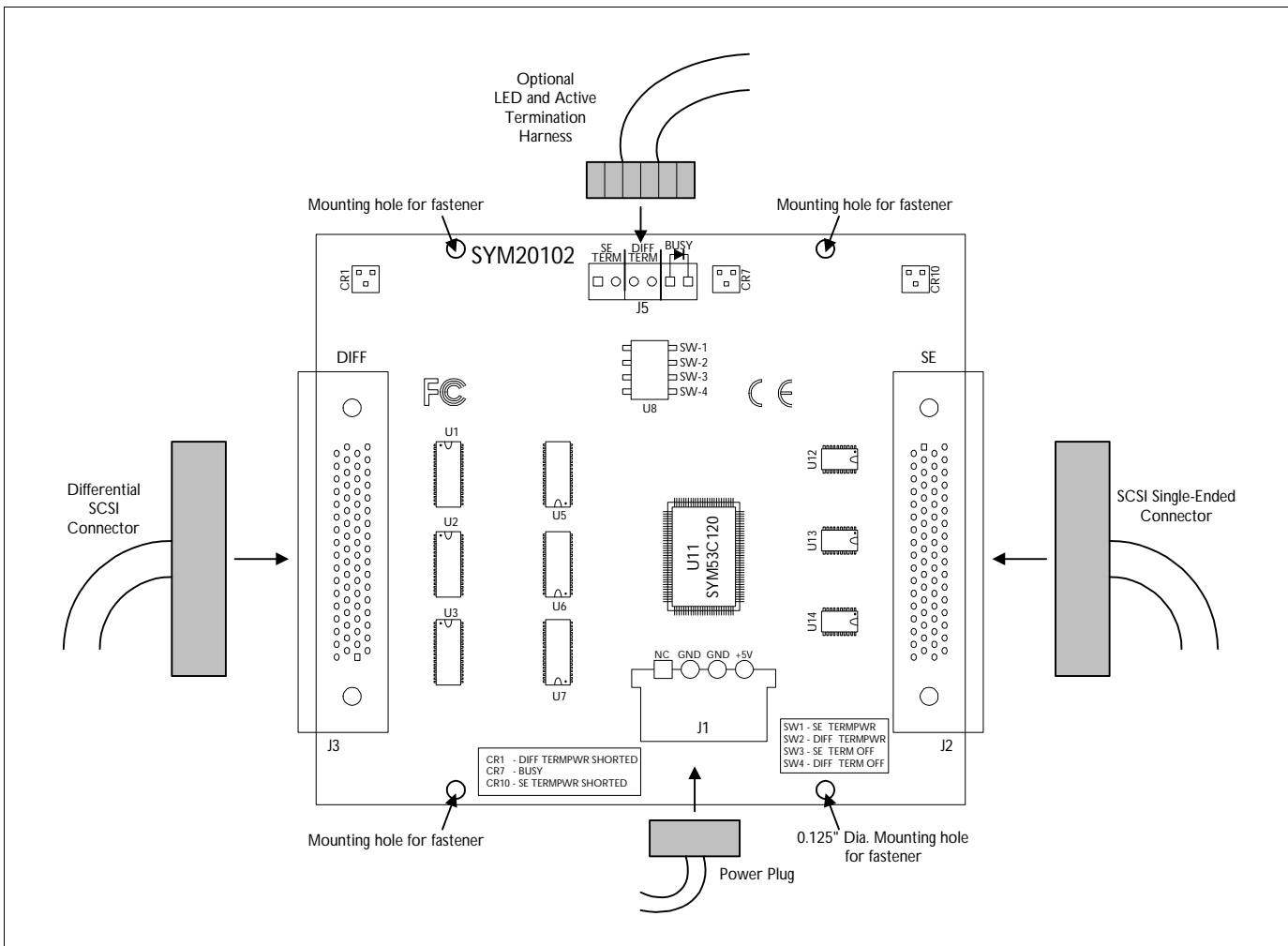
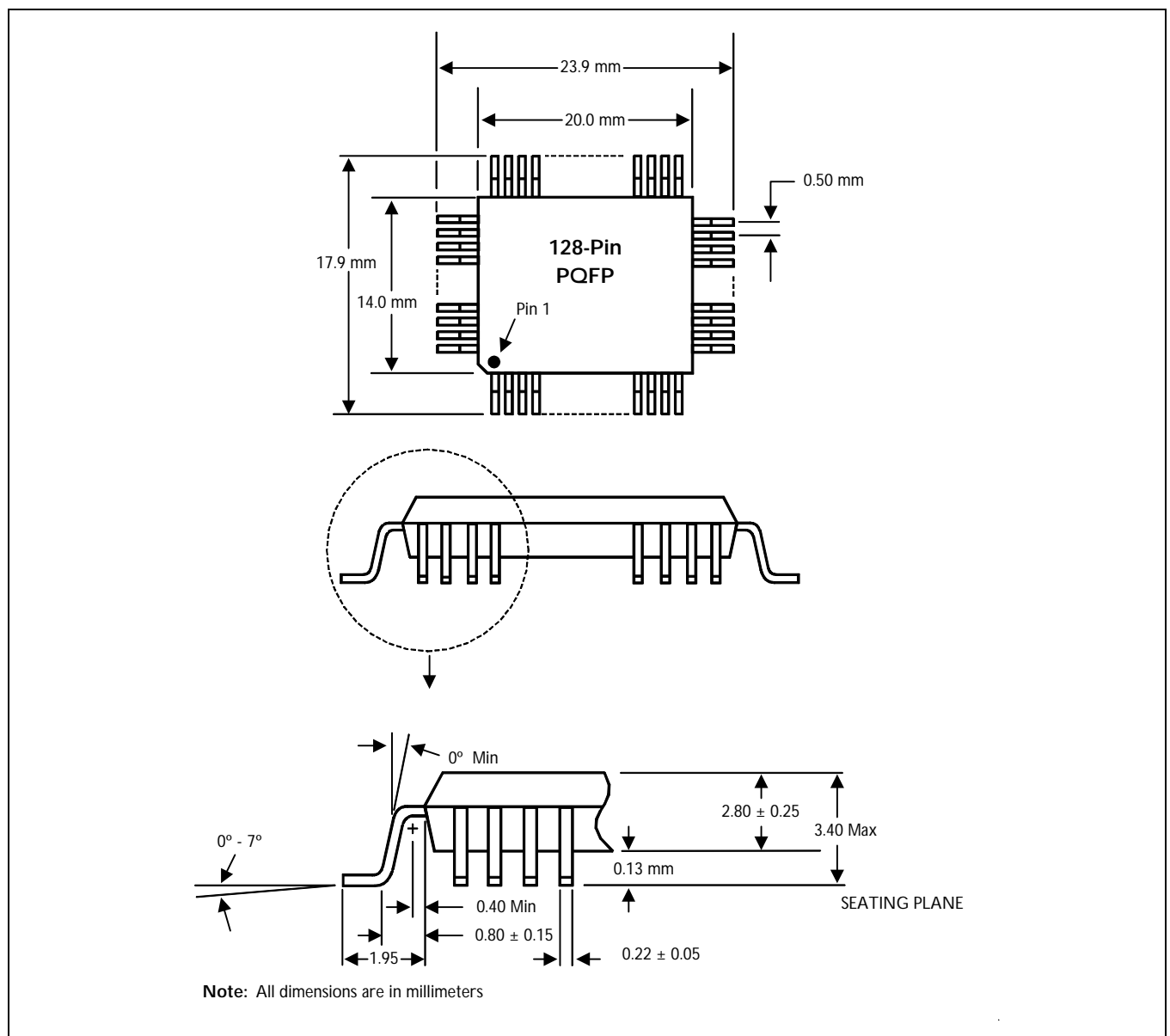


Figure 5-4: SYM20102 Board Installation

# Appendix A Mechanical Drawings

## SYM53C120 Mechanical Drawing

The SYM53C120 comes in a 128-pin metric Plastic Quad Flat Package (PQFP) with a 3.9 mm footprint.



**Figure A-1: SYM53C120 Mechanical Drawing**



# Appendix B Differential Wiring Diagram

## SYM53C120 Differential Wiring Diagram

Figure B-1 shows the wiring diagram for Ultra SCSI operation in the differential mode using pull-up resistors.

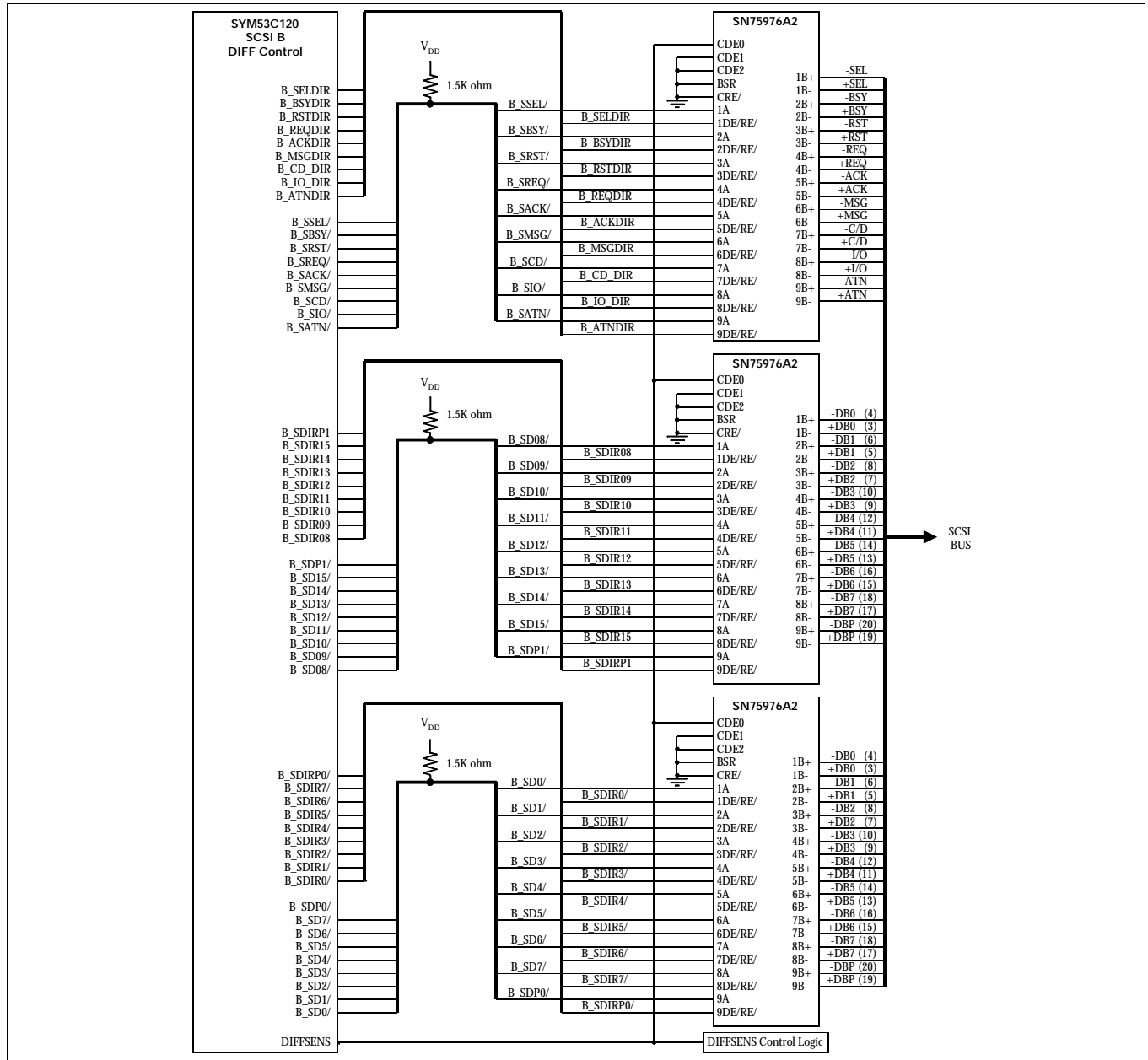


Figure B-1: SYM53C120 Differential Wiring Diagram





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# Glossary

**ACK/**

Acknowledge – Driven by an initiator, ACK/ indicates an acknowledgment for a SCSI data transfer. In the target mode, ACK/ is received as a response to the REQ/ Signal.

**ANSI**

American National Standards Institute.

**Arbitration**

The process of selecting one respondent from a collection of several candidates that request service concurrently.

**Asserted**

A signal is asserted when it is in the state which is indicated by the name of the signal. Opposite of negated or de-asserted.

**Assertion**

The act of driving a signal to the true state.

**Asynchronous Transmission**

Transmission in which each byte of the information is synchronized individually, through the use of Request (REQ/) and Acknowledge (ACK/) signals.

**ATN/**

Attention – Driven by an initiator, indicates an attention condition. In the target role, ATN/ is received and is responded to by entering the Message Out Phase.

**Auto-configuration Ports**

Three 8-bit ports (Address, Write\_Data, and Read\_Data) used by software to access the configuration space on each Plug and Play card. The configuration space is implemented as a set of 8-bit registers. These registers are used by the Plug and Play software to issue commands, check status, access the resource data information, and configure the Plug and Play hardware.

**Block**

A block is the basic 512 byte region of storage into which the storage media is divided. The Logical Block Address protocol uses sequential block addresses to access the media.

**BSY/**

Busy – Indicates that the SCSI Bus is being used. BSY/ can be driven by both the initiator and the target device.

**Bus**

A collection of unbroken signal lines that interconnect computer modules. The connections are made by taps on the lines.

**C\_D/**

Control/Data – Driven by a target, indicates Control or Data Information is on the SCSI Bus. This signal is received by the initiator.

**Connect**

The function that occurs when an initiator selects a target to start an operation, or a target reselects an initiator to continue an operation.

**Control Signals**

The set of nine lines used to put the SCSI bus into its different phases. The combinations of asserted and negated control signals define the phases.

**Controller**

A computer module that interprets signals between a host and a peripheral device. Often, the controller is a part of the peripheral device, such as circuitry on a disk drive.

**DB0/-DB7/**

SCSI Data Bits and Parity Bit – These eight Data Bits (DB0/-DB7/), plus a Parity Bit (DBP/), form the SCSI Bus. DB7/ is the most significant bit and has the highest priority ID during the Arbitration

Phase. Data parity is odd. Parity is always generated and optionally checked. Parity is not valid during arbitration.

#### **De-asserted**

The act of driving a signal to the false state or allowing the cable terminators to bias the signal to the false state (by placing the driver in the high impedance condition).

A signal is de-asserted or negated when it is in the state opposite to that which is indicated by the name of the signal. Opposite of asserted.

#### **Device**

A single unit on the SCSI bus, identifiable by an SCSI address. It can be a processor unit, a storage unit (such as a disk or tape controller or drive), an output unit (such as a controller or printer), or a communications unit.

#### **Disconnect**

The function that occurs when a target releases control of the SCSI bus, allowing the bus to go to the Bus Free phase.

#### **Driver**

When used in the context of electrical configuration, “driver” is the circuitry that creates a signal on a line. When used in the context of software, “driver” is the program that translates commands between the initiator and target.

#### **External Configuration**

All SCSI peripheral devices are external to the host enclosure.

#### **External Terminator**

The terminator that exists on the last peripheral subsystem that terminates the external end of the SCSI bus.

#### **Exit-Point Terminator**

A Terminator that may be enabled or disabled which exists at the 50-position high-density connector on hosts that support a mixed configuration (combination of internal and external SCSI peripheral devices).

#### **Free**

In the context of Bus Free phase, “free” means that no SCSI device is actively using the SCSI bus and, therefore, the bus is available for use.

#### **Gigabyte**

One billion bytes; equal to one thousand megabytes.

#### **High (logical level)**

A signal is in the high logic state when it is above approximately 2.5 volts.

#### **Host**

A processor, usually consisting of the central processing unit and main memory. Typically, a host communicates with other devices, such as peripherals and other hosts. On the SCSI bus, a host has an SCSI address.

#### **Host Adapter**

Circuitry that translates between a processor's internal bus and a different bus, such as SCSI. On the SCSI bus, a host adapter usually acts as an initiator.

#### **Initiator**

An SCSI device that requests another SCSI device (a target) to perform an operation. Usually, a host acts as an initiator and a peripheral device acts as a target.

#### **Internal Configuration**

All SCSI peripheral devices are internal to the host enclosure.

#### **Internal Terminator**

The terminator that exists within the host that terminates the internal end of the SCSI bus.

#### **I/O/**

Input/Output – Driven by a target, controls the direction of data transfer on the SCSI Bus. When active, this signal indicates input to the initiator. When inactive, this signal indicates output from the initiator. This signal is also used to distinguish between the Selection and Reselection Phases.

**I/O Cycle**

An I/O cycle is an Input (I/O Read) operation or Output (I/O Write) operation that accesses the PC Card's I/O address space.

**I/O Mapped**

A storage location or register is I/O mapped when it is available to be accessed using I/O cycles. The register or storage location might also be accessible using memory cycles, in which case it would also be memory mapped.

**IREQ**

Interrupt Request – Alerts the host computer of a condition that needs to be serviced. Most of the interrupts are individually maskable. The Interrupt Request signal between a PC Card and a socket when the I/O interface is active.

**LBA**

Abbreviation for Logical Block Address.

**Logical Block Address**

A logical block address is a sequential address for accessing the blocks on the storage media. The first block of the media is addressed as block 0 and succeeding blocks are numbered sequentially until the last block is encountered. This is the traditional method for accessing peripherals on an SCSI interface bus.

**Logical Unit**

The logical representation of a physical or virtual device, addressable through a target. A physical device can have more than one logical unit.

**Low (logical level)**

A signal is in the low logic level when it is below approximately 0.5 volts.

**LSB**

Abbreviation for Least Significant Bit or Least Significant Byte. That portion of a number, address or field that occurs right-most when its value is written as a single number in conventional hexadecimal or binary notation. The portion of the number having the least weight in a mathematical calculation using the value.

**LUN**

Logical Unit Number. Used to identify a logical unit.

**Mandatory**

A characteristic or feature that must be present in every implementation of the standard.

**Memory Cycle**

A memory cycle is a memory read (using Output Enable) operation or memory write (using Write Enable / Program) operation that accesses the PC Card's common memory or attribute memory address space.

**Memory Interface**

The memory interface is the default interface after power-up, PCMCIA Hard Reset, and PCMCIA Soft Reset for both PCMCIA cards and sockets. This interface supports memory operations as defined in PCMCIA Release 1.0 and later and is used by both Memory Cards and I/O Cards.

**Memory Mapped**

A storage location or register is memory mapped when it is available to be accessed using memory cycles. The register or storage location might also be accessible using I/O cycles, in which it would also be I/O mapped.

**MHz**

MegaHertz – Measurement in thousands of cycles per second. Used as a measurement of data transfer rate.

**microsecond ( $\mu$ s)**

One millionth of a second.

**MSB**

Abbreviation for Most Significant Bit and Most Significant Byte. That portion of a number, address or field that occurs left-most when its value is written as a single number in conventional hexadecimal or binary notation. The portion of the number having the most weight in a mathematical calculation using the value.

**MSG/**

Message – Driven active by a target during the Message Phase. This signal is received by the initiator.

**nanosecond (ns)**

One billionth of a second.

**Negated**

A signal is negated or de-asserted when it is in the state opposite to that which is indicated by the name of the signal. Opposite of asserted.

**Negation**

The act of driving a signal to the false state or allowing the cable terminators to bias the signal to the false state (by placing the driver in the high impedance condition).

**ns**

nanoseconds.

**PC**

Abbreviation for Personal Computer. Often used to refer to an 80x86 based computer system.

**Parity**

A method of checking the accuracy of binary numbers. An extra bit, called a parity bit, is added to a number. If even parity is used, the sum of all 1s in the number and its corresponding parity is always even. If odd parity is used, the sum of the 1s and the parity bit is always odd.

**Peripheral device**

A device that can be attached to an SCSI bus. Typical peripheral devices are disk drives, tape drives, printers, CD ROMs, or communications units.

**Phase**

One of the eight states to which the SCSI bus can be set. During each phase, different communication tasks can be performed.

**Plug and Play (PnP)**

Plug and Play is a specification that frees users from locating and setting ID and IRQ switches and jumpers. PnP permits a card to be configured automatically after installation.

**Port**

A connection into a bus. The SCSI bus allows eight ports.

**Priority**

The ranking of the devices on the bus during arbitration.

**Protocol**

A convention for data transmission that encompasses timing control, formatting, and data representation.

**Receiver**

The circuitry that receives electrical signals on a line.

**Reconnect**

The function that occurs when a target reselects an initiator to continue an operation after a disconnect.

**Release**

The act of allowing the cable terminators to bias the signal to the false state (by placing the driver in the high impedance condition).

**REQ/**

Request – Driven by a target, indicates a request for an SCSI data-transfer handshake. This signal is received by the initiator.

**Reselect**

A target can disconnect from an initiator in order to perform a time-consuming function, such as a disk seek. After performing the operation, the target can “reselect” the initiator.

**RESET**

Reset – Clears all internal registers when active. It does not assert the SCSI RST/ signal and therefore does not reset the SCSI bus.

**RST**

Reset – Indicates an SCSI Bus reset condition.

**SCSI Address**

The octal representation of the unique address (0-7) assigned to an SCSI device. This address is normally assigned and set in the SCSI device during system installation.

**SCSI ID (Identification) or SCSI Device ID**

The bit-significant representation of the SCSI address referring to one of the signal lines DB0/ through DB7/.

**SCSI**

Small Computer System Interface.

**SCAM**

An acronym for SCSI Configured AutoMagically or SCSI Configured AutoMatically. SCAM is SCSI's new automatic ID assignment protocol. SCAM frees SCSI user's from locating and setting SCSI ID switches and jumpers. SCAM is the key part of Plug and Play SCSI.

**SEL/**

Select – Used by an initiator to select a target or by a target to reselect an initiator.

**Single-ended configuration**

An electrical signal configuration that uses a single line for each signal, referenced to a ground path common to the other signal lines. The advantage of a single-ended configuration is that it uses half the pins, chips, and board area that differential configurations require. The main disadvantage of single-ended configurations is that they are vulnerable to common mode noise. Also, cable lengths are limited.

**Synchronous transmission**

Transmission in which the sending and receiving devices operate continuously at the same frequency and are held in a desired phase relationship by correction devices. For buses, synchronous transmission is a timing protocol that uses a master clock and has a clock period.

**Target**

An SCSI device that performs an operation requested by an initiator.

**Termination**

The electrical connection at each end of the SCSI bus, composed of a set of resistors.

**μs**

Microsecond.



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