Symbios™ SYM53C140 Ultra2 SCSI Bus Expander

Technical Manual

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Preface

This manual provides a description and electrical characteristics of the SYM53C140 Ultra2 SCSI Bus Expander chip that supports all combinations of Single-Ended, Low-Voltage Differential, and High-Voltage Differential SCSI bus conversions.

Audience

This manual assumes some prior knowledge of current and proposed SCSI standards. For background information, please contact:

ANSI
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(212) 642-4900
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Organization

This document has the following chapters and appendixes:

- Chapter 1, **Introduction**, contains the general information about the SYM53C140 product.
- Chapter 2, **Functional Descriptions**, describes the main functional areas of the chip in more detail, including the interfaces to the SCSI bus and external memory.
- Chapter 3, **Specifications**, contains the pin diagram, signal descriptions, electrical characteristics, AC timing diagrams, and mechanical drawing of the SYM53C140.
- Appendix A, **Wiring Diagrams**, contain wiring diagrams that show typical SYM53C140 usage.
- Appendix B, **Glossary**, contains commonly used terms and their definitions.

Revision Record

Page No.	Date	Version	Remarks
All	5/98	0.5	First draft of complete Data Manual.
All	6/99	1.0	Misc. changes / corrections for product introduction.

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Chapter 1
Introduction

1.1 General Description

The SYM53C140 Ultra2 SCSI Bus Expander is a single chip solution allowing the extension of SCSI device connectivity and/or cable length limits. A SCSI bus expander couples bus segments together without any impact to the SCSI protocol, software, or firmware. The SYM53C140 Ultra2 SCSI Bus Expander connects Single-Ended (SE) Ultra, Low-Voltage Differential (LVD) Ultra2 or High-Voltage Differential (HVD) peripherals together in any combination.

The SYM53C140 is capable of supporting any combination of bus mode SE, HVD, or LVD on either the A or B Side port. This provides the system designer with maximum flexibility in designing SCSI backplanes to accommodate any SCSI bus mode.

Figure 1.1 SYM53C140 SCSI Bus Modes

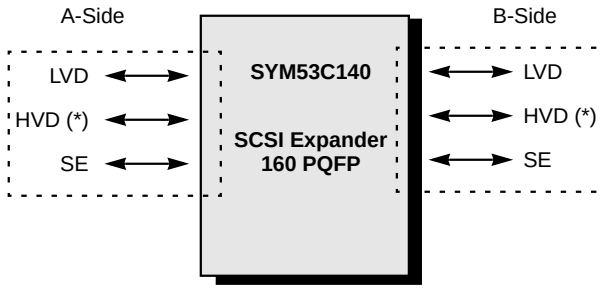


Figure 1.1 shows the three SCSI bus modes available on the A or B Side. LVDlink™ transceivers provide the multimode LVD, SE, or HVD capability. The SYM53C140 operates either as a expander or converter. In both SCSI Bus Expander and Converter modes, cable segments are electrically isolated from each other. This feature maintains the signal integrity of each cable segment.

As shown in Table 1.1, the SYM53C140 operates in all modes: single-ended, low-voltage differential, and high-voltage differential.

Table 1.1 Types of Operation

Signal Type	Mode	Speed
LVD to LVD	Repeater	Ultra2
HVD to HVD[1]	Repeater	Ultra
SE to SE	Repeater	Ultra
Or any combination above for Repeater.		
LVD to HVD[1]	Converter	Ultra
LVD to SE	Converter	Ultra
HVD[1] to SE	Converter	Ultra
Or any combination above for Converter.		

1. All HVD requires external differential transceivers and terminations.

The SYM53C140 provides additional control capability through the pin level electrical isolation mode. This feature permits logical disconnection of both the A Side bus and the B Side bus without disrupting SCSI transfers currently in progress. For example, devices on the logically disconnected B Side can be swapped out while the A Side bus remains active.

The SYM53C140 is based on bus expander technology resulting in some signal filtering and re-timing to maintain signal skew budgets. The SYM53C140 is independent of software.

1.1.1 Applications

- Server clustering environments
- Expanders creating distinct SCSI cable segments which are electrically isolated from each other

Figure 1.2 SYM53C140 Server Clustering

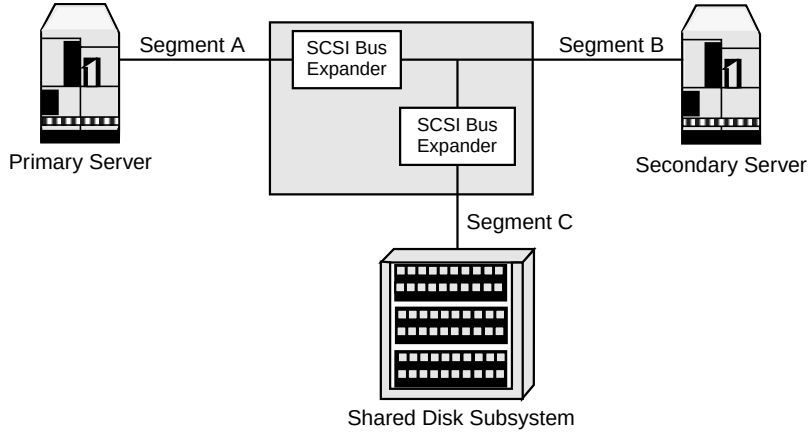


Figure 1.2 demonstrates how SCSI bus expanders are used to couple bus segments together without any impact of the SCSI protocol or software. Configurations that use the SYM53C140 SCSI Bus Expander in the Ultra2 mode (LVD to LVD) allow the system designer to take advantage of the inherent cable distance, device connectivity, data reliability, and increased transfer rate benefits of LVD signaling with Ultra2 SCSI peripherals.

In Figure 1.2 example, the SYM53C140 is configured as a three port expander board. This configuration allows segments A and B to be treated as a point-to-point segment. Segment C is treated as a load segment with at least 8 inches between every node. Table 1.2 shows the various distance requirements for each SCSI bus mode.

Table 1.2 SCSI Bus Distance Requirements

Segment	Mode	Length Limit
A, B	LVD (Ultra2)	25 meters
	SE (Ultra)	20 meters
	HVD (Ultra)	25 meters
Segment C	LVD (Ultra2)	12 meters
	SE (Ultra)	1.5 meters
	HVD (Ultra)	25 meters

In the second example, Figure 1.3, the SYM53C140 is cascaded to achieve four distinct SCSI segments. Segments A and D can be treated as point-to-point segments. Segments B and C are treated as load segments with at least 8 inch spacing between every node. Table 1.3 shows the various distance requirements for each transmission mode.

Figure 1.3 SYM53C140 SCSI Bus Device

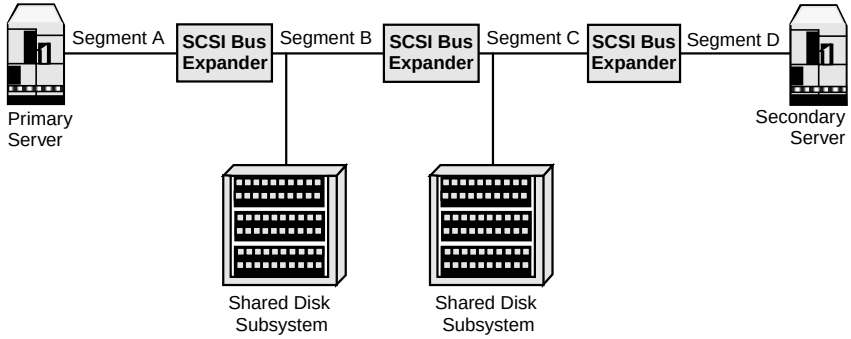


Table 1.3 Transmission Mode Distance Requirements

Segment	Mode	Length Limit
A, D	LVD (Ultra2)	25 meters
	SE (Ultra)	20 meters
	HVD (Ultra)	25 meters
B, C	LVD (Ultra2)	12 meters
	SE (Ultra)	1.5 meters
	HVD (Ultra)	25 meters

1.1.2 Features

- A flexible SCSI bus expander that supports any combination of Low-Voltage Differential (LVD), Single-Ended (SE), or High-Voltage Differential Transceivers (HVD)
- Creates distinct SCSI bus segments that are electrically isolated from each other

- Integrated LVDlink transceivers for direct attachment to either LVD, SE, or HVD bus segments
- Operates as a SCSI Bus Expander
  - LVD to LVD (Ultra2 SCSI)
  - HVD to HVD (Ultra SCSI)
  - SE to SE (Ultra SCSI)
- Operates as a SCSI Bus Converter
  - LVD to HVD (Ultra SCSI)
  - LVD to SE (Ultra SCSI)
  - HVD to SE (Ultra SCSI)
- Targets and initiators may be located on either the A or B Side of the device
- Accepts any asynchronous or synchronous transfer speed up to Ultra2 SCSI (for LVD to LVD mode only)
- Supports dynamic addition/removal of SCSI bus segments via the electrical isolation mode
- Does not consume a SCSI ID
- Propagates the RESET/ signal from one side to the other regardless of the SCSI bus state
- Notifies initiator(s) of changes in transmission mode (SE/LVD/HVD) on A or B side segments via SCSI bus RESET
- SCSI Busy LED driver for activity indicator
- Up to four SYM53C140s may be cascaded
- Completely independent of software

1.1.3 Specifications

- 40 MHz Input Clock
- 160-pin Plastic Quad Flat Pack (PQFP)
- Compliant with the SCSI Parallel Interconnect 2(SPI-2)
- Compliant with SCSI Enhanced Parallel Interface (EPI) Specifications

1.2 Benefits of LVDlink

The SYM53C140 supports Low-Voltage Differential (LVD) technology for SCSI, a signaling technology that increases the reliability of SCSI data transfers over longer distances than those supported by single-ended SCSI technology. The low current output of LVD allows the I/O transceivers to be integrated directly onto the chip. LVD provides the reliability of High-Voltage Differential (HVD) SCSI technology without the added cost of external differential transceivers. LVD allows a longer SCSI cable and more devices on the bus. LVD provides a long-term migration path to even faster SCSI transfer rates without compromising signal integrity, cable length, or connectivity.

For backward compatibility to existing single-ended devices, the SYM53C140 features multimode LVDlink transceivers that can switch between LVD and single-ended modes.

- Integrated LVDlink Multimode transceivers
  - Supports single-ended, LVD, or HVD technology (HVD must have external transceivers)
  - Allows greater device connectivity and longer cable length
  - LVDlink transceivers save the cost of external differential transceivers
  - Supports a long-term performance migration path

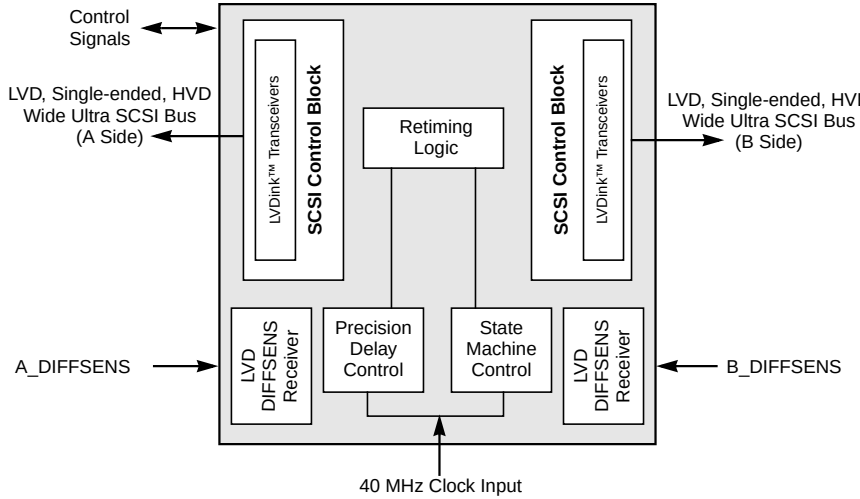
Chapter 2
Functional Descriptions

2.1 Interface Signal Descriptions

The SYM53C140 has no programmable registers, and therefore, no software requirements. SCSI control signals control all SYM53C140 functions. This chapter describes all signals, their groupings and their functions. Figure 2.1 shows a block diagram of the SYM53C140 device divided into the following blocks:

- A Side SCSI Control Block
  - LVD, SE, and HVD Drivers and Receivers
- B Side SCSI Control Block
  - LVD, SE, and HVD Drivers and Receivers
- Retiming Logic
- Precision Delay Control
- State Machine Control

Figure 2.1 SYM53C140 Block Diagram



In its simplest form, the SYM53C140 passes data and parity from a source bus to a load bus. The side asserting, deasserting, or releasing the SCSI signals is the source side. The model of the SYM53C140 is pieces of wire that allow corresponding SCSI signals to flow from one side to the other side. The SYM53C140 needs to know which signals are being driven by another device so it can enable the proper drivers to pass the signals along. In addition, the SYM53C140 does some signal retiming to maintain the signal skew budget from the source bus to the load bus as if the source was a local bus member.

2.1.1 SCSI A Side and B Side Control Blocks

The SCSI A Side pins are connected internally to the corresponding SCSI B Side pins, forming bidirectional connections to the SCSI bus.

In the LVD/LVD mode, the SCSI A Side and B Side control blocks connect to both targets and initiators and accept any asynchronous or synchronous data transfer rates up to the 80 Mbytes/s rate of Wide Ultra2 SCSI. TolerANT® and LVDlink technologies are part of both the A Side and B Side control blocks.

2.1.1.1 SYM53C140 Requirements for Synchronous Negotiation

The SYM53C140 builds a table of information regarding devices on the bus in on-chip RAM. The SDTR and WDTR information for each device is taken from the MSG byte during negotiation. For all devices in the configuration to communicate accurately with each other through the SYM53C140 at Ultra2 (Fast 40) rates, it is necessary for a complete synchronous negatiation to take place between the initatiator(s) and target(s) prior to any data transfer. Otherwise, the SYM53C140 defaults to Fast 20 rates.

2.1.1.2 TolerANT Technology

In the single-ended mode, the SYM53C140 features TolerANT technology, which includes active negation on the SCSI drivers and input signal filtering on the SCSI receivers. Active negation causes the SCSI Request, Acknowledge, Data, and Parity signals to be actively driven HIGH rather than passively pulled up by terminators.

TolerANT receiver technology improves data integrity in unreliable cabling environments, where other devices would be subject to data corruption. TolerANT receivers filter the SCSI bus signals to eliminate unwanted transitions without the long signal delays associated with RC-type input filters. This improved driver and receiver technology helps eliminate double clocking of data, the single biggest reliability issue with SCSI operations.

The benefits of TolerANT technology include increased immunity to noise on the deasserting signal edge, better performance due to balanced duty cycles, and improved SCSI transfer rates. In addition, TolerANT SCSI devices prevent glitches on the SCSI bus at power-up or power-down, so other devices on the bus are also protected from data corruption.

2.1.1.3 LVDlink Technology

To support greater device connectivity and longer SCSI cables, the SYM53C140 features LVDlink technology, the LSI Logic implementation of multimode LVD SCSI. LVDlink transceivers provide the inherent reliability of differential SCSI, and a long-term migration path of faster SCSI transfer rates.

LVDlink technology is based on current drive. Its low output current reduces the power needed to drive the SCSI bus. Therefore, the I/O drivers can be integrated directly onto the chip. This reduces the cost and complexity compared to traditional (high power) differential designs. LVDlink lowers the amplitude of noise reflections and allows higher transmission frequencies.

The LVDlink transceivers in side A and side B operate in the LVD, HVD (external differential transceivers), or single-ended modes. The SYM53C140 automatically detects the type of signal connected, based on the voltages detected by A_DIFFSENS and B_DIFFSENS.

2.1.2 Retiming Logic

The SCSI signals, as they propagate from one side of the SYM53C140 to the other side, are processed by logic circuits that re-time the bus signals, as needed, to guarantee or improve the required SCSI timings. The logic circuitry is governed by the State Machine Controls that keep track of SCSI phases, the location of initiator and target devices, and various timing functions. In addition, the logic circuitry contains numerous delay elements that are periodically calibrated by the Precision Delay Control block in order to guarantee specified timing such as output pulse widths, setup and hold times, and others.

2.1.3 State Machine Control

The State Machine Control keeps track of the SCSI bus phase protocol and other internal operating conditions. This block provides signals to the Retiming Logic that identify how to properly handle SCSI bus signal retiming and protocol, based on observed bus conditions.

2.1.4 Precision Delay Control

The Precision Delay Control block provides calibration information to the precision delay elements in the Retiming Logic block in order to maintain precise timing as signals propagate through the device. As the SYM53C140 operating conditions (such as voltage and temperature) vary over time, the Precision Delay Control block will periodically update the delay settings in the Retiming Logic to maintain constant and precise control over bus timing.

2.1.5 DIFFSENS Receiver

The SYM53C140 contains LVD DIFFSENS Receivers that detect the voltage level on the A Side or B Side DIFFSENS lines to inform the SYM53C140 of the transmission mode being used by the SCSI buses. The LVD DIFFSENS Receivers are capable of detecting the voltage level of incoming SCSI signals to determine whether it is from a single-ended, LVD, or HVD device. A device will not change its present signal driver or receiver mode based on the DIFFSENS voltage levels unless a new mode is sensed continuously for at least 100 ms.

Transmission mode detection for SE, LVD, or HVD is accomplished through the use of the DIFFSENS lines. Table 2.1 shows the voltages on the DIFFSENS lines and modes they will cause.

Table 2.1 DIFFSENS Voltage Levels

Voltage	Mode
-0.35 to +0.5	SE
+0.7 to +1.9	LVD
+2.4 to +5.5	HVD

2.1.6 Dynamic Transmission Mode Changes

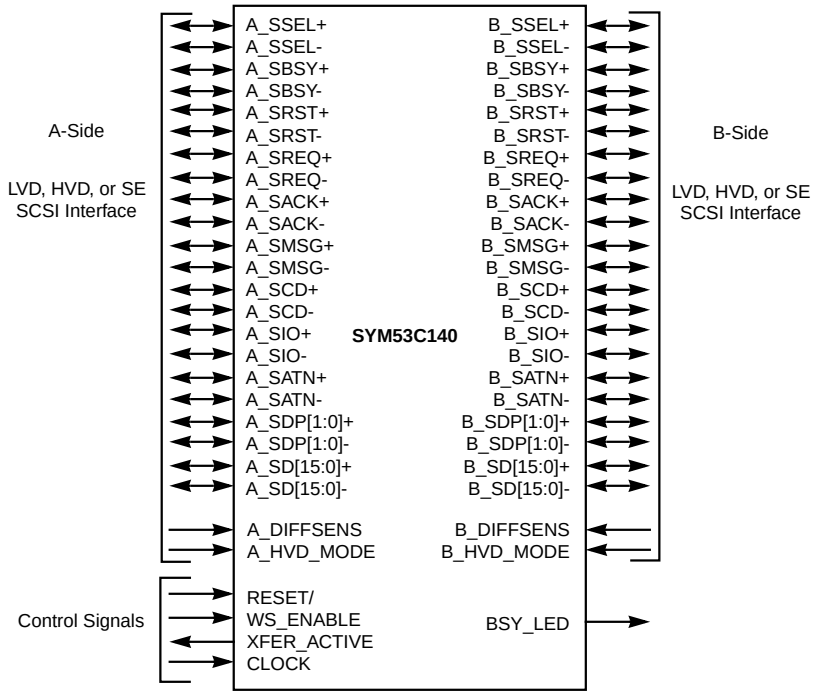
Any dynamic mode change (SE/LVD/HVD) on a bus segment is considered to be a catastrophic event that requires the initiator to determine whether the mode change meets the requirements for that bus segment.

The SYM53C140 supports dynamic transmission mode changes by notifying the initiator(s) of changes in transmission mode (SE/LVD/HVD) on A or B side segments via SCSI bus RESET. The DIFFSENS line is used to detect a valid mode switch on the bus segments. After the DIFFSENS state is present for 100 ms, the SYM53C140 generates a SCSI reset on the opposite bus from the one that the transmission mode change occurred on. This reset is used to inform any initiators residing on the opposite segment about the change in the transmission mode. The initiator(s) will then renegotiate synchronous transfer rates with each device on that segment to ensure that there is a valid bus segment for that mode.

2.1.7 SCSI Signal Descriptions

Figure 2.2 shows the SYM53C140 signal grouping. A description of the signal groups follow. For a description of a specific signal, see Section 3.1, “Signal Descriptions” in Chapter 3. For a signal electrical characteristics, see Section 3.2, “Electrical Characteristics” in Chapter 3. For SCSI bus signal timing, see Section 3.2.4, “SCSI Interface Timing” in Chapter 3.

Figure 2.2 SYM53C140 Signal Grouping



2.1.7.1 Data and Parity (SD and SDP)

The signals named A_SD[15:0] and A_SDP[1:0] are the data and parity signals from the A Side, and B_SD[15:0] and B_SDP[1:0] are the data and parity signals from the B Side of the SYM53C140. These signals are sent and received from the SYM53C140 via SCSI compatible drivers and receiver logic designed into the SYM53C140 interfaces. This logic provides the necessary drive, sense thresholds, and input hysteresis to function correctly in a SCSI bus environment.

The SYM53C140 receives data and parity signals and passes them from the source bus to the load bus and provides any necessary edge shifting to guarantee the skew budget for the load bus. Either side of the SYM53C140 may be the source bus or the load bus. The side that is asserting, deasserting or releasing the SCSI signals is the source side. The following steps describe the SYM53C140 data processing:

1. Asserted data is accepted from the receiver logic as soon as it is received. Once the clock signal has been received, data is gated from the receiver latch.
2. The path is next tested to be sure the data was not driven by the SYM53C140. This is because valid data needs to be generated by another node on the source bus to be passed through the SYM53C140 to the load bus.
3. The data is then leading edge filtered. The assertion edge is held for a specified time to prevent any signal bounce. The duration is controlled by the input signal.
4. The next stage uses a latch to sample the signal. This provides a stable data window for the load bus.
5. The final step develops pull-up and pull-down controls for the SCSI I/O logic, including 3-state controls for the pull-up.
6. A parallel function ensures that bus (transmission line) recovery occurs for a specified time after the last signal deassertion on each signal line.

2.1.7.2 SCSI Bus Activity LED (BSY_LED)

Internal logic is used to detect SCSI bus activity and generate a signal that will produce an active HIGH output. This output can be used to drive a LED to indicate SCSI activity.

The internal circuitry is a digital one shot that is an active HIGH with a minimum pulse width of 16 ms. The BSY_LED output current is 8 mA. This output may have an LED attached to it with the other lead of the LED grounded through a suitable resistor.

2.1.7.3 Busy Control (SBSY)

A_SBSY and B_SBSY signals are propagated from the source bus to the load bus. These signals go through the following process:

1. The bus is tested to be sure the data lines were not driven by the SYM53C140. This is because valid data needs to be generated by another node on the source bus to be passed through the SYM53C140 to the load bus.
2. The data is then leading edge filtered. The assertion edge is held for a specified time to prevent any signal bounce. The duration is controlled by the input signal.
3. The next stage has two modes. One mode simply passes data through. The other mode behaves like a large filter. The mode is selected by the current state in the SYM53C140 State Machine that tracks SCSI phases. The large filter mode is used when the Busy (SBSY) and Select (SSEL) sources switch from side to side. This output is then fed to the output driver which is a pull-down open collector only.
4. A parallel function ensures that bus (transmission line) recovery is available for a specified time after the last signal deassertion on each signal line.

2.1.7.4 Request and Acknowledge Control (SREQ and SACK)

A_SREQ, A_SACK, B_SREQ, and B_SACK are clock and control signals. Their signal paths contain controls to guarantee minimum pulse widths, filter edges, and does some retiming when used as data transfer clocks. SREQ and SACK have paths from the A Side to the B Side and from the B Side to the A Side. The received signal goes through the following processing steps before being sent to the opposite bus:

1. The asserted input signal is sensed and forwarded to the next stage if the direction control permits it. The direction controls are developed from state machines that are driven by the sequence of bus control signals.
2. The signal must then pass the test of not being generated by the SYM53C140.
3. In the A Side to B Side direction, the next stage is a leading edge filter. This ensures that the output will not switch during the specified hold time after the leading edge. The duration of the input signal determines the duration of the output after the hold time. In the B Side to A Side direction, the circuit guarantees a minimum pulse width.

4. The next stage passes the signal if it is not a data clock. If SREQ or SACK is a data clock, it delays the leading edge to improve data output setup times. The duration is again controlled by the input signal.
5. The following stage is a trailing edge signal filter. When the signal deasserts, the filter will not permit any signal bounce. The output signal deasserts at the first deasserted edge of the input signal.
6. The last stage develops pull-up and pull-down signals with drive and 3-state control.
7. A parallel function ensures that bus (transmission line) recovery occurs for a specified time after the last signal deassertion on each signal line.

2.1.7.5 Reset Control (SRST)

A_SRST and B_SRST are also passed from the source to the load bus. This output has pull-down control for an open collector driver. These reset signals are processed using the following steps:

1. The input signal is blocked if it is already being driven by the SYM53C140.
2. The next stage is a leading edge filter. This ensures that the output will not switch during a specified time after the leading edge. The duration of the input signal then determines the duration of the output.
3. A parallel function ensures that bus (transmission line) recovery occurs for a specified time after the last signal deassertion on each signal line.

2.1.7.6 Control/Data, Input/Output, Message, and Attention Controls (SCD, SIO, SMSG, and SATN)

A_SCD, A_SIO, A_SMSG, A_SATN, B_SCD, B_SIO, B_SMSG and B_SATN are control signals that have the following processing steps:

1. The input signal is blocked if it is being driven by the SYM53C140.
2. The next stage is a leading edge filter. This ensures the output will not switch for a specified time after the leading edge. The duration of the input signal determines the duration of the output.

3. The final stage develops pull-up and pull-down controls for the SCSI I/O logic, including 3-state controls for the pull-up.
4. A parallel function ensures that bus (transmission line) recovery is for a specified time after the last signal deassertion on each signal line.

2.1.7.7 Select Control (SSEL)

A_SSEL and B_SSEL are control signals used during bus arbitration and selection. Whichever side asserts, SSEL propagates it to the other side. If both signals are asserted at the same time, the A Side receives SSEL and sends it to the B Side. This output has pull-down control for an open collector driver. The signal goes through the following processing steps:

1. The input signal is blocked if it is being driven by the SYM53C140.
2. The next stage is a leading edge filter. This ensures that the output will not switch for a specified time after the leading edge. The duration of the input signal then determines the duration of the output.
3. A parallel function ensures that bus (transmission line) recovery occurs for a specified time after the last signal deassertion on each signal line.

2.1.7.8 Differential Direction Controls

A_SD[15:0], A_SDP[1:0], A_SBSY, A_SSEL, A_SCD, A_SIO, A_SMSG, A_SREQ, A_SACK, A_SATN, A_SRST, B_SD[15:0], B_SDP[1:0], B_SBSY, B_SSEL, B_SCD, B_SIO, B_SMSG, B_SREQ, B_SACK, B_SATN, and B_SRST are all multimode signals. The mode is controlled by the HVD_MODE input pins and the voltage is sensed at the DIFFSENS inputs.

When High-Voltage Differential signaling is selected and the DIFFSENS line sees the proper voltage input, all the minus signal leads become single-ended inputs/outputs to HVD drivers/receivers. All plus signals

become the HVD driver/receiver direction control signals. The A and B Sides are independently controlled.

Table 2.2 Direction Control Signal Polarities

Signal Level	State	Effect
LOW = 0	Deasserted	Input signals into the SYM53C140
HIGH = 1	Asserted	Drive the SYM53C140 signals onto the bus

When the single-ended mode is selected by the lack of HVD_MODE and the correct DIFFSENS voltage, the plus signal leads are internally tied to ground and the minus SCSI signals become the single-ended input/outputs.

When the Low-Voltage Differential mode is selected by the lack of HVD_MODE and the correct DIFFSENS voltage, the plus and minus signal leads are differential signal pairs.

2.1.7.9 Clock (CLOCK)

This is the 40 MHz oscillator input to the SYM53C140. It is the clock source for the protocol control state machines and timing generation logic. This clock is not used in any bus signal transfer paths.

2.1.7.10 A and B High-Voltage Differential Mode (A_HVD_MODE and B_HVD_MODE)

These inputs inform the SYM53C140 that external drivers and receivers are used in this particular application. The effect of this control is to disable the LVD and single-ended modes of operation from the corresponding port.

Table 2.3 HVD_MODE Control Signal Polarity

Signal Level	State	Effect
LOW = 0	Deasserted	SYM53C140 drivers function in single-ended or LVD mode.
HIGH = 1	Asserted	High-Voltage Differential Signals and Controls are enabled from the port.

2.1.7.11 Chip Reset (RESET/)

This general purpose chip reset is intended to force all of the internal elements of the SYM53C140 into a known state. It will bring the State Machine to an idle state and force all controls to a passive state. The minimum RESET/ input asserted pulse width is 100 ns.

The SYM53C140 also contains an internal Power On Reset (POR) function that is ORed with the chip reset pin. This eliminates the need for an external chip reset.

Table 2.4 RESET/ Control Signal Polarity

Signal Level	State	Effect
LOW = 0	Asserted	Reset is forced to all internal SYM53C140 elements.
HIGH = 1	Deasserted	SYM53C140 is not in a forced reset state.

2.1.7.12 A and B Differential Sense (A_DIFFSENS and B_DIFFSENS)

These control pins are used to determine the mode of SCSI bus signaling that will be expected.

Table 2.5 Mode Sense Control Voltage Levels

Voltage	Mode
-0.35 to +0.5	SE
+0.7 to +1.9	LVD
+2.4 to +5.5	HVD

For example, if a differential source is plugged into the B Side that has been configured to run in the differential mode and if a single-ended source is detected, then the B Side is disabled and no B Side signals will be driven. This is a protection mechanism for single-ended interfaces that are connected to differential drivers.

2.1.7.13 Warm Swap Enable (WS_ENABLE)

This input is used to remove the chip from an active bus without disturbing the current SCSI transaction (for Warm Swap). When asserted

LOW, the chip will wait until the next SCSI Bus Free state, then reset internally. Once reset, all SCSI activity will be ignored until the WS_ENABLE pin is deasserted HIGH and both SCSI busses enter the Bus Free state. As an indication that the chip is idle, or ready to be warm swapped, the XFER_ACTIVE signal will deassert LOW. An LED or some other indicator could be connected to the XFER_ACTIVE signal.

Table 2.6 WS_ENABLE Signal Polarity

Signal Level	State	Effect
HIGH = 1	Asserted	The SYM53C140 performs normal transfers through the device
LOW = 0	Deasserted	The SYM53C140 discontinues transfers through the device (off-line) upon detection of a SCSI Bus Fee state

2.1.7.14 Transfer Active (XFER_ACTIVE)

This output is an indication that the chip has finished its internal testing, the SCSI bus has entered a Bus Free state, and SCSI traffic can now pass from one bus to the other. The signal is asserted HIGH when the chip is active.

Table 2.7 XFER_ACTIVE Signal Polarity

Signal Level	State	Effect
HIGH = 1	Asserted	Indicates normal operation, transfers through the SYM53C140 are enabled
LOW = 0	Deasserted	The SYM53C140 has detected a Bus Free state do to WS_ENABLE being low disabling transfers through the device

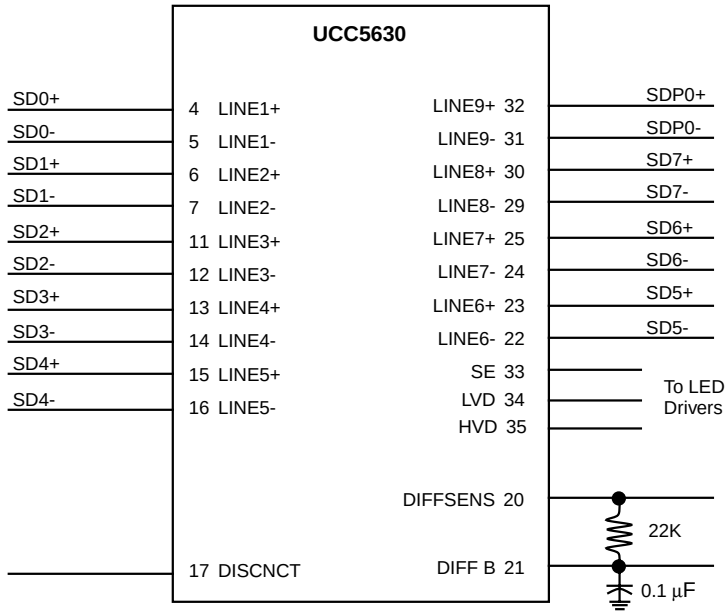
2.1.8 SCSI Termination

The terminator networks provide the biasing needed to pull signals to an inactive voltage level, and to match the impedance seen at the end of the cable with the characteristic impedance of the cable. Terminators must be installed at the extreme ends of each SCSI segment, and only at the ends. No SCSI segment should ever have more or less than two terminators installed and active. SCSI host adapters should provide a

means of accommodating terminators. The terminators should be socketed, so they may be removed if not needed. Or, there should be a means of disabling them with software.

Multi-mode terminators are required because they provide both LVD and single-ended termination, depending on what mode of operation is detected by the DIFFSENS pins. HVD requires a different termination configuration. The use of active termination is highly recommended.

Figure 2.3 SCSI Termination



DIFFSENS connects to the SCSI bus DIFFSENS line to detect what type of devices (single-ended, LVD, or high-voltage differential) are connected to the SCSI bus. DISCNCT shuts down the terminator when it is not at the end of the bus. The disconnect pin low enables the terminator.
*Use additional UCC5630 terminators to terminate the SCSI control signals and wide SCSI data byte as needed.

Chapter 3
Specifications

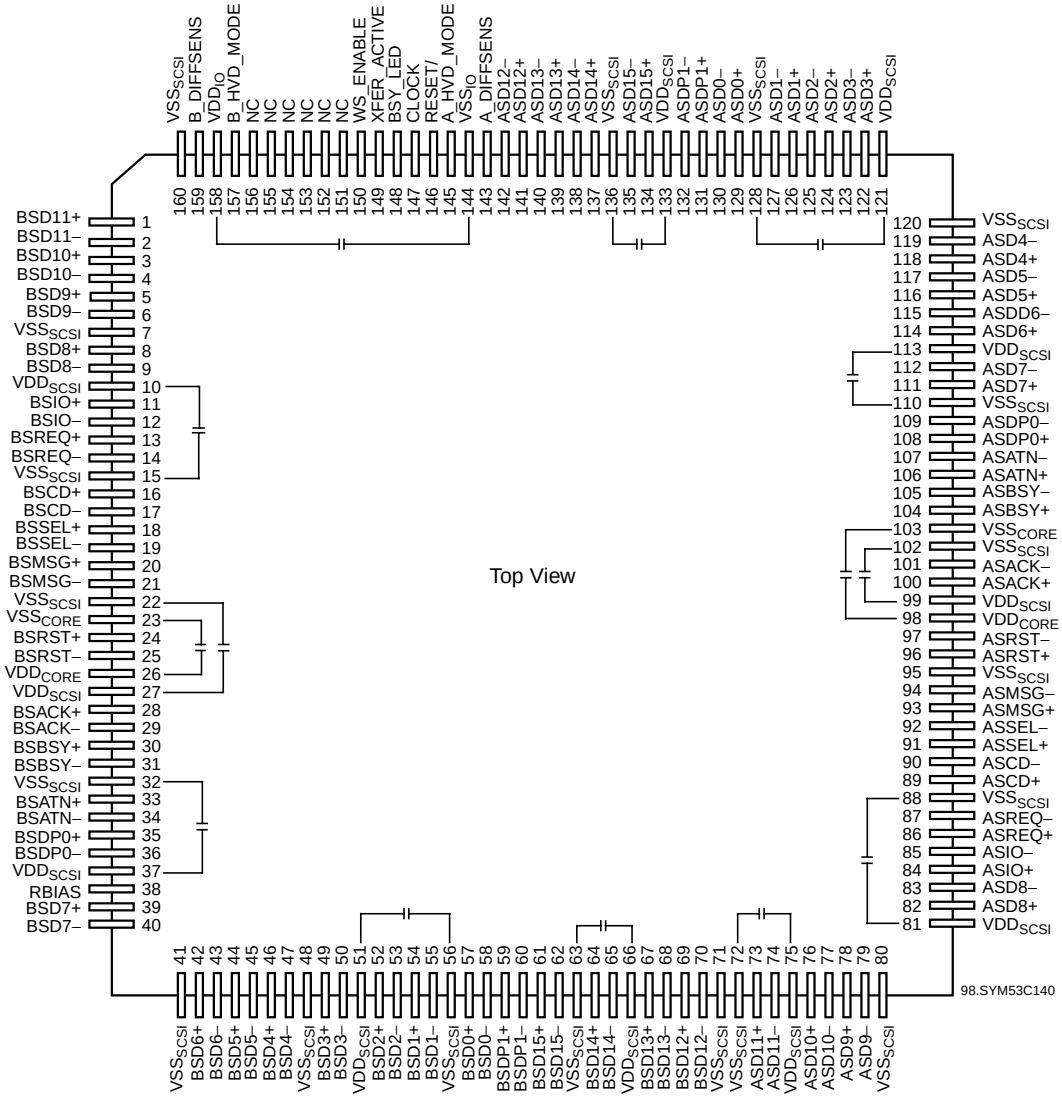
3.1 Signal Descriptions

The SYM53C140 is packaged in a 160-pin Plastic Quad Flat Pack (PQFP) shown in Figure 3.1. The SYM53C140 signal grouping is shown in Figure 3.2 and Tables 3.1 through 3.4 list the signal descriptions grouped by function:

- SCSI A Side Interface Pins (Table 3.1)
- SCSI B Side Interface Pins (Table 3.2)
- Chip Interface Control Pins (Table 3.3)
- Power and Ground Pins (Table 3.4)

The decoupling capacitor arrangement shown below is recommended to maximize the benefits of the internal split ground system. Capacitor values should be between 0.01 F and 0.1 F.

Figure 3.1 SYM53C140 160-pin PQFP Pin Diagram



1. *NC* pins are not connected.

Figure 3.2 SYM53C140 Functional Signal Grouping

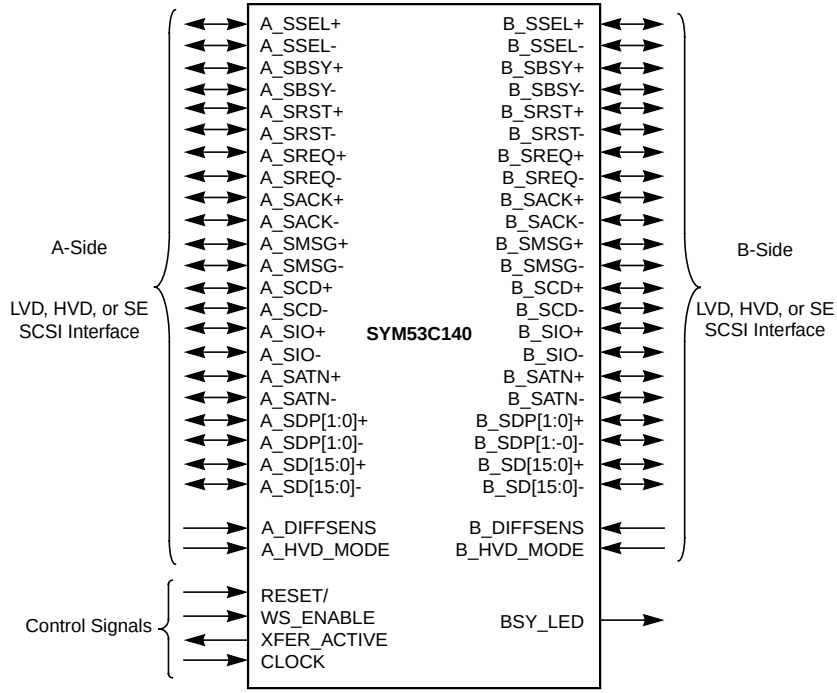


Table 3.1 SCSI A Side Interface Pins

SCSI A	Pin	Type	Description
A_SSEL+,-	91, 92	I/O	A Side SCSI bus Select control signal.
A_SBSY+,-	104, 105	I/O	A Side SCSI bus Busy control signal.
A_SRST+,-	96, 97	I/O	A Side SCSI bus Reset control signal.
A_SREQ+,-	86, 87	I/O	A Side SCSI bus Request control signal.
A_SACK+,-	100, 101	I/O	A Side SCSI bus Acknowledge control signal.
A_SMSG+,-	93, 94	I/O	A Side SCSI bus Message control signal.
A_SCD+,-	89, 90	I/O	A Side SCSI bus Control and Data control signal.
A_SIO+,-	84, 85	I/O	A Side SCSI bus Input and Output control signal.
A_SATN+,-	106, 107	I/O	A Side SCSI bus Attention control signal.
A_SDP[1:0]+,-	108, 109, 131, 132	I/O	A Side SCSI bus Data Parity signal.
A_SD[15:0]+,-	73, 74, 76–79, 82, 83, 111, 112, 114–119, 122–127, 129, 130, 134, 135, 137–142	I/O	A Side SCSI bus Data signals.
A_DIFFSENS	143	I	A Side SCSI bus Differential Sense signal.
A_HVD_MODE	145	I	A Side SCSI bus HVD Mode control signal.

Table 3.2 SCSI B Side Interface Pins

SCSI B	Pin	Type	Description
B_SSEL+,-	18, 19	I/O	B Side SCSI bus Select control signal.
B_SBSY+,-	30, 31	I/O	B Side SCSI bus Busy control signal.
B_SRST+,-	24, 25	I/O	B Side SCSI bus Reset control signal.
B_SREQ+,-	13, 14	I/O	B Side SCSI bus Request control signal.
B_SACK+,-	28, 29	I/O	B Side SCSI bus Acknowledge control signal.
B_SMSG+,-	20, 21	I/O	B Side SCSI bus Message control signal.
B_SCD+,-	16, 17	I/O	B Side SCSI bus Control and Data control signal.
B_SIO+,-	11, 12	I/O	B Side SCSI bus Input and Output control signal.
B_SATN+,-	33, 34	I/O	B Side SCSI bus Attention control signal.
B_SDP[1:0]+,-	59, 60, 35, 36	I/O	B Side SCSI bus Data Parity signal.
B_SD[15:0]+,-	1-6, 8, 9, 39, 40, 42–47, 49, 50, 52–55, 57, 58, 61, 62, 64, 65, 67–70,	I/O	B Side SCSI bus Data signals.
B_DIFFSENS	159	I	B Side SCSI bus Differential Sense signal.
B_HVD_MODE	157	I	B Side SCSI bus HVD Mode control signal.

Table 3.3 Chip Interface Control Pins

Control	Pin	Type	Description
RESET/	146	I	Master Reset for SYM53C140, active LOW.
WS_ENABLE	150	I/O	Enable/disable SCSI transfers through the SYM53C140.
XFER_ACTIVE	149	I/O	Transfers through the SYM53C140 are enabled/disabled.
CLOCK	147	I	Oscillator input for SYM53C140 (40 MHz).
BSY_LED	148	O	SCSI activity LED output, 8 mA.

Table 3.4 Power and Ground Pins

Power and Ground	Pin	Type	Description
VDD_{SCSI}	10, 27, 37, 51, 66, 75, 81, 99, 113, 121, 133	I	Power supplies to the SCSI bus I/O pins.
VSS_{SCSI}	7, 15, 22, 32, 41, 48, 56, 63, 71, 72, 80, 88, 95, 102, 110, 120, 128, 136, 160	I	Ground for the SCSI bus I/O pins.
VDD_{CORE}	26, 98	I	Power supplies to the CORE logic.
VSS_{CORE}	23, 103	I	Ground for the CORE logic.
VDD_{IO}	158	I	Power supplies to the I/O logic.
VSS_{IO}	144	I	Ground for the I/O logic.
RBIAS	38	I	Receiver bias control, R = 9.76 KΩ 1%.
NC	151–156	N/A	No Connections.

Note:
- All V_{DD} pins must be supplied 3.3 V. The SYM53C140 output signals drive 3.3 V.
- If the power supplies to the VDD_{IO} and VDD_{CORE} pins in a chip testing environment are separated, either power up the pins simultaneously or power up VDD_{CORE} before VDD_{IO}. The VDD_{IO} pin must always power down before the VDD_{CORE} pin.

3.2 Electrical Characteristics

This section specifies the DC and AC electrical characteristics of the SYM53C140. These electrical characteristics are in the following four categories:

- DC Characteristics
- TolerANT Technology Electrical Characteristics
- AC Characteristics
- SCSI Interface Timing

3.2.1 DC Characteristics

Table 3.5 Absolute Maximum Stress Ratings[1]

Symbol	Parameter	Min	Max	Unit	Test Conditions
T_{STG}	Storage temperature	-55	150	°C	–
V_{DD}	Supply voltage	-0.5	4.5	V	–
V_{IN}	Input Voltage	V_{SS} - 0.3	V_{DD} + 0.3	V	–
I_{LP}[2]	Latch-up current	± 150	–	mA	–
ESD	Electrostatic discharge	–	2K	V	MIL-STD 883C, Method 3015.7

1. Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the Operating Conditions section of the manual is not implied.
2. -2 V < VPIN < 8 V.

Table 3.6 Operating Conditions[1]

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{DD}	Supply voltage	3.13	3.47	V	–
I_{DD}	Supply current (dynamic SE)	–	130	mA	–
	Supply current (dynamic LVD)	–	600	mA	RBIAS = 9.76 KΩ 1% V_{DD} = 3.3 V
	Supply current (static)	–	1	mA	–
T_A	Operating free air	0	70	˚C	–
θ_{JA}	Thermal resistance (junction to ambient air)	–	35	˚C/ W	–

1. Conditions that exceed the operating limits may cause the device to function incorrectly.

Table 3.7 LVD Driver SCSI Signals — B_SD[15:0], B_SDP[1:0], B_SCD, B_SIO, B_SMSG, B_SREQ, B_SACK, B_SBSY, B_SATN, B_SSEL, B_SRST[1]

Symbol	Parameter	Min	Max	Units	Test Conditions
I_O+	Source (+) current	7	12	mA	Asserted state
I_O-	Sink (-) current	-7	-12	mA	Asserted state
I_O+	Source (+) current	-3.5	-6	mA	Negated state
I_O-	Sink (-) current	3.5	6	mA	Negated state
I_{OZ}	3-state leakage	-20	20	µA	–

1. V_{CM} = 0.7 - 1.8 V, R_L = 0 - 110 Ω, R_{bias} = 9.76 KΩ.

Figure 3.3 LVD Driver

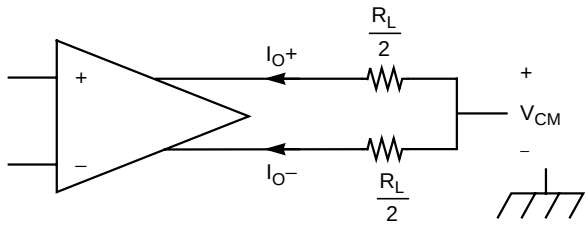


Table 3.8 LVD Receiver SCSI Signals — B_SD[15:0], B_SDP[1:0] , B_SCD, B_SIO, B_SMSG, B_SREQ, B_SACK, B_SBSY, B_SATN, B_SSEL, B_SRST[1]

Symbol	Parameter	Min	Max	Units	Test Conditions
V_I	LVD receiver voltage asserting	60	–	mV	–
V_I	LVD receiver voltage negating	–	-60	mV	–

1. V_{CM} = 0.7 - 1.8 V

Figure 3.4 LVD Receiver

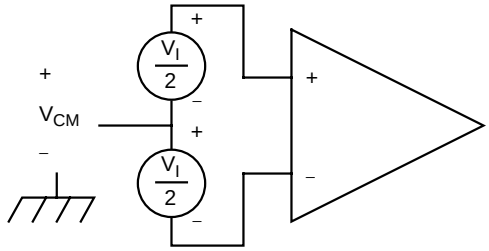


Table 3.9 DIFFSENS SCSI Signal

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	High-voltage differential sense voltage	2.4	V_{DD} + 0.3	V	–
V_S	LVD sense voltage	0.7	1.9	V	–
V_{IL}	Single-ended sense voltage	V_{SS} -0.3	0.5	V	–
I_{OZ}	3-state leakage	-10	10	µA	–

Table 3.10 Input Capacitance

Symbol	Parameter	Min	Max	Unit	Test Conditions
C_I	Input capacitance of input pads	–	7	pF	–
C_{IO}	Input capacitance of I/O pads	–	10	pF	–

Table 3.11 Bidirectional SCSI Signals — A_SD[15:0]/, A_SDP[1:0]/, A_SREQ/, A_SACK/, B_SD[15:0], B_SDP[1:0], B_SREQ, B_SACK

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	1.9	V_{DD}	V	–
V_{IL}	Input low voltage	V_{SS}	1.0	V	–
V_{OH}[1]	Output high voltage	2.0	V_{DD}	V	I_{OH} = 7.0 mA
V_{OL}	Output low voltage	V_{SS}	0.5	V	48 mA
I_{OZ}	3-state leakage	-10	10	µA	–

1. TolerANT active negation enabled.

Table 3.12 Bidirectional SCSI Signals — A_SCD/, A_SIO/, A_SMSG/, A_SBSY/, A_SATN/, A_SSEL/, A_SRST/, B_SCD, B_SIO, B_SMSG, B_SBSY, B_SATN, B_SSEL, B_SRST

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	1.9	V_{DD}	V	–
V_{IL}	Input low voltage	V_{SS}	1.0	V	–
V_{OL}	Output low voltage	V_{SS}	0.5	V	48 mA
I_{OZ}	3-state leakage	-10	10	µA	–

Table 3.13 Input Control Signals — CLOCK, RESET/, WS_ENABLE

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	V_{DD}	V	–
V_{IL}	Input low voltage	V_{SS}	0.8	V	–
I_{OZ}	3-state leakage	-10	10	µA	–

Figure 3.5 External Reset Circuit

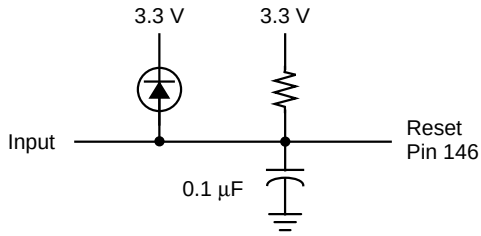


Table 3.14 Output Control Signals — BSY_LED, XFER_ACTIVE

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{OH}	Output high voltage	2.4	V_{DD}	V	8 mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	8 mA
I_{OZ}	3-state leakage	–10	10	µA	–

3.2.2 TolerANT Technology Electrical Characteristics

Table 3.15 TolerANT Technology Electrical Characteristics[1]

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{OH}[2]	Output high voltage	2.0	V_{DD} + 0.3	V	I_{OH} = 7 mA
V_{OL}	Output low voltage	V_{SS}	0.5	V	I_{OL} = 48 mA
V_{IH}	Input high voltage	2.0	V_{DD} + 0.3	V	–
V_{IL}	Input low voltage	V_{SS} – 0.3	0.8	V	Referenced to V_{SS}
V_{IK}	Input clamp voltage	–0.66	–0.77	V	V_{DD} = 4.75; I_I = –20 mA
V_{TH}	Threshold, HIGH to LOW	1.0	1.2	V	–
V_{TL}	Threshold, LOW to HIGH	1.4	1.6	V	–
V_{TH}-V_{TL}	Hysteresis	300	500	mV	–
I_{OH}[2]	Output high current	2.5	24	mA	V_{OH} = 2.5 V

(Sheet 1 of 2)

Table 3.15 TolerANT Technology Electrical Characteristics[1] (Cont.)

Symbol	Parameter	Min	Max	Units	Test Conditions
I_{OL}	Output low current	100	200	mA	V_{OL} = 0.5 V
I_{OSH}[2]	Short-circuit output high current	–	625	mA	Output driving low, pin shorted to V_{DD} supply[3]
I_{OSL}	Short-circuit output low current	–	95	mA	Output driving high, pin shorted to V_{SS} supply
I_{LH}	Input high leakage	–	20	µA	$-0.5<V_{DD}<V_{DD}$ 5 Max $V_{PIN} = V_{DD}3$
I_{LL}	Input low leakage	–	–20	µA	$-0.5<V_{DD}<V_{DD}$ 5 Max V_{PIN} = 0 V
R_I	Input resistance	20	–	MΩ	SCSI pins[4]
C_P	Capacitance per pin	–	15	pF	PQFP
t_R[2]	Rise time, 10% to 90%	4.0	18.5	ns	Figure 3.6
t_F	Fall time, 90% to 10%	4.0	18.5	ns	Figure 3.6
dV_H/dt	Slew rate, LOW to HIGH	0.15	0.50	V/ns	Figure 3.6
dV_L/dt	Slew rate, HIGH to LOW	0.15	0.50	V/ns	Figure 3.6
ESD	Electrostatic discharge	2	–	KV	MIL-STD-883C; 3015-7
	Latch-up	100	–	mA	–
	Filter delay	20	30	ns	Figure 3.7
	Ultra filter delay	10	15	ns	Figure 3.7
	Ultra2 filter delay	5	8	ns	Figure 3.7
	Extended filter delay	40	60	ns	Figure 3.7

(Sheet 2 of 2)

1. These values are guaranteed by periodic characterization; they are not 100% tested on every device.
2. Active negation outputs only: Data, Parity, SREQ/, SACK/. (Minus Pins) SCSI mode only.
3. Single pin only; irreversible damage may occur if sustained for one second.
4. SCSI RESET pin has 10 kΩ pull-up resistor.

Figure 3.6 Rise and Fall Time Test Conditions

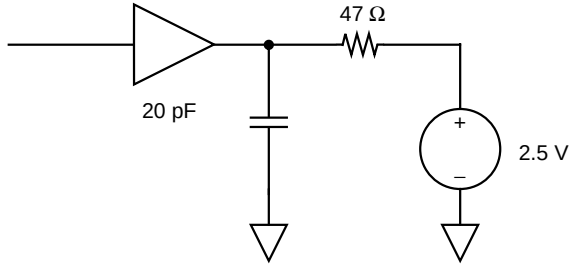
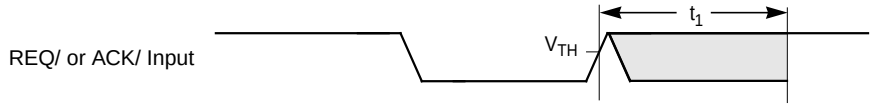


Figure 3.7 SCSI Input Filtering



Note: t_1 is the input filtering period.

Figure 3.8 Hysteresis of SCSI Receivers

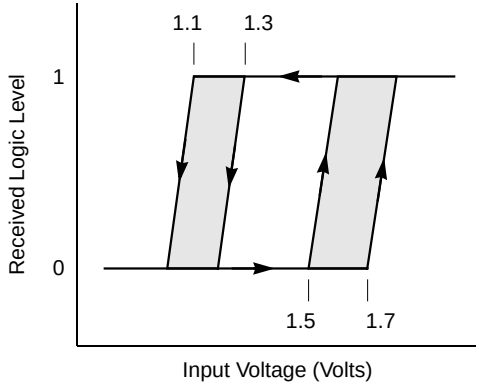


Figure 3.9 Input Current as a Function of Input Voltage

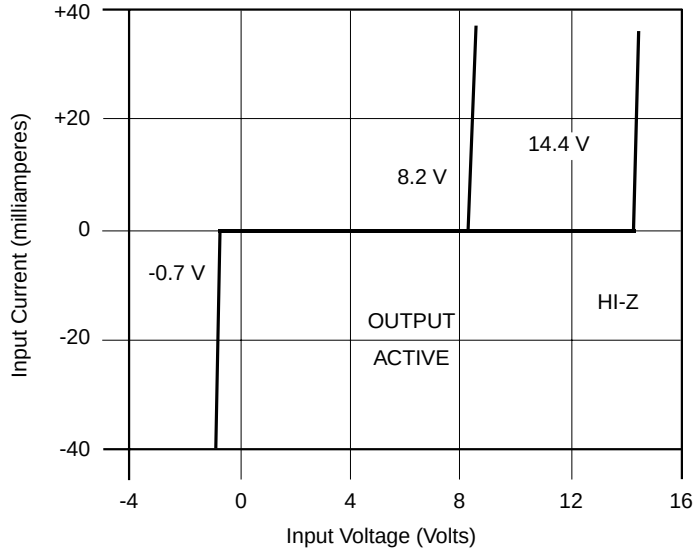
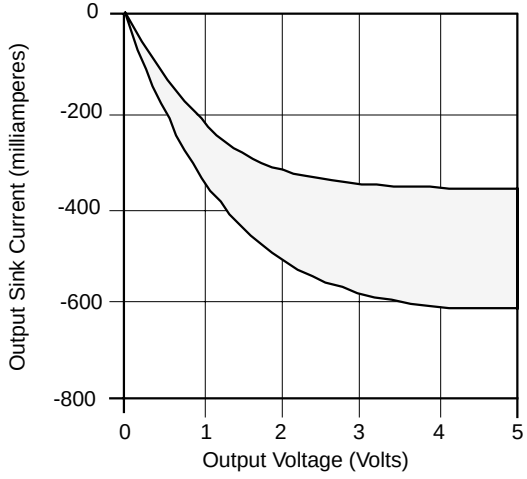
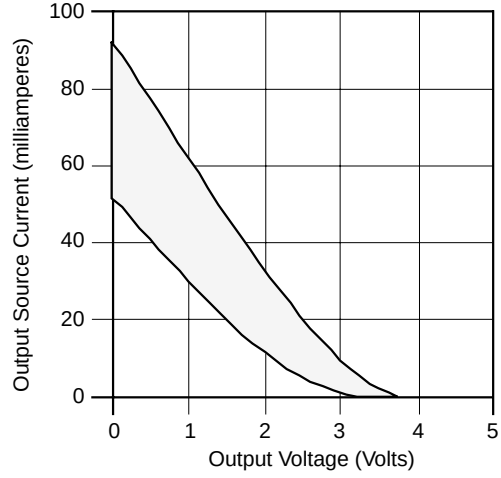


Figure 3.10 Output Current as a Function of Output Voltage





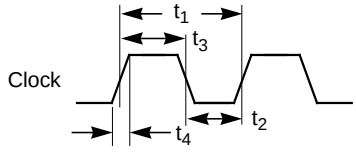
3.2.3 AC Characteristics

The AC characteristics described in this section apply over the entire range of operating conditions (refer to DC Characteristics in this chapter). Chip timing is based on simulation at worst case voltage, temperature, and processing. The SYM53C140 requires a 40 MHz clock input.

Table 3.16 Clock Timing

Symbol	Parameter	Min	Max	Units
t_1	Clock period	24.75	25.25	ns
t_2	Clock low time	10	15	ns
t_3	Clock high time	10	15	ns
t_4	Clock rise time	1	–	V/ns

Figure 3.11 Clock Timing



3.2.4 SCSI Interface Timing

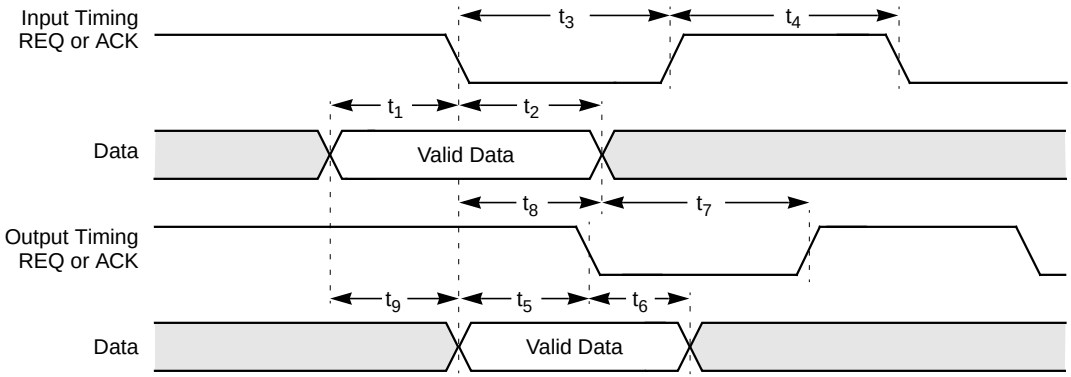
Table 3.17 Input Timing

Symbol	Parameter	Min	Max	Units
t_1	Input data setup	1	–	ns
t_2	Input data hold	4.75	–	ns
t_3	Input REQ/ACK assertion pulse width	11	–	ns
t_4	Input REQ/ACK deassertion pulse width	11	–	ns

Table 3.18 Output Timing

Symbol	Parameter	Min	Max	Units
t_5	Output data setup	min [t_1 + 17ns, t_4+5]	–	ns
t_6	Output data hold	max [24, (t_2 - 20), t_3]	–	ns
t_7	Output REQ/ACK pulse width	max [20 ns, t_3 -5]	max [30 ns, t_3 +5]	ns
t_8	REQ/ACK transport delay	25 ns if REQ/ACK is clock for input data, 10 ns if not	50 ns if REQ/ACK is clock for input data, 30 ns if not	ns
t_9	Data transport delay	6	[t_3 +35]	ns

Figure 3.12 Input/Output Timing



3.3 Mechanical Drawings

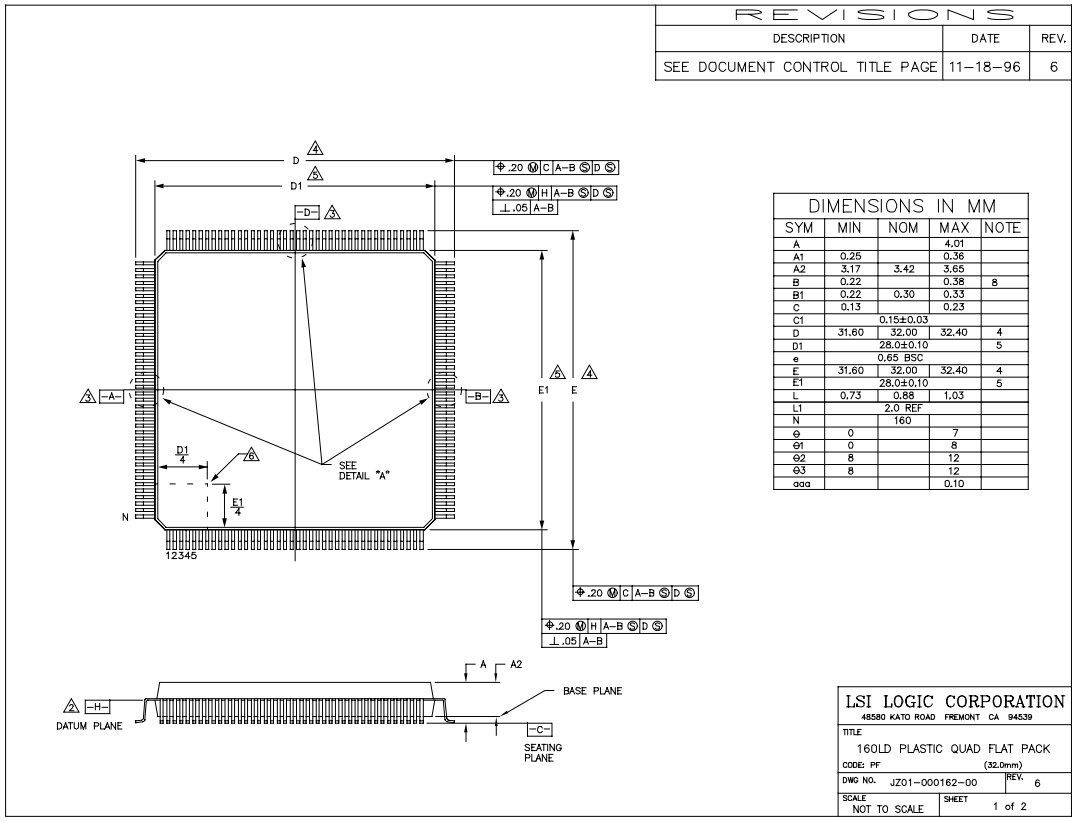
LSI Logic component dimensions conform to a current revision of the JEDEC Publication 95 standard package outline, using ANSI 14.5Y “Dimensioning and Tolerancing” interpretations. As JEDEC drawings are balloted and updated, changes may have occurred. To ensure the use of a current drawing, the JEDEC drawing revision level should be verified. Visit www.eia.org/jedec for review of Publication 95 drawings and revision levels.

For printed circuit board land patterns that will accept LSI Logic components, it is recommended that customers refer to the IPC standards (Institute for Interconnecting and Packaging Electronic Circuits). Specification number IPC-SM-782, “Surface Mount Design and Land Pattern Standard” is an established method of designing land patterns. Feature size and tolerances are industry standards based on IPC assumptions.

3.3.1 SYM53C140 160-pin PQFP Mechanical Drawing

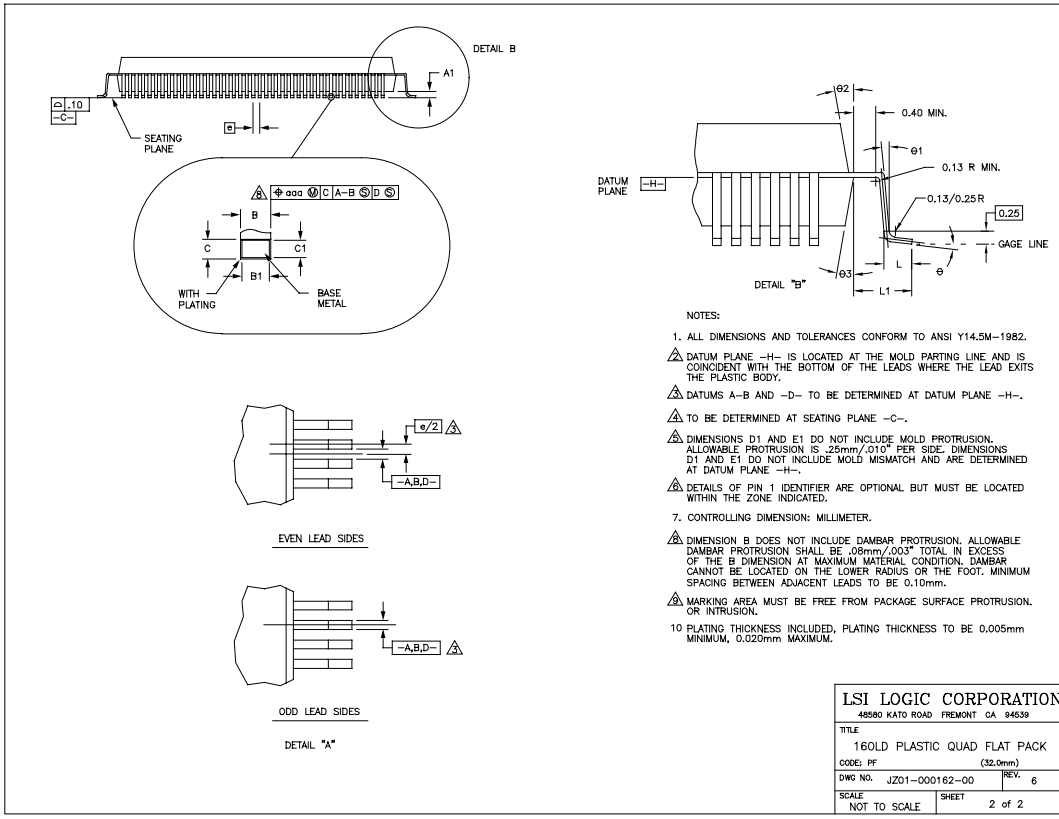
The SYM53C140 is packaged in a 160-pin metric Plastic Quad Flat Pack (PQFP).

Figure 3.13 SYM53C140 160 Pin PQFP (PF) Mechanical Drawing



Important: **This drawing may not be the latest version. For board layout and manufacturing, obtain the most recent engineering drawings from your LSI Logic marketing representative by requesting the outline drawing for package code PF.**

Figure 3.13 SYM53C140 Pin 160 PQFP (PF) Mechanical Drawing (Cont.)



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Appendix A
Wiring Diagrams

A.1 SYM53C140 Wiring Diagrams

The following four pages of wiring diagrams are of a typical SYM53C140 in a evaluation test board application.

Figure A.1 SYM53C140 Wiring Diagram 1 of 4

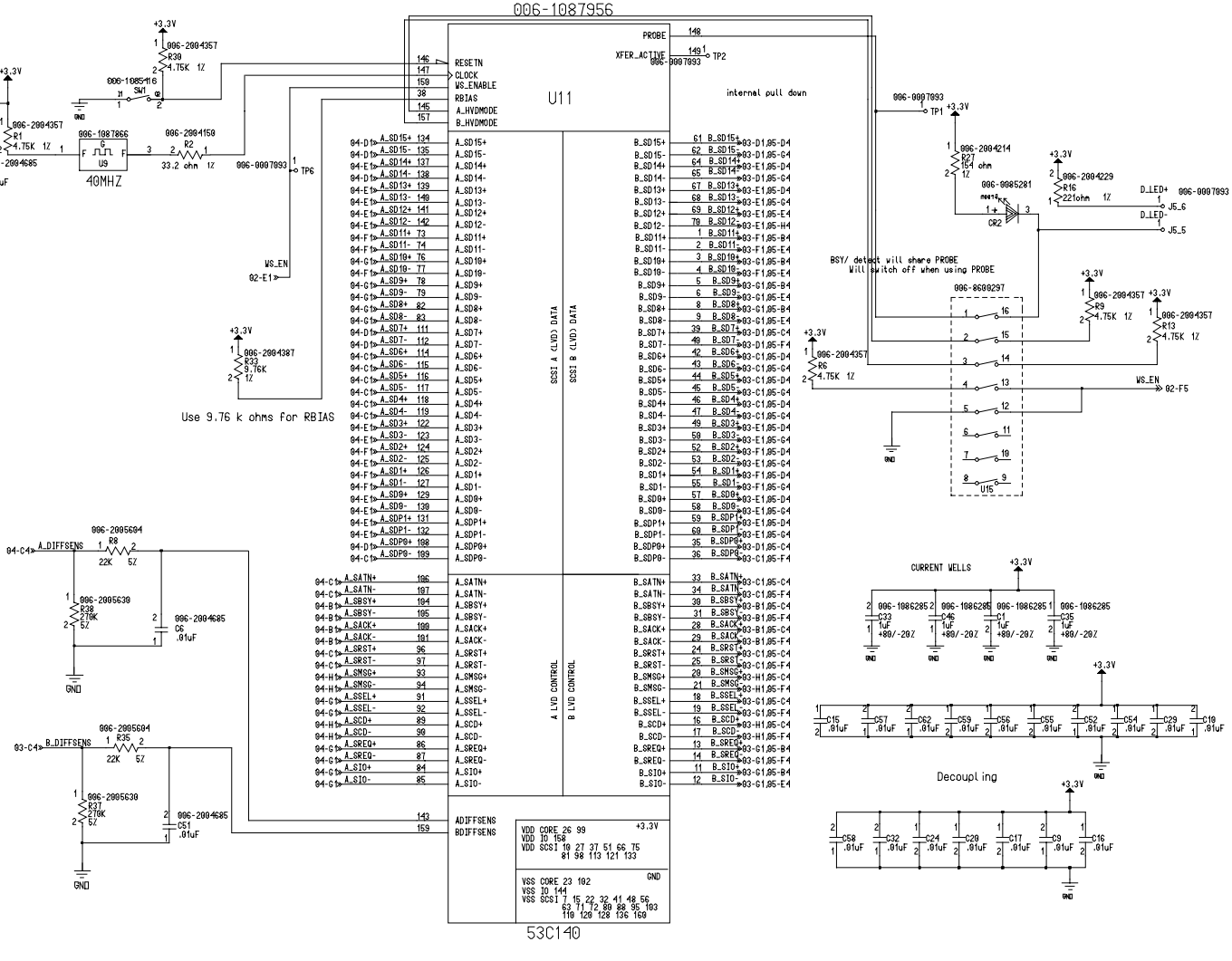


Figure A.1 SYM53C140 Wiring Diagram 2 of 4

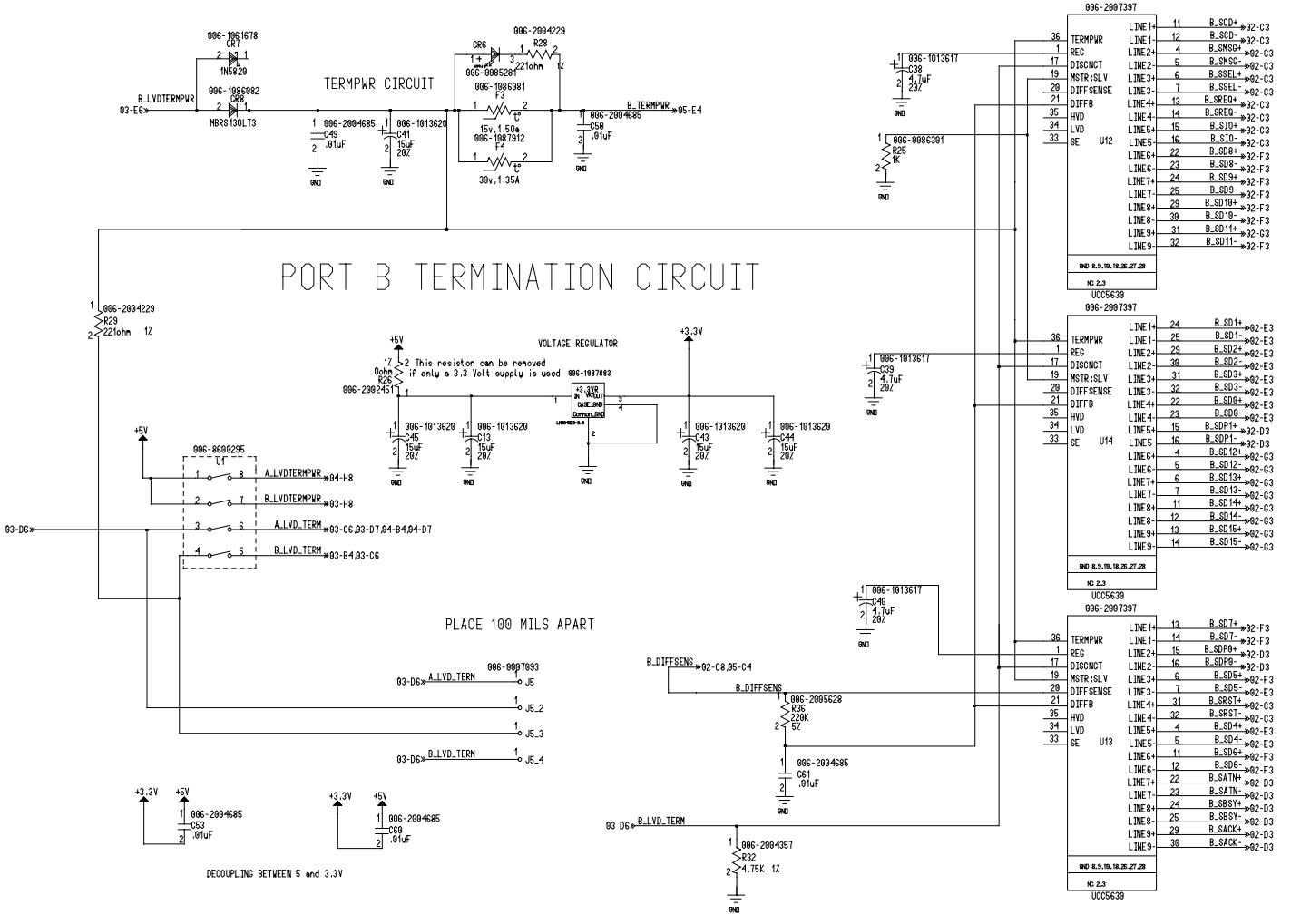


Figure A.1 SYM53C140 Wiring Diagram 3 of 4

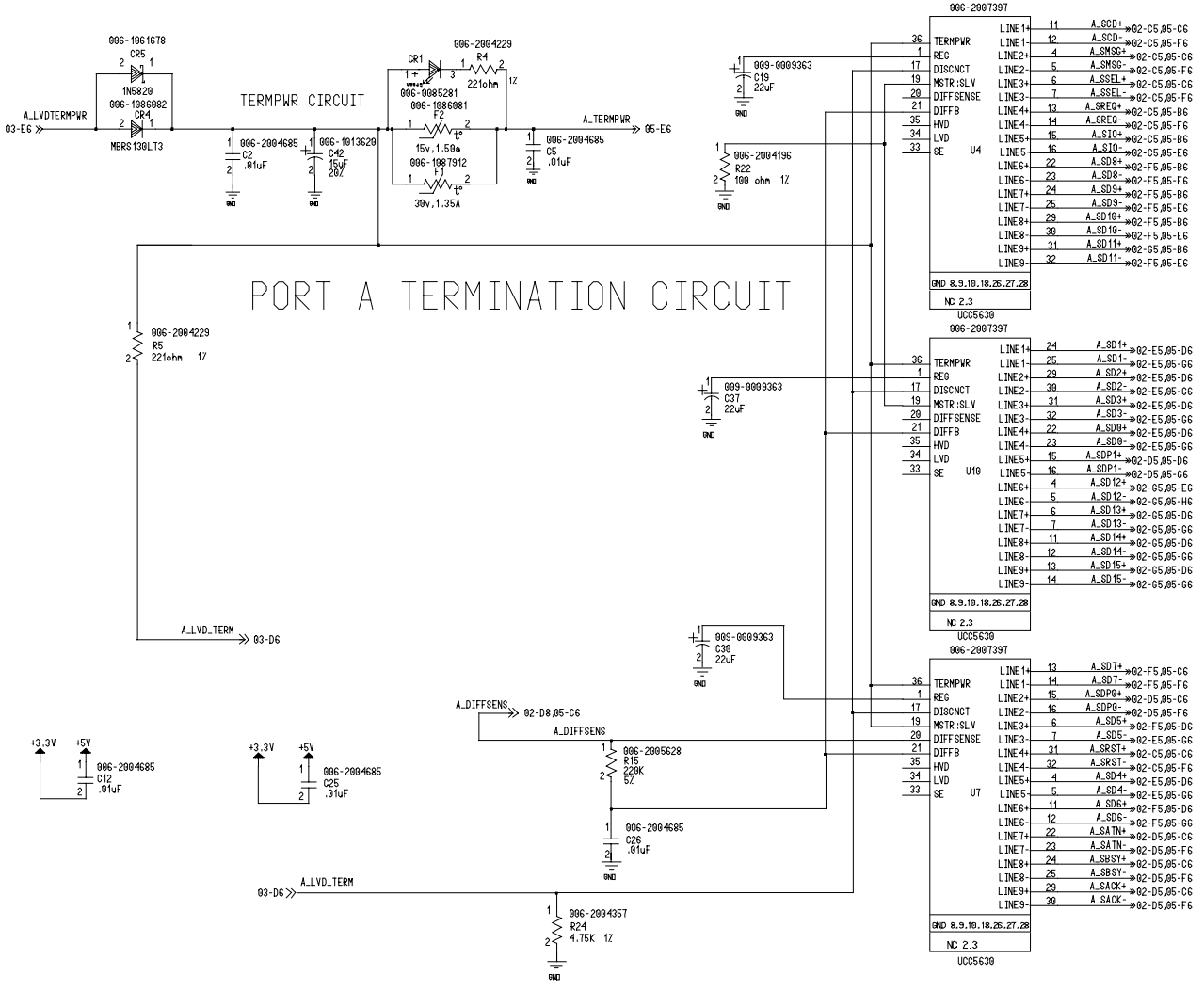
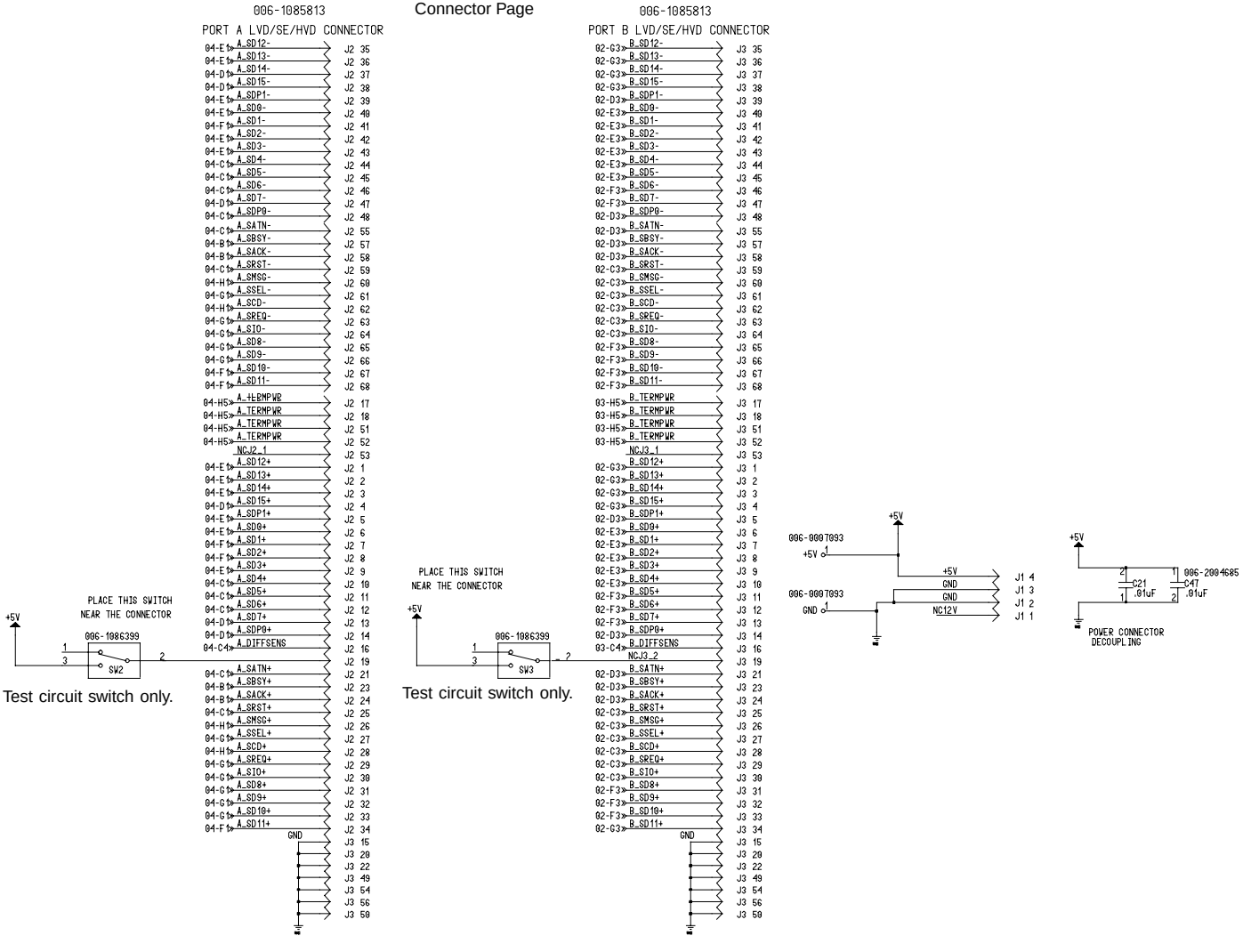


Figure A.1 SYM53C140 Wiring Diagram 4 of 4



Appendix B
Glossary

ACK/	Acknowledge – Driven by an initiator, ACK/ indicates an acknowledgment or a SCSI data transfer. In the target mode, ACK/ is received as a response to the REQ/ Signal.
ANSI	American National Standards Institute.
Arbitration	The process of selecting one respondent from a collection of several candidates that request service concurrently.
Asserted	A signal is asserted when it is in the state that is indicated by the name of the signal. Opposite of negated or deasserted.
Assertion	The act of driving a signal to the true state.
Asynchronous Transmission	Transmission in which each byte of the information is synchronized individually through the use of Request (REQ/) and Acknowledge (ACK/) signals.
ATN/	Attention – Driven by an initiator, indicates an attention condition. In the target role, ATN/ is received and is responded to by entering the Message Out Phase.
Block	A block is the basic 512 byte size of storage that the storage media is divided into. The Logical Block Address protocol uses sequential block addresses to access the media.
BSY/	Busy – Indicates that the SCSI Bus is being used. BSY/ can be driven by the initiator or the target device.
Bus	A collection of unbroken signal lines that interconnect computer modules. The connections are made by taps on the lines.
Bus Expander	Bus expander technology permits the extension of a bus by providing some signal filtering and retiming to maintain signal skew budgets.

Cable Skew Delay	Cable skew delay is the minimum difference in propagation time allowed between any two SCSI bus signals measured between any two SCSI devices.
C_D/	Control/Data – Driven by a target. When asserted, indicates Control or Data Information is on the SCSI Bus. This signal is received by the initiator.
Connect	The function that occurs when an initiator selects a target to start an operation, or a target reselects an initiator to continue an operation.
Control Signals	The set of nine lines used to put the SCSI bus into its different phases. The combinations of asserted and negated control signals define the phases.
Controller	A computer module that interprets signals between a host and a peripheral device. Often, the controller is a part of the peripheral device, such as circuitry on a disk drive.
DB[7:0]/	SCSI Data Bits – These eight Data Bits (DB[7:0]/), plus a Parity Bit (DBP/), form the SCSI Bus. DB7/ is the most significant bit and has the highest priority ID during the Arbitration Phase. Data parity is odd. Parity is always generated and optionally checked. Parity is not valid during arbitration.
Deasserted	The act of driving a signal to the false state or allowing the cable terminators to bias the signal to the false state (by placing the driver in the high impedance condition). A signal is deasserted or negated when it is in the state opposite to that which is indicated by the name of the signal. Opposite of asserted.
Device	A single unit on the SCSI bus, identifiable by a SCSI address. It can be a processor unit, a storage unit (such as a disk or tape controller or drive), an output unit (such as a controller or printer), or a communications unit.
Differential	A signaling alternative that employs differential drivers and receivers to improve signal-to-noise ratios and increase maximum cable lengths.
Disconnect	The function that occurs when a target releases control of the SCSI bus, allowing the bus to go to the Bus Free phase.
Driver	When used in the context of electrical configuration, “driver” is the circuitry that creates a signal on a line.

External Configuration	All SCSI peripheral devices are external to the host enclosure.
External Terminator	The terminator that exists on the last peripheral device that terminates the end of the external SCSI bus.
Free	In the context of Bus Free phase, “free” means that no SCSI device is actively using the SCSI bus and, therefore, the bus is available for use.
Host	A processor, usually consisting of the central processing unit and main memory. Typically, a host communicates with other devices, such as peripherals and other hosts. On the SCSI bus, a host has a SCSI address.
Host Adapter	Circuitry that translates between a processor's internal bus and a different bus, such as SCSI. On the SCSI bus, a host adapter usually acts as an initiator.
Initiator	A SCSI device that requests another SCSI device (a target) to perform an operation. Usually, a host acts as an initiator and a peripheral device acts as a target.
Internal Configuration	All SCSI peripheral devices are internal to the host enclosure.
Internal Terminator	The terminator that exists within the host that terminates the internal end of the SCSI bus.
I/O/	Input/Output – Driven by a target. I/O controls the direction of data transfer on the SCSI Bus. When active, this signal indicates input to the initiator. When inactive, this signal indicates output from the initiator. This signal is also used to distinguish between the Selection and Reselection Phases.
I/O Cycle	An I/O cycle is an Input (I/O Read) operation or Output (I/O Write) operation that accesses the PC Card’s I/O address space.
Logical Unit	The logical representation of a physical or virtual device, addressable through a target. A physical device can have more than one logical unit.
Low (logical level)	A signal is at the low logic level when it is below approximately 0.5 volts.

LSB	Abbreviation for Least Significant Bit or Least Significant Byte. That portion of a number, address or field that occurs right-most when its value is written as a single number in conventional hexadecimal or binary notation. The portion of the number having the least weight in a mathematical calculation using the value.
LUN	Logical Unit Number. Used to identify a logical unit.
Mandatory	A characteristic or feature that must be present in every implementation of the standard.
MHz	MegaHertz – Measurement in millions of Hertz per second. Used as a measurement of data transfer rate.
microsecond (μs)	One millionth of a second.
MSB	Abbreviation for Most Significant Bit or Most Significant Byte. That portion of a number, address or field that occurs left-most when its value is written as a single number in conventional hexadecimal or binary notation. The portion of the number having the most weight in a mathematical calculation using the value.
MSG/	Message – Driven active by a target during the Message Phase. This signal is received by the initiator.
nanosecond (ns)	One billionth of a second.
Negated	A signal is negated or deasserted when it is in the state opposite to that which is indicated by the name of the signal. Opposite of asserted.
Negation	The act of driving a signal to the false state or allowing the cable terminators to bias the signal to the false state.
Parity	A method of checking the accuracy of binary numbers. An extra bit, called a parity bit, is added to a number. If even parity is used, the sum of all 1s in the number and its corresponding parity is always even. If odd parity is used, the sum of the 1s and the parity bit is always odd.
Peripheral device	A device that can be attached to the SCSI bus. Typical peripheral devices are disk drives, tape drives, printers, CD ROMs, or communications units.
Phase	One of the eight states to which the SCSI bus can be set. During each phase, different communication tasks can be performed.
Port	A connection into a bus.

Priority	The ranking of the devices on the bus during arbitration.
Protocol	A convention for data transmission that encompasses timing control, formatting, and data representation.
Receiver	The circuitry that receives electrical signals on a line.
Reconnect	The function that occurs when a target reselects an initiator to continue an operation after a disconnect.
Release	The act of allowing the cable terminators to bias the signal to the false state (by placing the driver in the high impedance condition).
REQ/	Request – Driven by a target, indicates a request for a SCSI data-transfer handshake. This signal is received by the initiator.
Reselect	A target can disconnect from an initiator in order to perform a time-consuming function, such as a disk seek. After performing the operation, the target can “reselect” the initiator.
RESET	Reset – Clears all internal registers when active. It does not assert the SCSI RST/ signal and therefore does not reset the SCSI bus.
RST	Reset – Indicates a SCSI Bus reset condition.
SCSI Address	The octal representation of the unique address ([7:0]) assigned to an SCSI device. This address is normally assigned and set in the SCSI device during system installation.
SCSI ID (Identification) or SCSI Device ID	The bit-significant representation of the SCSI address referring to one of the signal lines DB7/ through DB0/.
SCSI	Small Computer System Interface.
SCAM	An acronym for SCSI Configured AutoMatically. SCAM is the new SCSI automatic ID assignment protocol. SCAM frees SCSI users from locating and setting SCSI ID switches and jumpers. SCAM is the key part of Plug and Play SCSI.
SEL/	Select – Used by an initiator to select a target, or by a target to reselect an initiator.
Single-ended configuration	An electrical signal configuration that uses a single line for each signal, referenced to a ground path common to the other signal lines. The advantage of a single-ended configuration is that it uses half the pins, chips, and board area that differential/low-voltage differential

	configurations require. The main disadvantage of single-ended configurations is that they are vulnerable to common mode noise. Also, cable lengths are limited.
Synchronous transmission	Transmission in which the sending and receiving devices operate continuously at the same frequency and are held in a desired phase relationship by correction devices. For buses, synchronous transmission is a timing protocol that uses a master clock and has a clock period.
Target	A SCSI device that performs an operation requested by an initiator.
Termination	The electrical connection at each end of the SCSI bus, composed of a set of resistors.
µs	Microsecond. One millionth of a second.

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