Chapter 6

Electrical Specifications

DC Electrical Characteristics

Table 6-1: Absolute Maximum Stress Ratings

Parameter	Symbol	Pins	Test Conditions	Min	Max	Unit
Storage temperature	T_{STG}	-	-	-55	150	°C
Supply voltage	V_{DD}	-	-	-0.5	7.0	V
Input voltage	V_{IN}	-	-	V_{SS}- 0.5	V_{DD}+ 0.5	V
Latch-up current	I_{LU}	-	$-2V < V_{PIN} < +8V$	± 100	-	mA

Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the Operating Conditions section of this specification is not implied.

Table 6-2: Recommended Operating Conditions

Parameter	Symbol	Pins	Test Conditions	Min	Max	Unit
Supply voltage	V_{DD}	-	-	4.75	5.25	V
Supply current	I_{DD}	-	Static*	-	1	mA
Supply current	I_{DD}	-	Dynamic	-	50	mA
Ambient temperature	T_A	-	-	0	70	°C
Thermal resistance, junction/ambient	Θ_{JA}			-	32	°C/W
Rise Time	t_r	**	-	1	-	V/ns
Fall Time	t_f	**	-	1	-	V/ns

* *Static means: all inputs are deasserted, all outputs floating, and all bidirectional pins configured as inputs.*

** *These timings apply to all pins without Schmitt triggers.*

Table 6-3: Inputs

Parameter	Symbol	Pins	Test Conditions	Min	Max	Unit
Input high voltage	V_{IH}	-	-	2.0	V_{DD} + 0.5	V
Input low voltage	V_{IL}	-	-	V_{SS} –0.5	0.8	V
Input leakage current	I_{IN}	Non-SCSI	$0 < V_{IN} < V_{DD}$	–10	10	µA
Hysteresis	V_H	SCSI	-	300	400	mV
Input leakage current	I_{IL}	SCSI	$0 < V_{IN} < V_{DD}$	–10	10	µA
Capacitance	C_{IN}		-	-	10	pF

Table 6-4: Outputs

Parameter	Symbol	Pins	Test Conditions	Min	Max	Unit
Output high voltage	V_{OH}	DREQ	I_{OH}= –2 mA	2.4	V_{DD}	V
Output low voltage	V_{OL}	DREQ, INT/	I_{OL}= 4 mA	V_{SS}	0.4	V
Output low voltage*	V_{OL}	RST/, SEL/, ACK/, REQ/, BSY/, SDP, SD7-0	I_{OL}= 48 mA	V_{SS}	0.5	V
Hi Z state leakage	I_{OZ}	-	$0 < V_{OUT} < V_{DD}$	–10	10	µA
Fall Time	T_F	SCSI pins	SCSI termination	5.2	14.7	ns
Capacitance	C_{OUT}	-	-	-	10	pF

* TolerANT Active Negation not enabled.

Table 6-5: Bidirectional Pins

Parameter	Symbol	Pins	Test Conditions	Min	Max	Unit
Input high voltage	V_{IH}	-	-	2.0	V_{DD}+ 0.5	V
Input low voltage	V_{IL}	-	-	V_{SS}–0.5	0.8	V
Output high voltage*	V_{OH}	SCSI inputs	I_{OH}= –2 mA	2.4	V_{DD}	V
Output low voltage	V_{OL}	SCSI inputs	I_{OL}= 4 mA	V_{SS}	0.4	V
Output low voltage*	V_{OL}	SD7-0, SDP, REQ/ , ACK/	I_{OL}= 48 mA	V_{SS}	0.5	V
Hysteresis	V_H	SCSI	-	300	400	mV
Input leakage	I_I	SCSI	$0 < V_{IN} < V_{DD}$	–10	10	µA
Input current, low	I_{IL}	DB7-0, DBP, PAD7-0	V_{IN}= 0	–200	-50	µA
Input current, high	I_{IH}	DB7-0, DBP, PAD7-0	V_{IN}= V_{DD}	0	10	µA
Hi-Z pull-up current	I_{PU}	DB7-0, DBP, PAD7-0	V_{IN}= 0	-200	-50	µA
Capacitance	C_{IO}		-	-	10	pF

* TolerANT Active Negation not enabled.

Symbios Logic Tolerant® Specifications

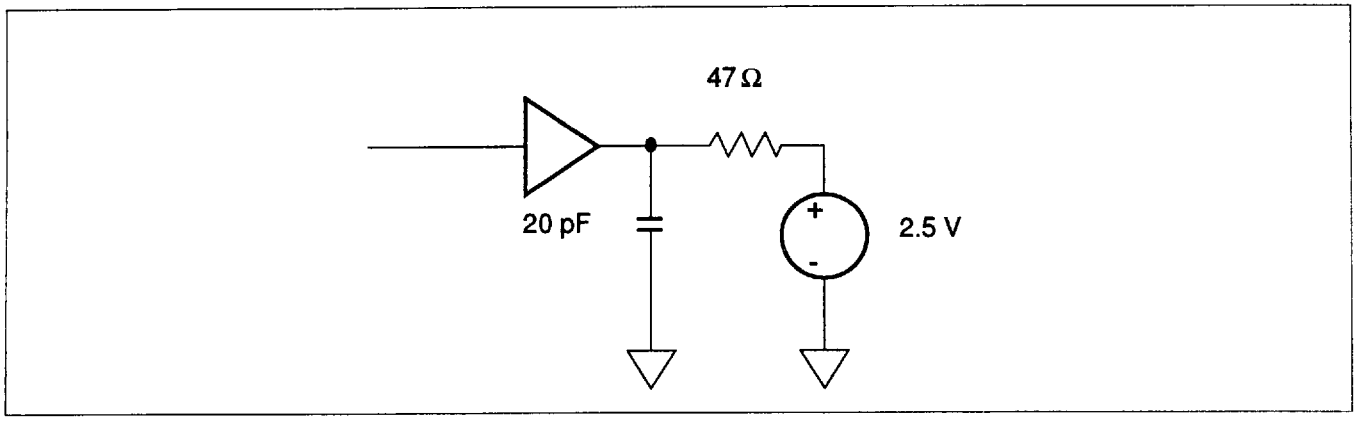


Figure 6-1: Rise and Fall Time Test Conditions

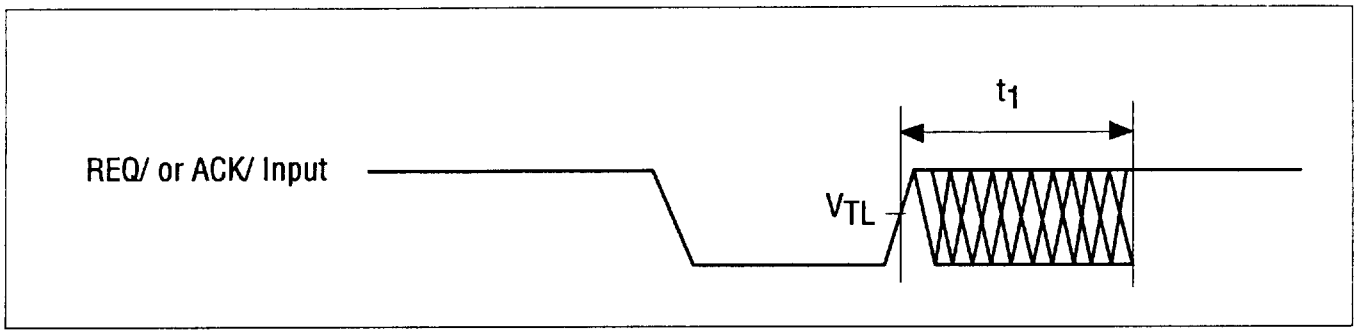


Figure 6-2: SCSI Input Filtering

t_1 = input filtering period, register-programmable (bit 4 of the Config-3 Register, Register 0C) to either 30 or 60 ns.

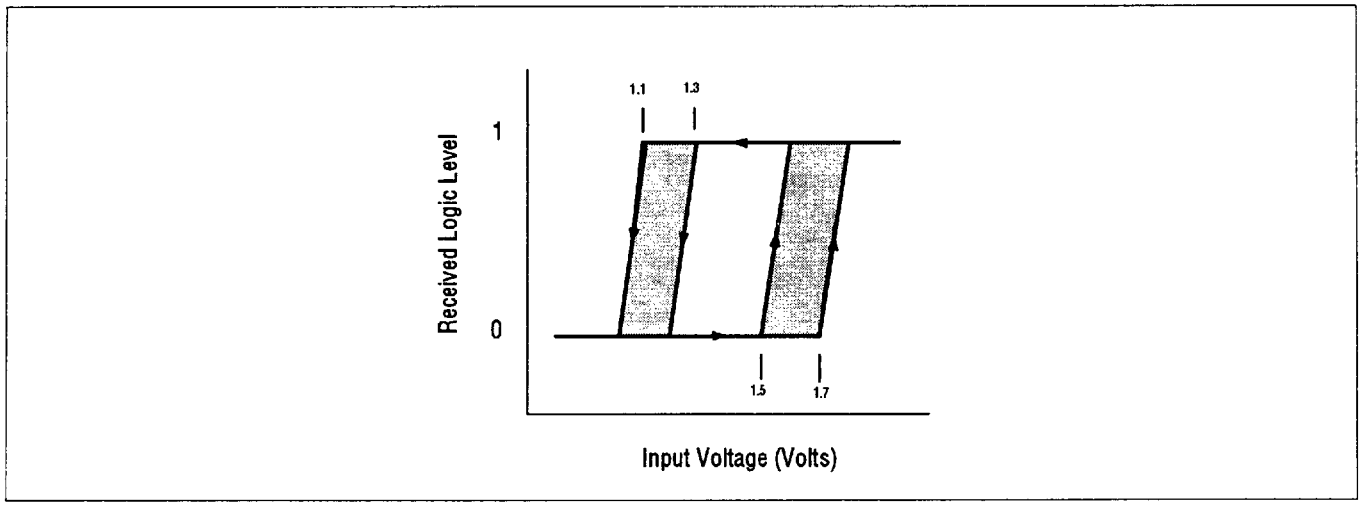


Figure 6-3: Hysteresis of SCSI Receiver

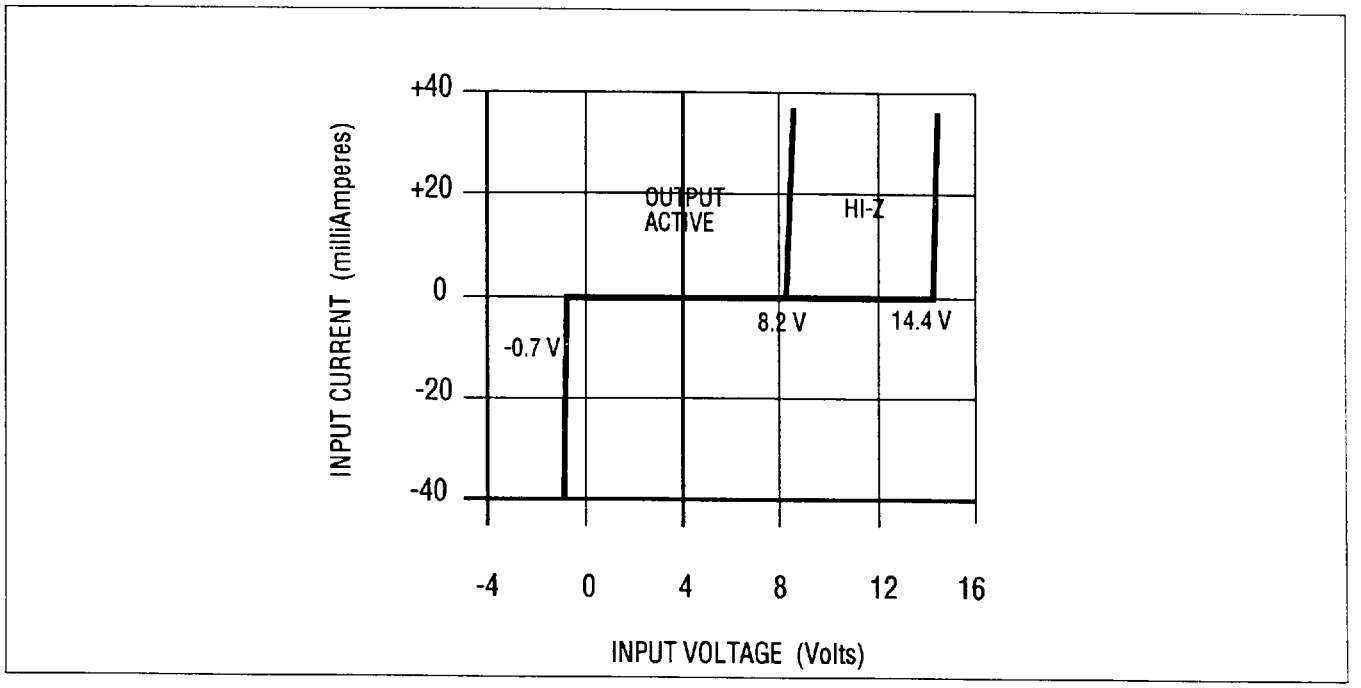


Figure 6-4: Input Current as a Function of Input Voltage

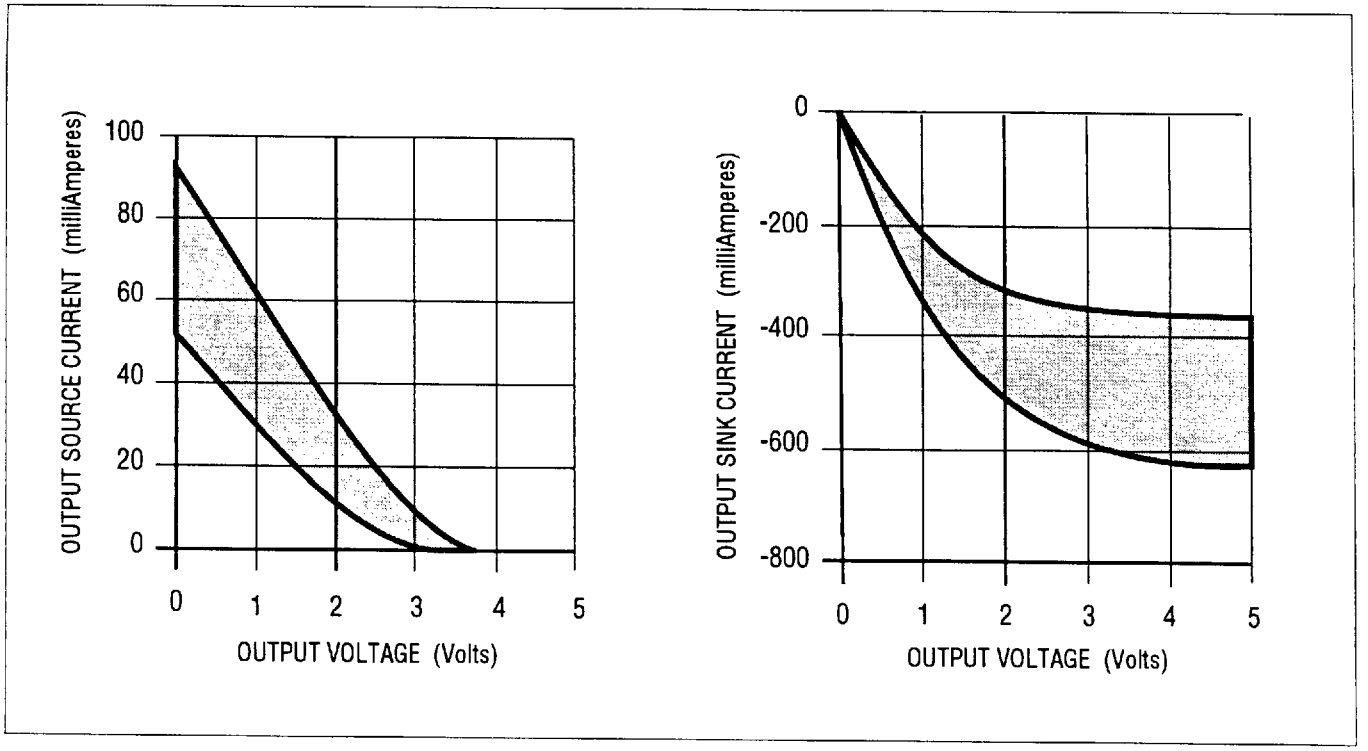


Figure 6-5: Output Current as a Function of Output Voltage

Table 6-6: Symbios Logic TolerANT® Active Negation Technology Electrical Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{OH}[1]	Output high voltage	I_{OH} = 2.5 mA	2.5	3.1	3.5	V
V_{OL}	Output low voltage	I_{OL} = 48 mA	0.1	0.2	0.5	V
V_{IH}	Input high voltage		2.0		7.0	V
V_{IL}	Input low voltage	Referenced to V_{SS}	-0.5		0.8	V
V_{IK}	Input clamp voltage	V_{DD} = min; I_I = -20 mA	-0.66	-0.74	-0.77	V
V_{TH}	Threshold, high to low		1.1	1.2	1.3	V
V_{TL}	Threshold, low to high		1.5	1.6	1.7	V
V_{TH} - V_{TL}	Hysteresis		300	350	400	mV
I_{OH}[1]	Output high current	V_{OH} = 2.5 Volts	2.5	15	24	mA
I_{OL}	Output low current	V_{OL} = 0.5 Volts	100	150	200	mA
I_{OSH}[1]	Short-circuit output high current	Output driving low, pin shorted to V_{DD} supply[2]			625	mA
I_{OSL}	Short-circuit output low current	Output driving high, pin shorted to V_{SS} supply			95	mA
I_{LH}	Input high leakage	-0.5 < V_{DD} < 5.25 V_{PIN} = 2.7 V		0.05	10	µA
I_{LL}	Input low leakage	-0.5 < V_{DD} < 5.25 V_{PIN} = 0.5V		-0.05	-10	µA
R_I	Input resistance	SCSI pins [3]		20		MΩ
C_P	Capacitance per pin	Quad Flat Pack Package	6	8	10	pF
t_R[1]	Rise time, 10% to 90%	Figure 6-1	9.7	15.0	18.5	ns
t_F	Fall time, 90% to 10%	Figure 6-1	5.2	8.1	14.7	ns
dV_H/dt	Slew rate, low to high	Figure 6-1	0.15	0.23	0.49	V/ns
dV_L/dt	Slew rate, high to low	Figure 6-1	0.19	0.37	0.67	V/ns
I_{LU}	Latch-up		100			mA
t_1	Filter Delay	Figure 6-2	20	25	30	ns
t_1	Extended Filter Delay	Figure 6-2	40	50	60	ns

Note: These values are guaranteed by periodic characterization.

Legend:

1 Active Negation outputs only: Data, Parity, REQ/, ACK/

2 Single pin only; irreversible damage may occur if sustained for 1 second

3 SCSI RESET pin has 10KΩ pull-up resistor

AC Electrical Characteristics

The AC characteristics described in this section apply over the operating voltage and temperature range, $4.75\,V \geq V_{DD} \geq 5.25\,V$ and $0°C \geq T_A \geq 70°C$. Output timing is based on simulation under worst case conditions (4.75 V, 70°C) and worst case processing using the following termination. All timings in this specification are taken from the 10% and 90% points with respect to the specified V_{OL} and V_{OH} of the waveforms.

Note: Performance numbers are based upon the FSC operating with a 40MHz clock. Other clock inputs will also allow for increased transfer rates in proportion to their frequencies.

Table 6-7: Pin Terminations

Pin	Termination
DREQ, PAD7-0	50 pF
INT/	50 pF, 2.2K pull-up
DB7-0, DBP	80 pF
SDP, SD7-0, RST/, SEL/, BSY/, ATN/, MSG/, CD/, IO/, REQ/, ACK/	200 pF, 110Ω pullup, 165Ω pulldown

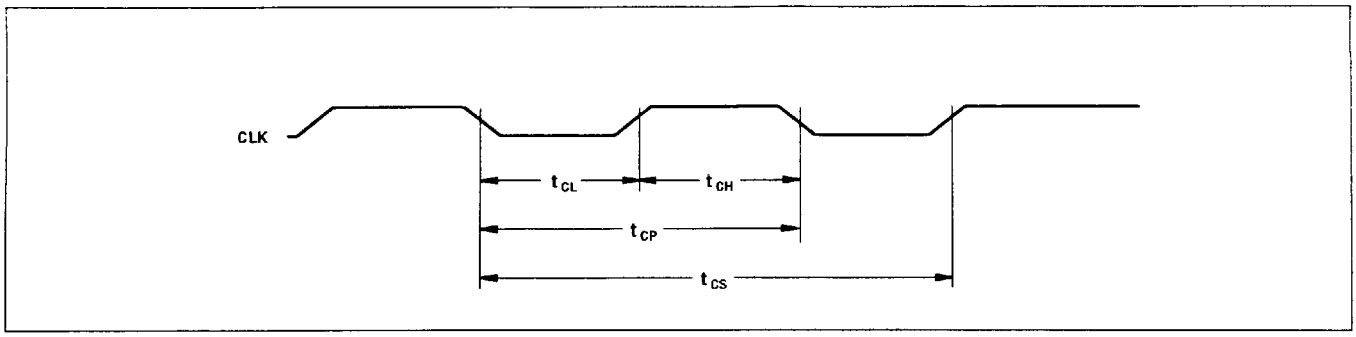


Figure 6-6: Clock Input

Table 6-8: Clock Timings (FASTCLK bit cleared)

Parameter	Symbol	Min	Max	Units	Notes
Clock frequency, asynchronous SCSI	t_{CPA}	10	25	MHz	1
Clock frequency, synchronous SCSI	t_{CPS}	12	25	MHz	1
Clock high time	t_{CH}	$0.4t_{CP}$	$0.6t_{CP}$	ns	
Clock low time	t_{CL}	$0.4t_{CP}$	$0.6t_{CP}$	ns	
Clock period	t_{CP}	40	100	ns	-
Synchronization latency = t_{CP} + t_{CL}	t_{CS}	t_{CP}	t_{CL} + t_{CP}	-	-

Table 6-9: Clock Timings (FASTCLK bit set)

Parameter	Symbol	Min	Max	Units	Notes
Clock frequency, asynchronous SCSI	t_{CPA}	25	40	MHz	1
Clock frequency, synchronous SCSI	t_{CPS}	25	40	MHz	1
Clock high time	t_{CH}	0.4 * t_{CP}	0.6 * t_{CP}	ns	-
Clock low time	t_{CL}	0.4 * t_{CP}	0.6 * t_{CP}	ns	-
Clock period	t_{CP}	25	40	ns	-
Synchronization latency = t_{CP} + t_{CL}	t_{CS}	t_{CP}	t_{CL} + t_{CP}	-	-

1. Minimum frequencies to meet ANSI timing specifications.

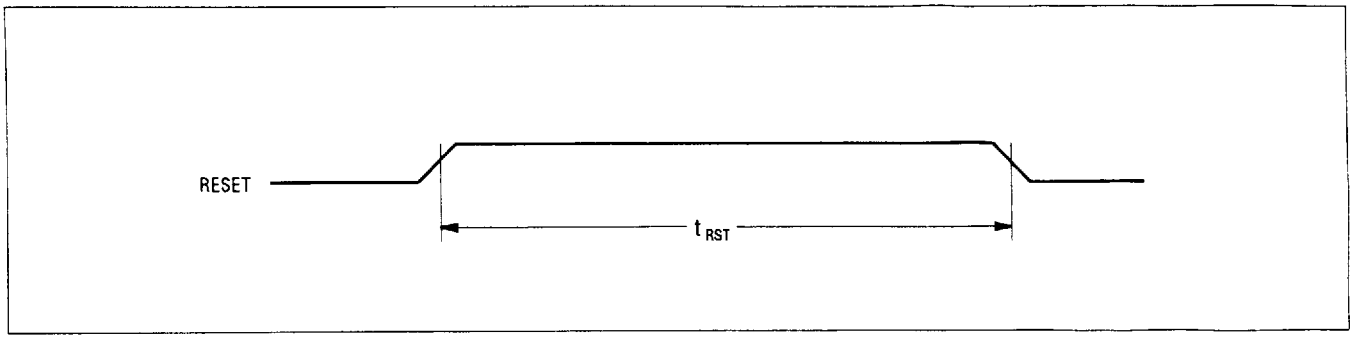


Figure 6-7: Reset Input

Table 6-10: Reset Timing

Parameter	Symbol	Min	Max	Units	Notes
RESET pulse width	t_{RST}	$3t_{CP}$	-	ns	1

1. *At power up, the RESET pin must be asserted as V_{DD} first becomes stable.*

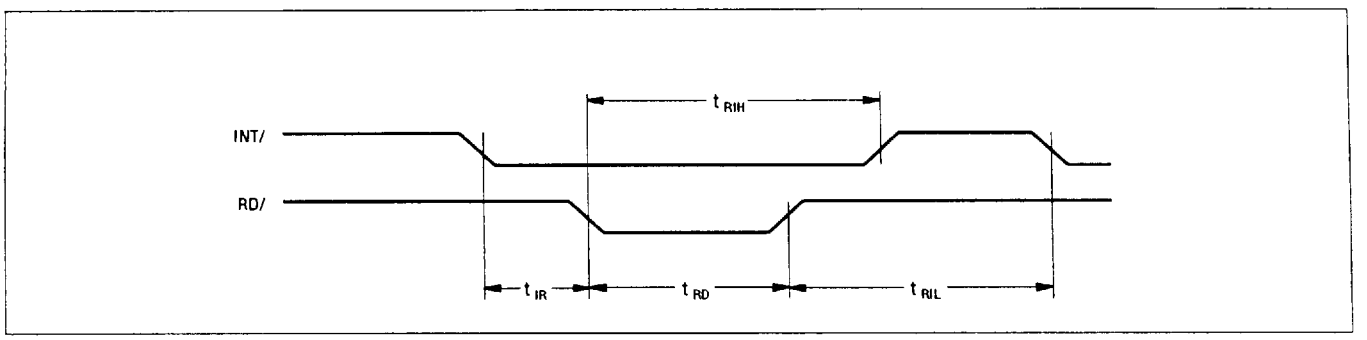


Figure 6-8: Interrupt Output

Table 6-11: Interrupt Timings

Parameter	Symbol	Min	Max	Units	Notes
INT/ low to Interrupt Register read	t_{IR}	0	-	ns	2
RD/ pulse width	t_{RD}	30	-	ns	1
RD/ low to INT/ high	t_{RIH}	0	$3t_{CP}$ + 30	ns	-
RD/ high to INT/ low	t_{RIL}	t_{CS}	-	ns	-

1. *Refer to the register read specifications for the timing requirements of CS/, RD/, and address for reading the Interrupt register.*
2. *The Interrupt register should not be read when INT/ is false.*

Register Interface, Non-Multiplexed PAD Bus

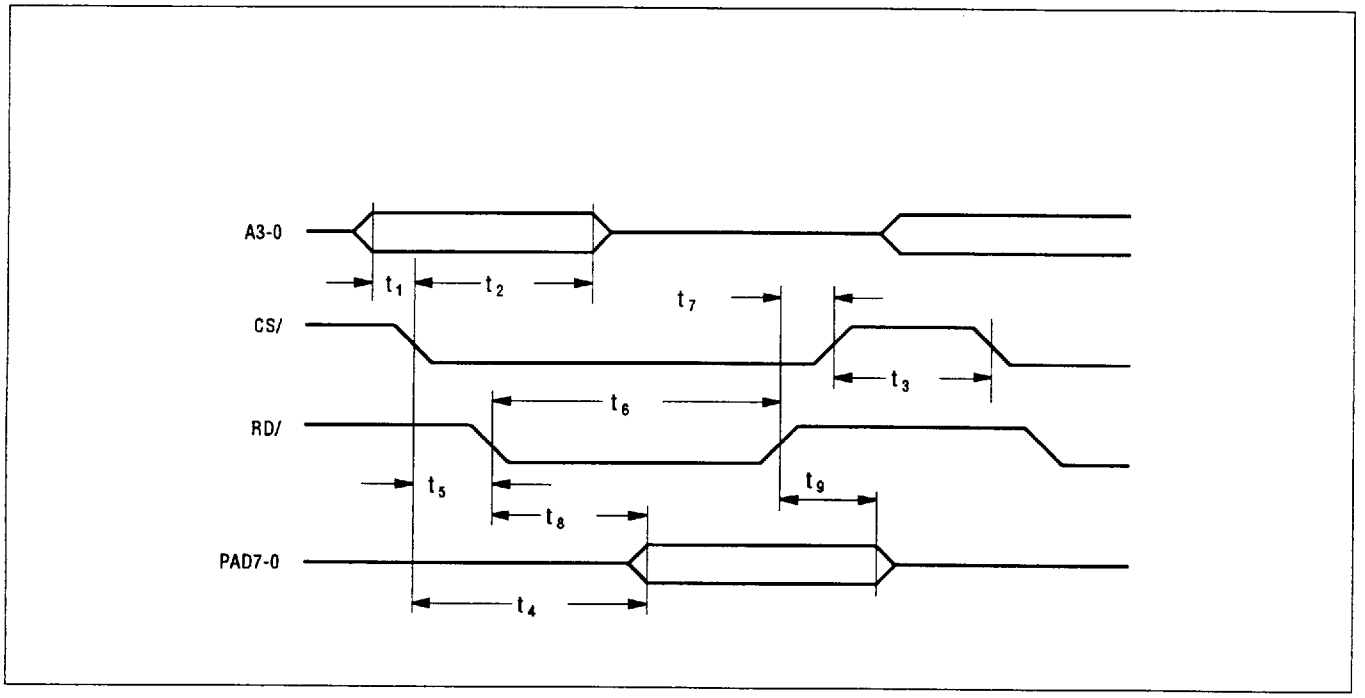


Figure 6-9: Register Read, Nonmultiplexed PAD Bus

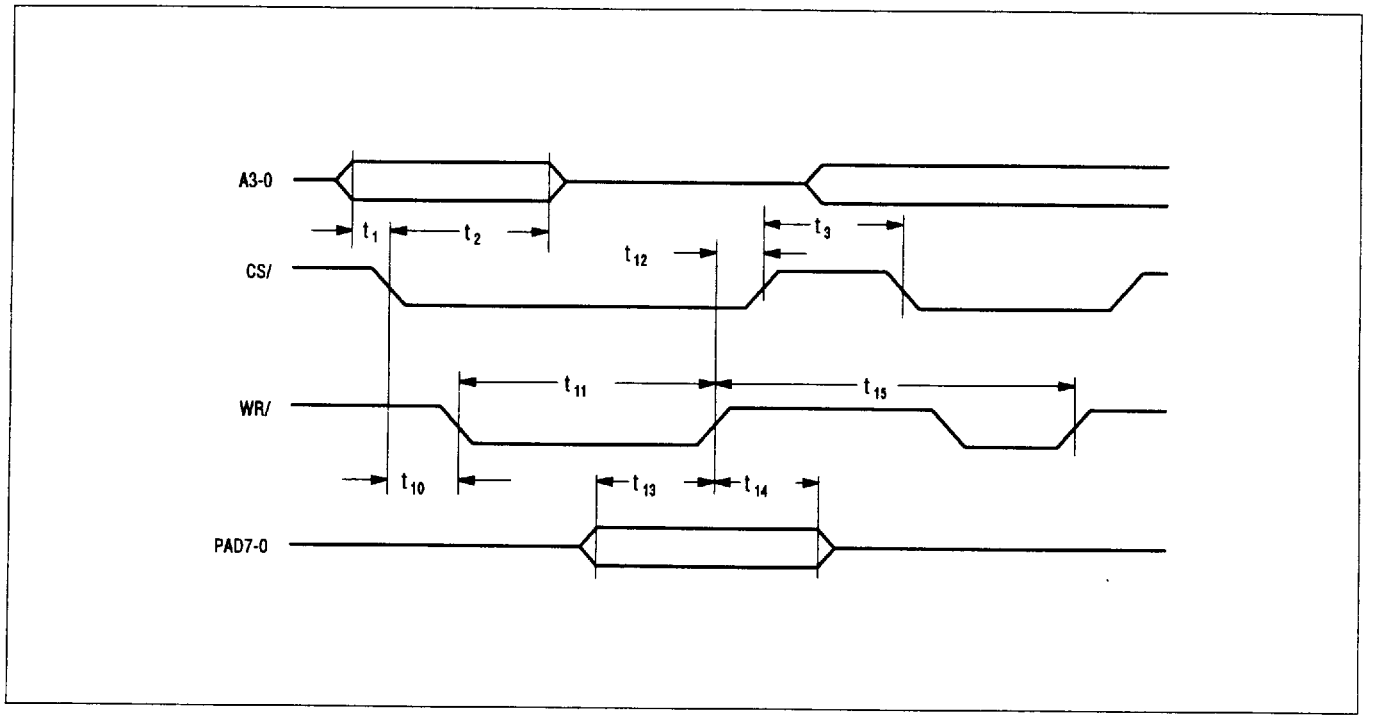


Figure 6-10: Register Write, Nonmultiplexed PAD Bus

Table 6-12: Register Interface, Non-Multiplexed PAD Bus

Parameter	Symbol	Min	Max	Units	Notes
Address setup to CS/ low	t_1	3	-	ns	1
Address hold from CS/ low	t_2	20	-	ns	-
CS/ high to CS/ low	t_3	t_{CP} + 5	-	ns	7
CS/ low to read data valid	t_4	-	t_{CP} + 30	ns	2
CS/ setup to RD/ low	t_5	0	-	ns	3, 6
RD/ pulse width	t_6	30	-	ns	-
RD/ high to CS/ high	t_7	0	-	ns	3
RD/ low to data valid	t_8	-	30	ns	4
RD/high to data bus disable	t_9	2	30	ns	-
CS/ setup to WR/ low	t_{10}	0	-	ns	5, 6
WR/ pulse width	t_{11}	30	-	ns	-
WR/ high to CS/ high	t_{12}	0	-	ns	5
Data setup to WR/ high	t_{13}	15	-	ns	-
Data hold after WR/ high	t_{14}	4	-	ns	-
CS/ or WR/ high to CS/ or WR/ high	t_{15}	$3t_{CP}$	-	ns	-

1. *CS/ must make a high to low transition to latch a new register address.*
2. *t_8 must also be satisfied.*
3. *If RD/ is held low, the time from CS/ low to stable data is t_4 and the output disable time from CS/ high is t_9.*
4. *t_4 must also be satisfied.*
5. *If WR/ is held low, the data setup to CS/ high is t_{13} minimum; data hold from CS/ high is t_{13} minimum.*
6. *If DMA is active, the FIFO must not be accessed.*
7. *t_3 min is (2 * $3t_{CP}$ + 5) for successive FIFO reads or a FIFO write/read followed by a read of the FIFO flags register.*

Register Interface, Multiplexed PAD Bus

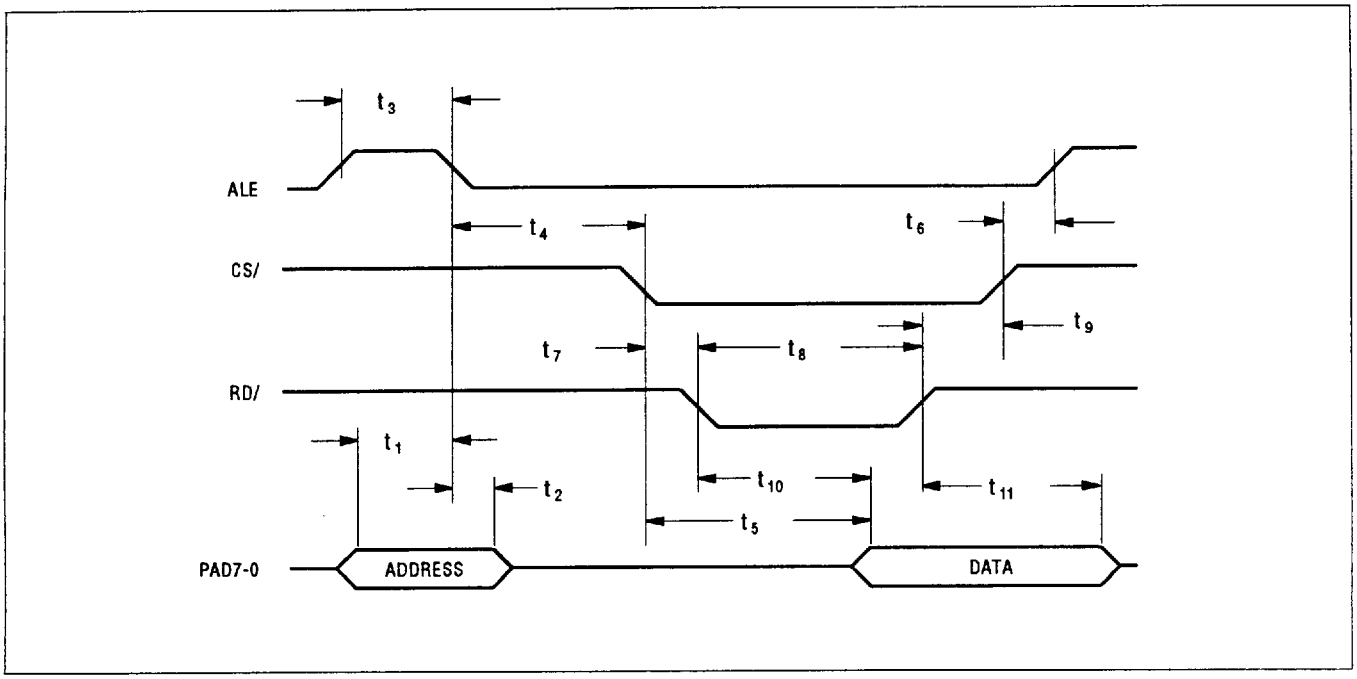


Figure 6-11: Register Read, Multiplexed PAD Bus

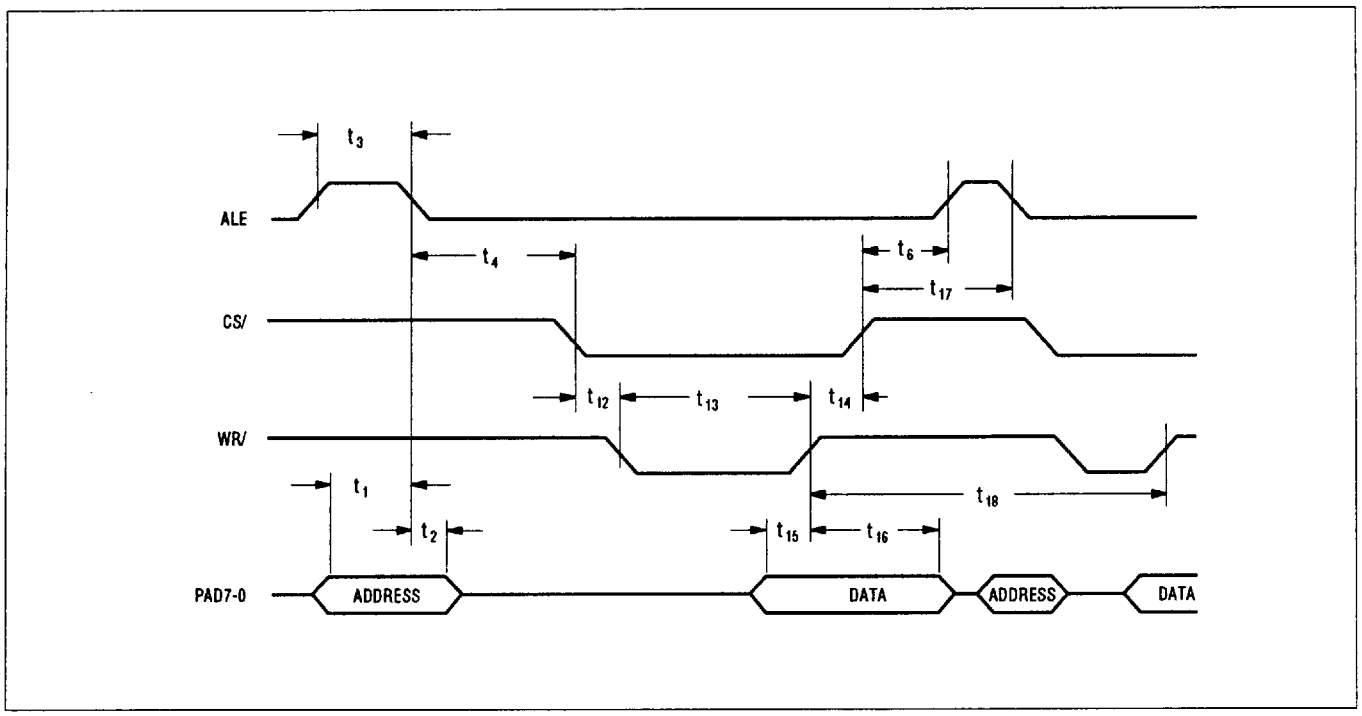


Figure 6-12: Register Write, Multiplexed PAD Bus

Table 6-13: Register Interface, Multiplexed PAD Bus

Parameter	Symbol	Min	Max	Units	Notes
Address setup to ALE low	t_1	10	-	ns	-
Address hold from ALE low	t_2	10	-	ns	-
ALE pulse width	t_3	20	-	ns	-
ALE low to CS/ low	t_4	10	-	ns	-
CS/ low to data valid	t_5	-	t_{CP} + 30	ns	3
CS/ high to ALE high	t_6	0	-	ns	-
CS/ setup to RD/ low	t_7	0	-	ns	1, 4
RD/ pulse width	t_8	30	-	ns	-
RD/ high to CS/ high	t_9	0	-	ns	4
RD/ low to data valid	t_{10}	-	30	ns	5
RD/high to data bus disable	t_{11}	2	30	ns	-
CS/ setup to WR/ low	t_{12}	0	-	ns	1, 6
WR/ pulse width	t_{13}	30	-	ns	-
WR/ high to CS/ high	t_{14}	0	-	ns	6
Data setup to WR/ high	t_{15}	15	-	ns	-
Data hold from WR/ high	t_{16}	4	-	ns	-
WR/ high to ALE high	t_{17}	t_{CP} + 5	-	ns	7
CS/ or WR/ high to CS/ or WR/ high	t_{18}	$3t_{CP}$	-	ns	

1. *If DMA is active, the FIFO register must not be accessed.*
2. *ALE must pulse to capture a new register address.*
3. *t_{10} must also be satisfied.*
4. *If RD/ is held low, the time from CS/ low to stable data is t_5 and the data release time from CS/ high is t_{11}.*
5. *t_5 must also be satisfied.*
6. *If WR/ is held low, data setup to CS/ high is t_{15} and data hold from CS/ high is t_{16} minimum.*
7. *t_3 min is (2 * $3t_{CP}$ + 5) for successive FIFO reads or a FIFO write/read followed by a read of the FIFO flags register.*

DMA Interface (Non-Multiplexed Mode only)

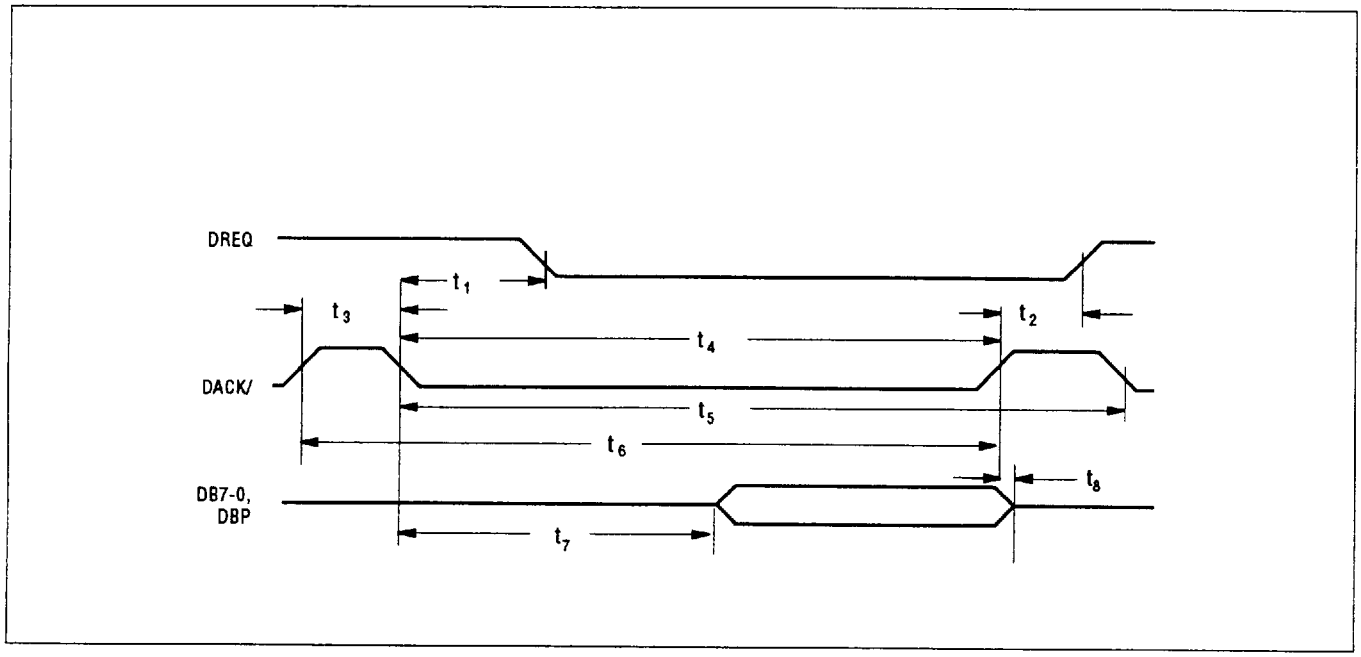


Figure 6-13: DMA Read (Non-Multiplexed Mode only)

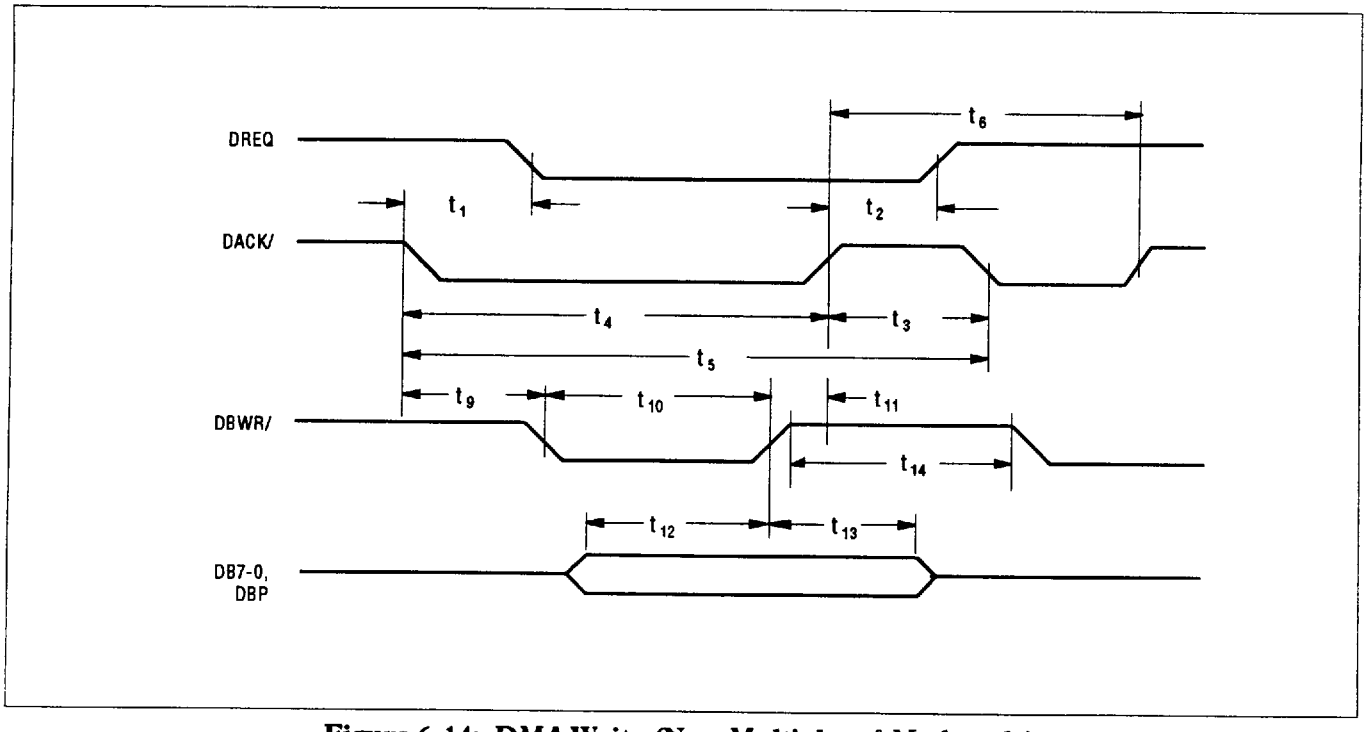


Figure 6-14: DMA Write (Non-Multiplexed Mode only)

Table 6-14: DMA Interface (Non-Multiplexed Mode only)

Parameter	Symbol	Min	Max	Units	Notes
DACK/ low to DREQ low	t_1	-	30	ns	4
DACK/ high to DREQ high	t_2	30	-	ns	-
DACK/ high to DACK/ low	t_3	$t_{CP} + 5$	-	ns	3
DACK/ pulse width	t_4	$t_{CP} + 5$	-	ns	-
DACK/ period (low to low)	t_5	$3t_{CP}$	-	ns	-
DACK/ period (high to high)	t_6	$3t_{CP}$	-	ns	
DACK/ low to data valid	t_7	-	30	ns	-
DACK/ high to data bus disable	t_8	2	30	ns	-
DACK/ low to DBWR/ low	t_9	0	-	ns	3
DBWR/ pulse width	t_{10}	30	-	ns	-
DBWR/ high to DACK/ high	t_{11}	0	-	ns	3
Data setup to DBWR/	t_{12}	15	-	ns	-
Data hold from DBWR/	t_{13}	4	-	ns	-
DBWR/ high to DBWR/ low	t_{14}	30	-	ns	-

1. *Alternate DMA is disabled.*
2. *DACK/ must toggle once for each access.*
3. *DBWR/ edges may precede or follow DACK/ edges. Recommended values are: $t_9 \geq 0$ and $t_{11} \geq 0$. If DBWR/ is held low, the data setup to DACK/ high 15 ns minimum; data hold from DACK/ high is 4 ns minimum.*
4. *DREQ may stay high if the FIFO has room to accept another byte during DMA write, or send another byte during DMA read. If the current DMA acknowledge cycle fills the FIFO (write) or empties the FIFO (read), then DREQ will go low.*

DMA Interface (Multiplexed Mode only)

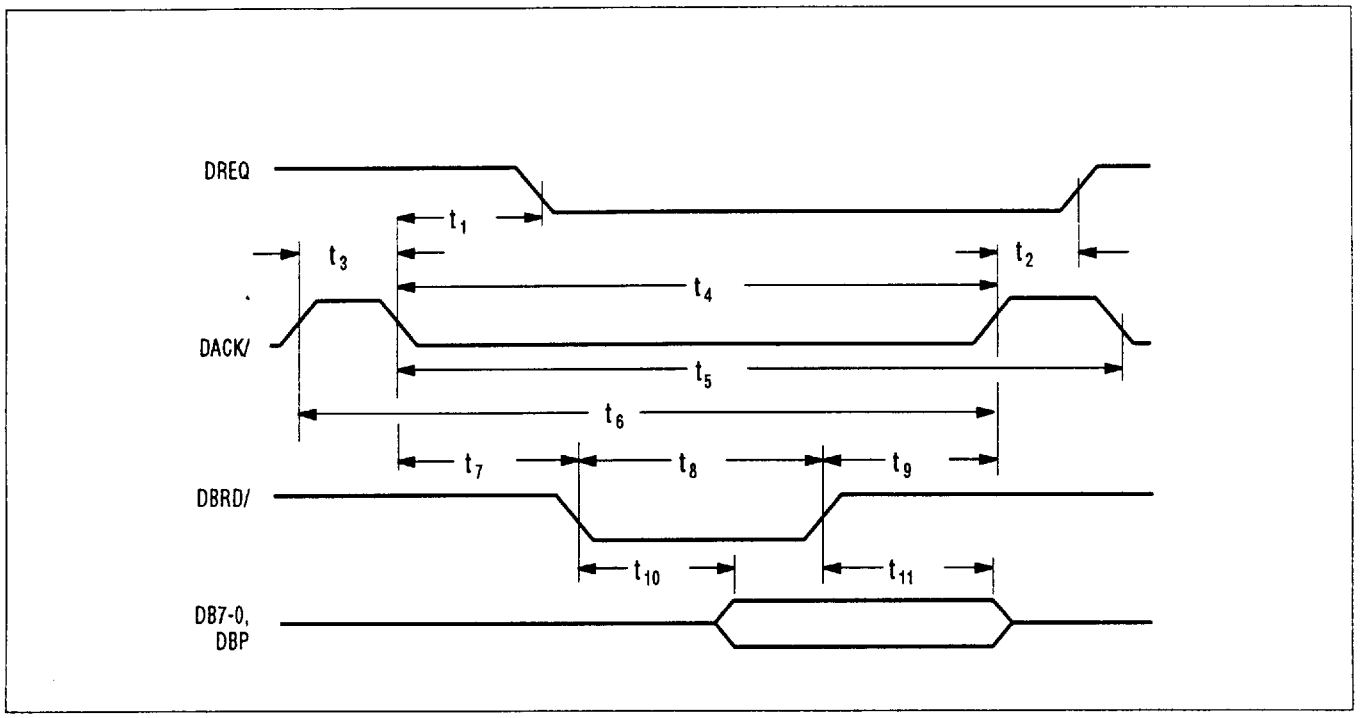


Figure 6-15: DMA Read (Multiplexed Mode only)

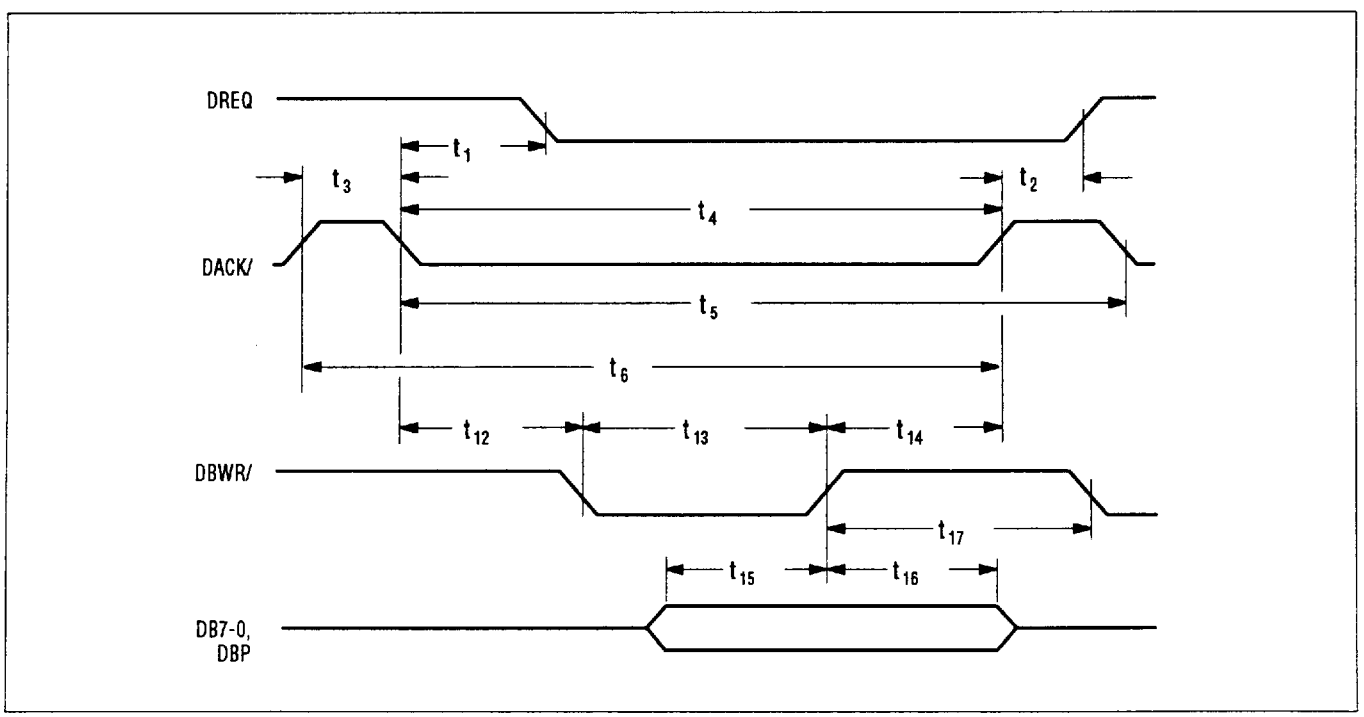


Figure 6-16: DMA Write (Multiplexed Mode only)

Table 6-15: DMA Interface (Multiplexed Mode only)

Parameter	Symbol	Min	Max	Units	Notes
DACK/ low to DREQ low	t_1	-	30	ns	5
DACK/ high to DREQ high	t_2	30	-	ns	5
DACK/ high to DACK/ low	t_3	$t_{CP} + 5$	-	ns	2
DACK/ pulse width	t_4	$t_{CP} + 5$	-	ns	-
DACK/ period (low to low)	t_5	$3t_{CP}$	-	ns	-
DACK/ period (high to high)	t_6	$3t_{CP}$	-	ns	-
DACK/ low to DBRD/ low	t_7	0	-	ns	3
DBRD/ pulse width	t_8	30	-	ns	-
DBRD/ high to DACK/ high	t_9	0	-	ns	3
DBRD/ to data valid	t_{10}	0	30	ns	-
DBRD/ high to data bus disable	t_{11}	2	30	ns	-
DACK/ low to DBWR/ low	t_{12}	0	-	ns	4
DBWR/ pulse width	t_{13}	30	-	ns	-
DBWR/ high to DACK/ high	t_{14}	0	-	ns	4
Data setup to DBWR/ high	t_{15}	15	-	ns	-
Data hold from DBWR/ high	t_{16}	4	-	ns	-
DBWR/ high to DBWR/ low	t_{17}	30	-	ns	-

1. *Alternate DMA is disabled.*
2. *DACK/ must toggle once for each access.*
3. *DBRD/ trailing edge may precede or follow DACK/ trailing edge. The recommended value is: $t_9 \geq 0$. If DBRD/ is held low past DACK/, the time from DACK/ low to stable data is 30 ns max, and the time from DACK/ high to data bus disable is 2 ns min and 25 ns max.*
4. *DBWR/ trailing edge may precede or follow DACK/ trailing edge. The recommended value is: $t_{14} \geq 0$. If DBWR/ is held past DACK/, the data setup to DACK/ high is 10 ns minimum, data hold from DACK/ high is 10 ns minimum.*
5. *DREQ may stay high if the FIFO has room to accept more data during DMA write, or send more data during DMA read. If the current DMA acknowledge cycle fills the FIFO (write) or empties the FIFO (read), then DREQ will go low.*

Burst Mode DMA Interface (Multiplexed Mode)

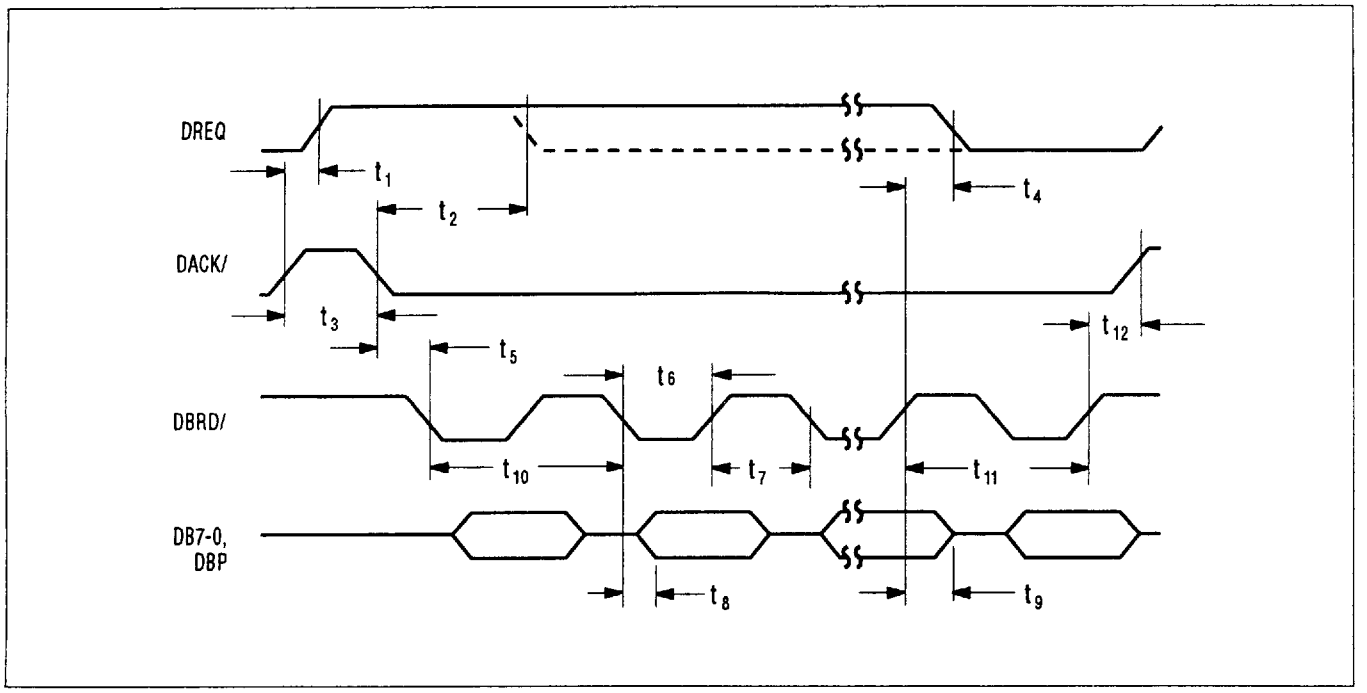


Figure 6-17: Burst Mode DMA Read (Multiplexed Mode)

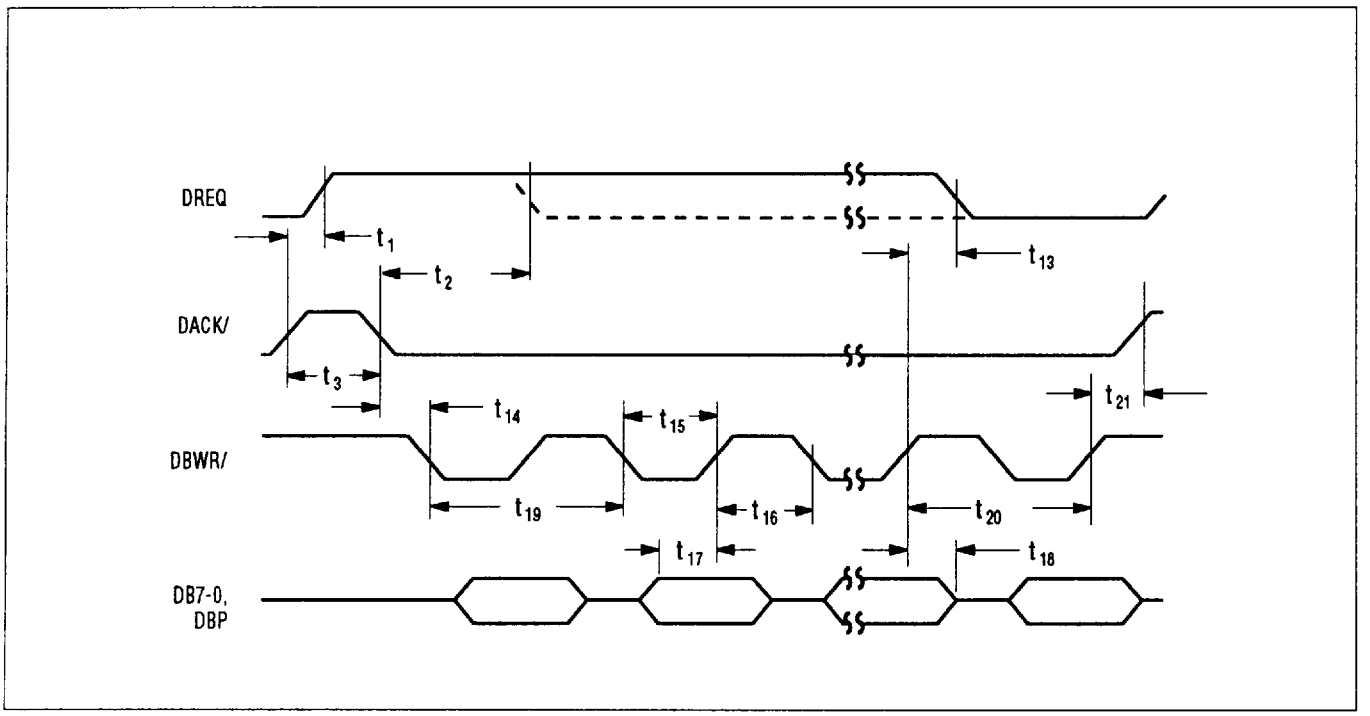


Figure 6-18: Burst Mode DMA Write (Multiplexed Mode)

Table 6-16: Burst Mode DMA Interface (Multiplexed Mode)

Parameter	Symbol	Min	Max	Units	Notes
DACK/ high to DREQ high	t_1	30	-	ns	3
DACK/ low to DREQ low	t_2	-	30	ns	1
DACK/ high to DACK/ low	t_3	t_{CP} + 5	-	ns	-
DBRD/ high to DREQ low	t_4	-	$2t_{CP} + t_{CL}$ +30	ns	2
DACK/ low to DBRD/ low	t_5	0	-	ns	-
DBRD/ pulse width	t_6	t_{CP} + 5	-	ns	-
DBRD/ high to DBRD/ low	t_7	t_{CP} + 5	-	ns	-
DBRD/ low to data valid	t_8	-	30	ns	-
DBRD/ high to data bus disable	t_9	-	30	ns	-
DBRD/ low to DBRD/ low	t_{10}	$3t_{CP}$	-	ns	-
DBRD/ high to DBRD/ high	t_{11}	$3t_{CP}$	-	ns	-
DBRD/ high to DACK/ high	t_{12}	0	-	ns	-
DBWR/ high to DREQ low	t_{13}	-	$2t_{CP} + t_{CL} + 30$	ns	2
DACK/ low to DBWR/ low	t_{14}	0	-	ns	-
DBWR/ pulse width	t_{15}	t_{CP} + 5	-	ns	-
DBWR/ high to DBWR/ low	t_{16}	t_{CP} + 5	-	ns	-
Data setup to DBWR/ high	t_{17}	10	-	ns	-
Data hold from DBWR/ high	t_{18}	4	-	ns	-
DBWR/ low to DBWR/ low	t_{19}	$3t_{CP}$	-	ns	-
DBWR/ high to DBWR/ high	t_{20}	$3t_{CP}$	-	ns	-
DBWR/ high to DACK/ high	t_{21}	0	-	ns	-

1. *Single DMA transfer only.*
2. *Multiple DMA transfers only.*
3. *Assertion pending. If the FIFO is empty during DMA read, or full during DMA write, then assertion will not be pending.*

Burst Mode DMA Interface (Non-Multiplexed Mode)

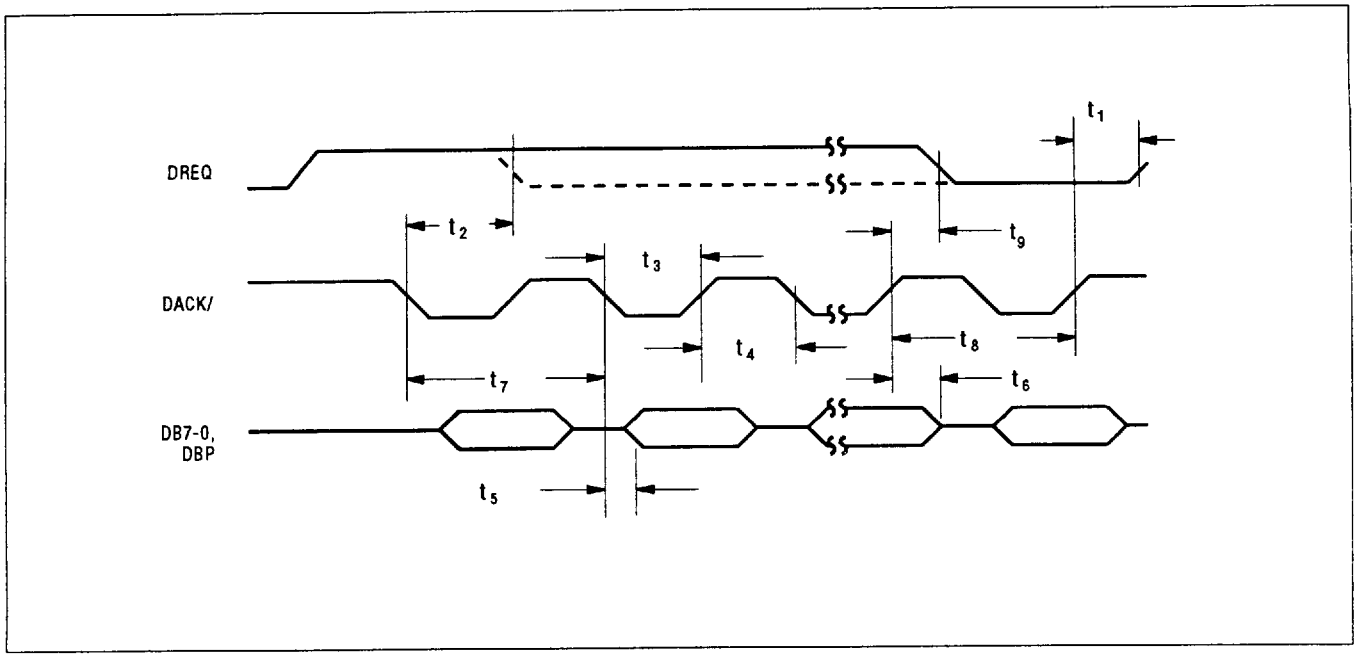


Figure 6-19: Burst Mode DMA Read (Non-Multiplexed Mode)

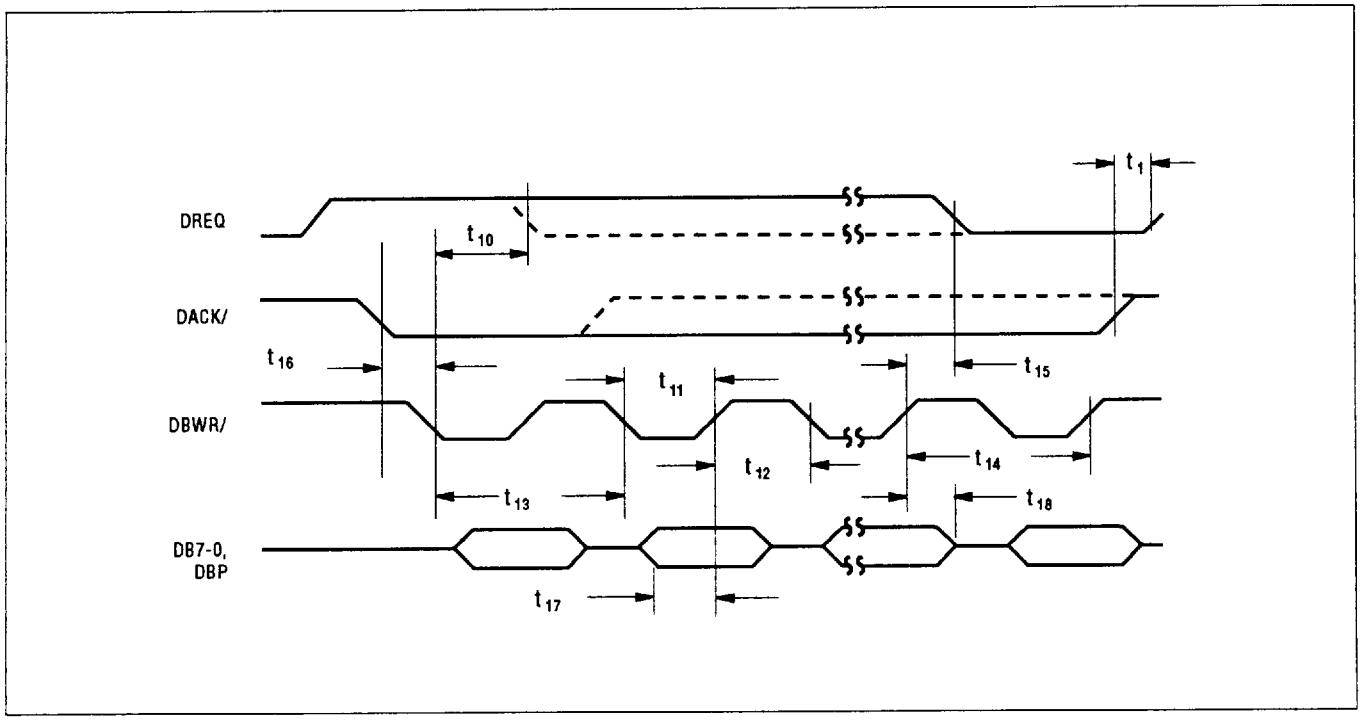


Figure 6-20: Burst Mode DMA Write (Non-Multiplexed Mode)

Table 6-17: Burst Mode DMA Interface (Non-Multiplexed Mode)

Parameter	Symbol	Min	Max	Units	Notes
DACK/ high to DREQ high	t_1	30	-	ns	3
DACK/ low to DREQ low	t_2	-	30	ns	1
DACK/ pulse width	t_3	t_{CP} + 5	-	ns	5
DACK/ high to DACK/ low	t_4	t_{CP} + 5	-	ns	-
DACK/ low to data valid	t_5	-	30	ns	-
DACK/ high to data bus disable	t_6	-	30	ns	-
DACK/ low to DACK/ low	t_7	$3t_{CP}$	-	ns	5
DACK/ high to DACK/ high	t_8	$3t_{CP}$	-	ns	5
DACK/ high to DREQ low	t_9	-	$2t_{CP} + t_{CL} + 30$	ns	2
DBWR/ low to DREQ low	t_{10}	-	30	ns	1, 6
DBWR/ pulse width	t_{11}	t_{CP} + 5	-	ns	6
DBWR/ high to DBWR/ low	t_{12}	t_{CP} + 5	-	ns	6
DBWR/ low to DBWR/ low	t_{13}	$3t_{CP}$	-	ns	6
DBWR/ high to DBWR/ high	t_{14}	$3t_{CP}$	-	ns	6
DBWR/ high to DREQ low	t_{15}	-	$2t_{CP} + t_{CL} + 30$	ns	2, 6
DACK/ low to DBWR/ low	t_{16}	0	-	ns	4, 6
Data setup to DBWR/ high	t_{17}	15	-	ns	6
Data hold from DBWR/ high	t_{18}	4	-	ns	6

1. *Single DMA transfer only.*
2. *Multiple DMA transfers only.*
3. *Assertion pending. If the FIFO is empty during DMA read, or full during DMA write, then assertion will not be pending.*
4. *DBWR/ low may precede DACK/ low.*
5. *DACK/ is used for DMA reads and writes. For DMA reads, DACK/ must toggle, and is assumed to be coincident with an external read signal.*
6. *Either DACK/ or DBWR/ may toggle during a burst write. Timings are shown for DBWR/ toggling; however, DACK/ and DBWR/ may be interchanged in Figure 6-20 and Table 6-17.*

SCSI Timings

Initiator Asynchronous Send

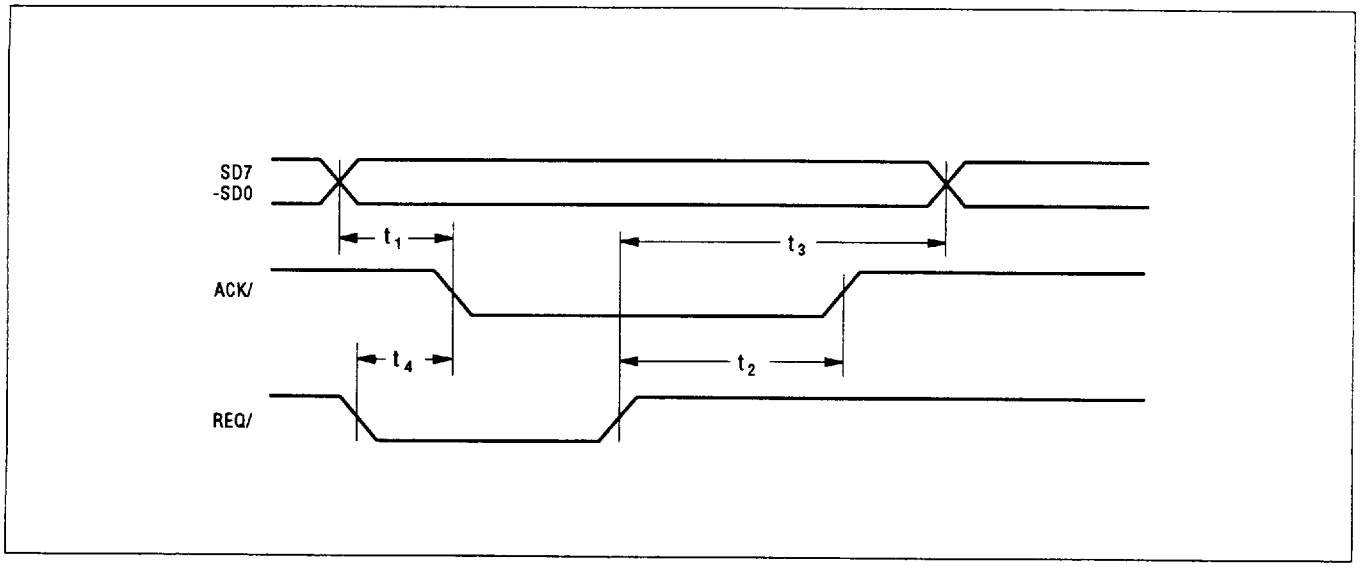


Figure 6-21: Initiator Asynchronous Send

Table 6-18: Initiator Asynchronous Send Timings

Parameter	Symbol	Min	Max	Units
Data setup to ACK/ low	t_1	60	-	ns
ACK/ high from REQ/ high	t_2	10	-	ns
Data hold from REQ/ high	t_3	5	-	ns
ACK/ low from REQ/ low	t_4	10	-	ns

Initiator Asynchronous Receive

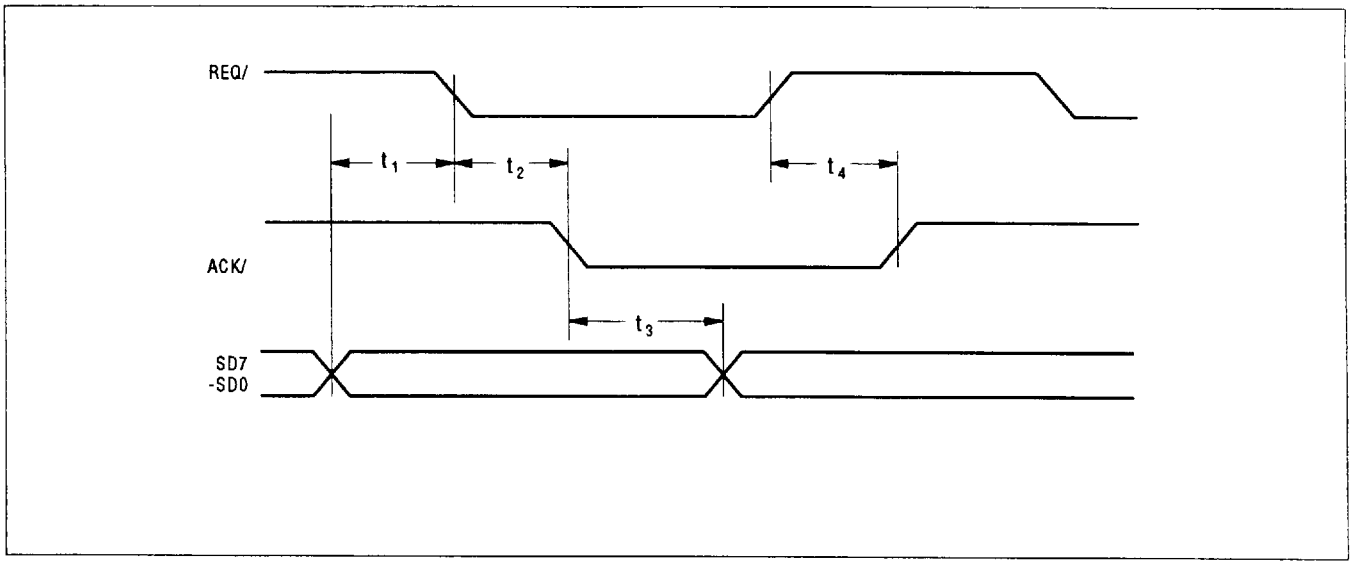


Figure 6-22: Initiator Asynchronous Receive

Table 6-19: Initiator Asynchronous Receive Timings

Parameter	Symbol	Min	Max	Units
Data setup to REQ/ low	t_1	0	-	ns
ACK/ low from REQ/ low	t_2	10	-	ns
Data hold from ACK/ low	t_3	0	-	ns
ACK/ high from REQ/ high	t_4	10	-	ns

Target Asynchronous Send

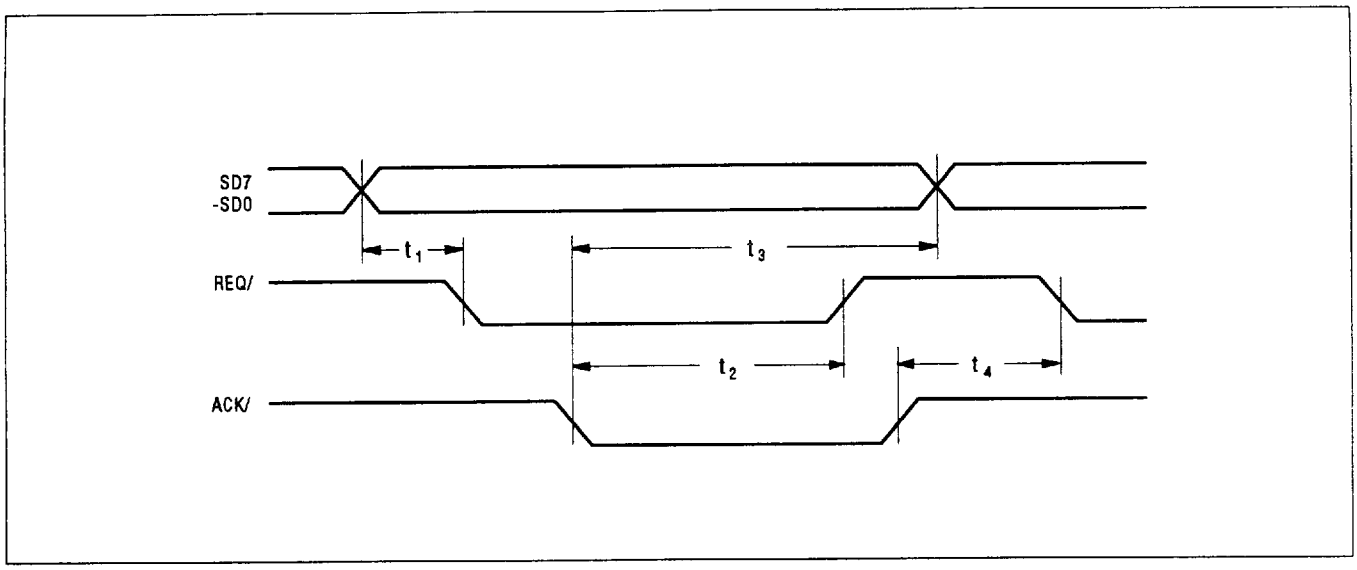


Figure 6-23: Target Asynchronous Send

Table 6-20: Target Asynchronous Send Timings

Parameter	Symbol	Min	Max	Units
Data setup to REQ/ low	t_1	60	-	ns
REQ/ high from ACK/ low	t_2	10	-	ns
Data hold from ACK/ low	t_3	5	-	ns
REQ/ low from ACK/ high	t_4	10	-	ns

Target Asynchronous Receive

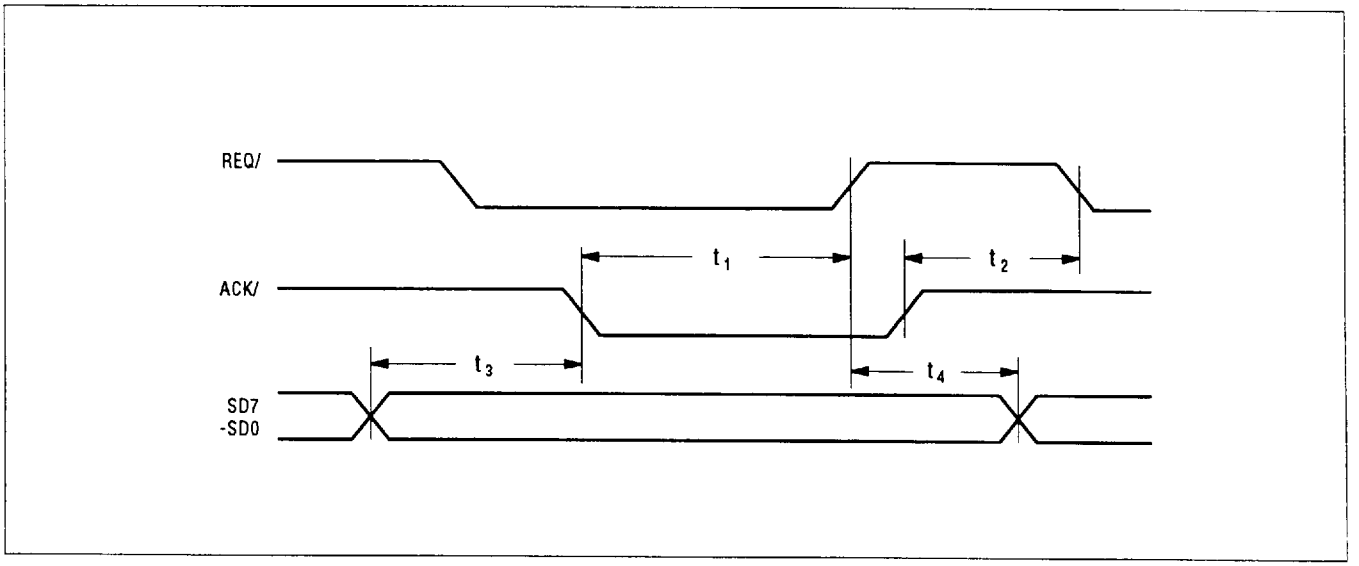


Figure 6-24: Target Asynchronous Receive

Table 6-21: Target Asynchronous Receive Timings

Parameter	Symbol	Min	Max	Units
REQ/ high from ACK/ low	t_1	10	-	ns
REQ/ low from ACK/ high	t_2	10	-	ns
Data setup to ACK/ low	t_3	0	-	ns
Data hold from REQ/ high	t_4	0	-	ns

Target and Initiator Synchronous Transfers

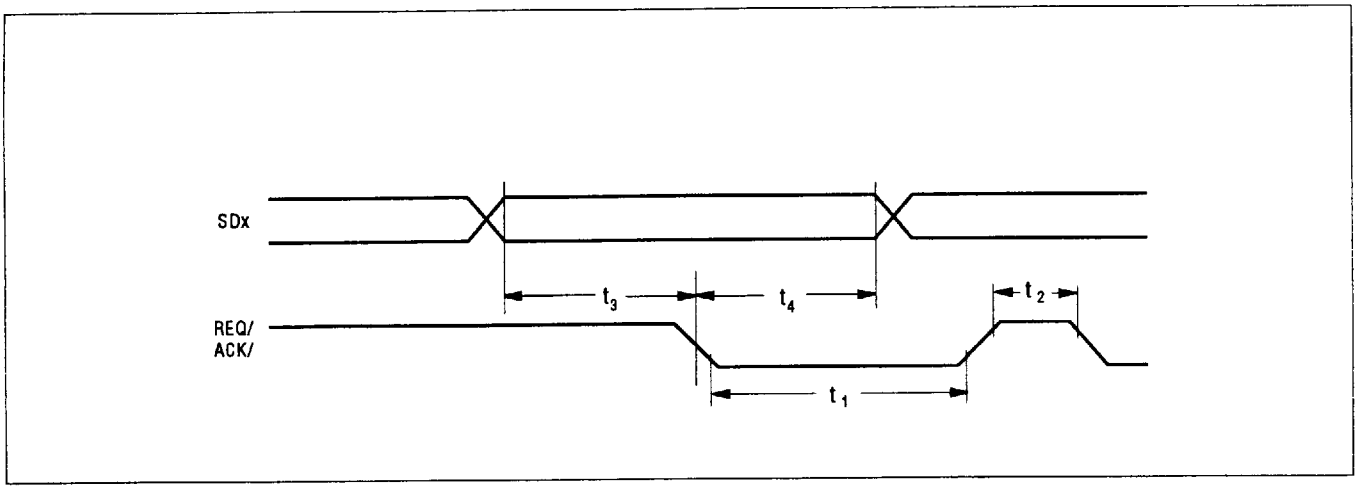


Figure 6-25: Target and Initiator Synchronous Output

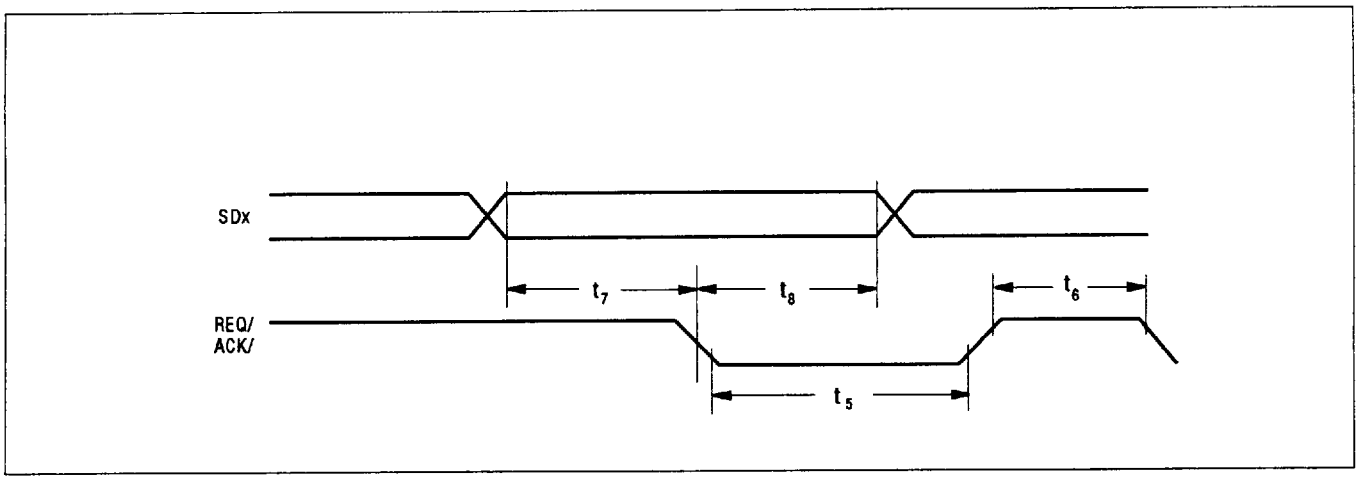


Figure 6-26: Target and Initiator Synchronous Input

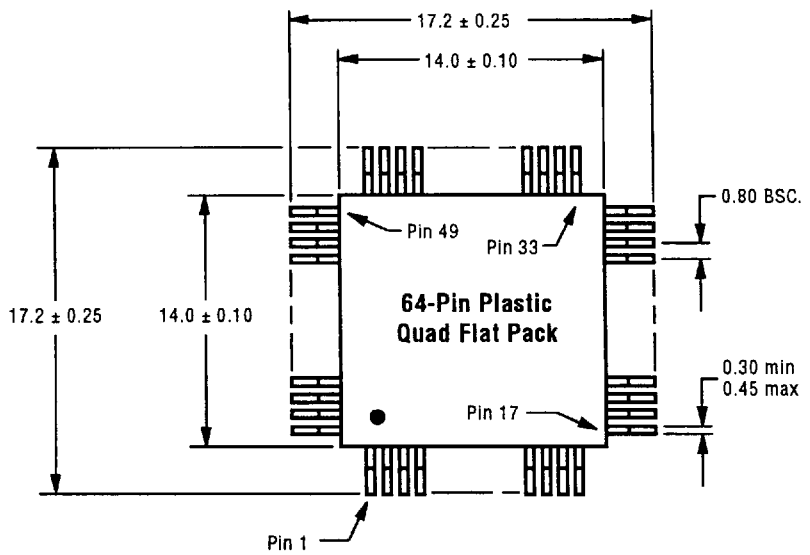
Table 6-22: SCSI-1 Single-Ended Transfers (5 MB/s)

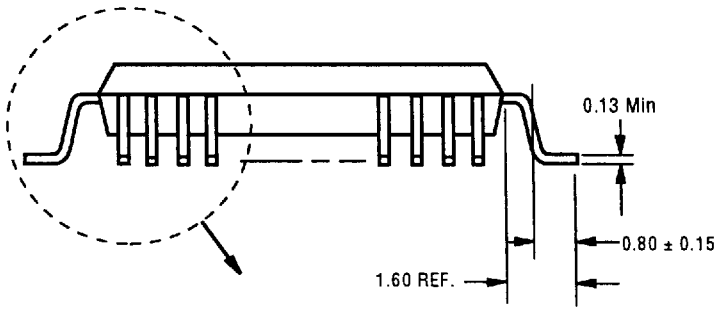
Parameter	Symbol	Min	Max	Units
REQ/ or ACK/ assertion period	t_1	90	-	ns
REQ/ or ACK/ negation period	t_2	90	-	ns
Data setup to REQ/ or ACK/ low	t_3	65	-	ns
Data hold from ACK/ or REQ/ low	t_4	100	-	ns
REQ/ or ACK/ assertion period	t_5	90	-	ns
REQ/ or ACK/ negation period	t_6	90	-	ns
Data setup to REQ/ low or ACK/ low	t_7	0	-	ns
Data hold from REQ/ low or ACK/ low	t_8	45	-	ns

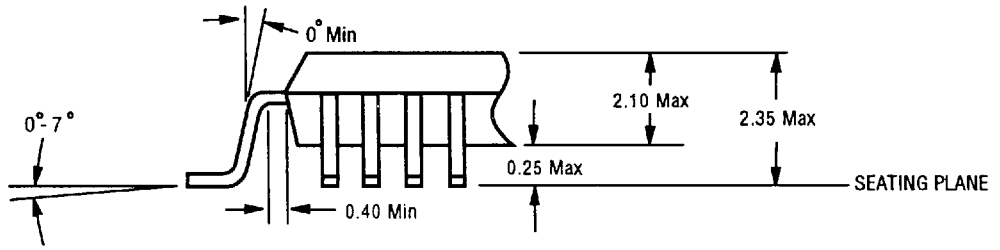
Table 6-23: Fast SCSI-2 Single-Ended Transfers (10 MB/s)

Parameter	Symbol	Min	Max	Units
REQ/ or ACK/ assertion period	t_1	32	-	ns
REQ/ or ACK/ negation period	t_2	32	-	ns
Data setup to REQ/ or ACK/ low	t_3	25	-	ns
Data hold from REQ/ or ACK/ low	t_4	35	-	ns
REQ/ or ACK/ assertion period	t_5	20	-	ns
REQ/ or ACK/ negation period	t_6	20	-	ns
Data setup to REQ/ low or ACK/ low	t_7	0	-	ns
Data hold from REQ/ low or ACK/ low	t_8	10	-	ns

Appendix C
Mechanical Drawings







All dimensions are in millimeters

Figure C-1: 64-Pin Plastic Quad Flat Pack

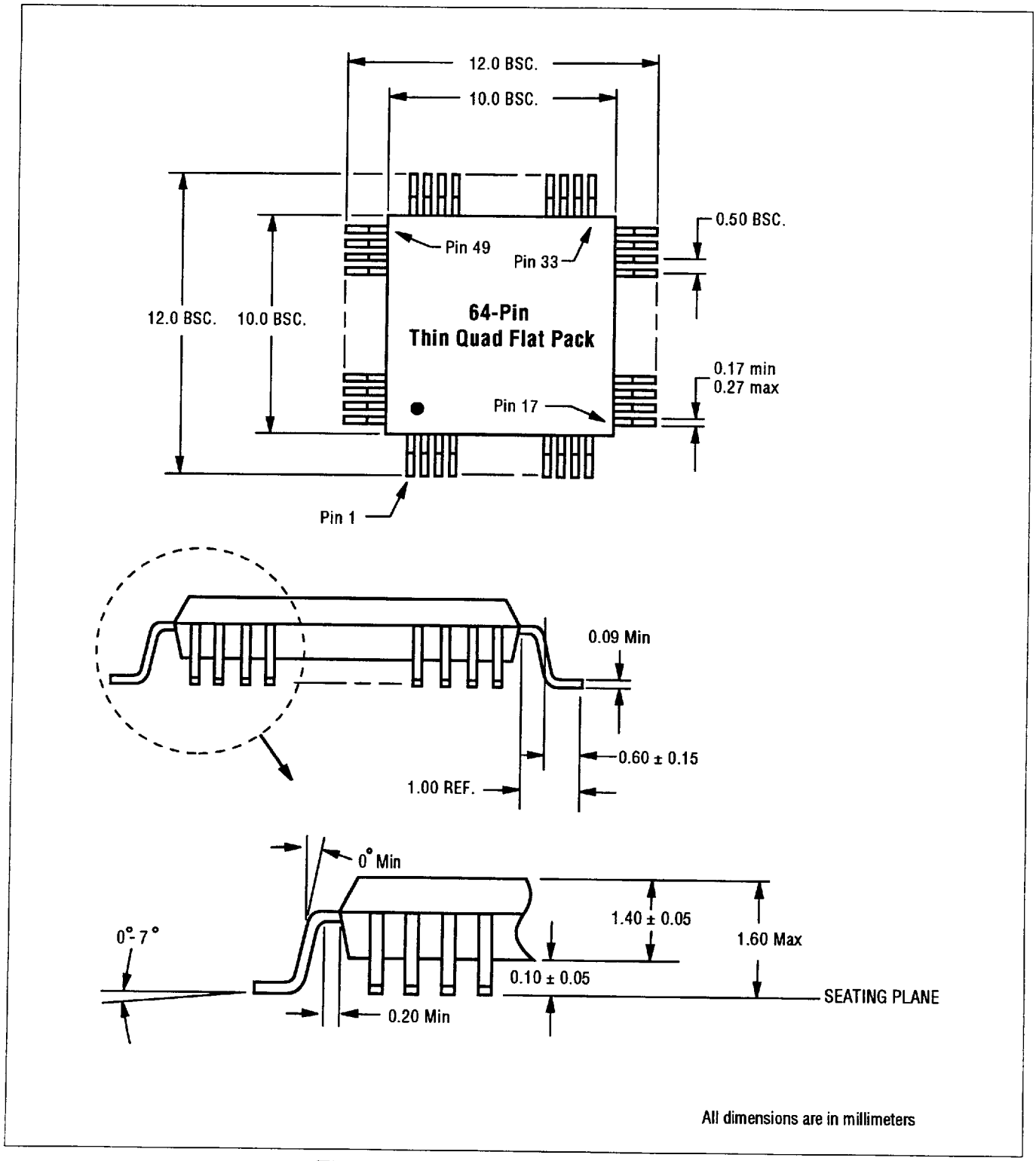


Figure C-2: 64-Pin Thin Quad Flat Pack