

ESD7451, SZESD7451

ESD Protection Diodes Micro-Packaged Diodes for ESD Protection

The ESD7451 is designed to protect voltage sensitive components that require ultra-low capacitance from ESD and transient voltage events. Excellent clamping capability, low capacitance, low leakage, and fast response time, make these parts ideal for ESD protection on designs where board space is at a premium. Because of its low capacitance, the part is well suited for use in high frequency designs such as USB 2.0 high speed and antenna line applications.

Features

- Ultra-Low Capacitance (0.35 pF Max)
- Low Clamping Voltage
- Stand-off Voltage: 3.3 V
- Low Leakage
- Response Time is < 1 ns
- Low Dynamic Resistance < 1 Ω
- Protection for the Following Standards:
IEC 61000-4-2 (Level 4) & ISO 10605
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- RF Signal ESD Protection
- RF Switching, PA, and Antenna ESD Protection
- Near Field Communications

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|-----------------|--|---------------------------|
| Total Power Dissipation on FR-5 Board (Note 1) @ $T_A = 25^\circ\text{C}$ | P_D | 250 | mW |
| Thermal Resistance, Junction-to-Ambient | $R_{\theta JA}$ | 400 | $^\circ\text{C}/\text{W}$ |
| Junction and Storage Temperature Range | T_J, T_{stg} | -55 to +150 | $^\circ\text{C}$ |
| Lead Solder Temperature – Maximum (10 Second Duration) | T_L | 260 | $^\circ\text{C}$ |
| IEC 61000-4-2 Contact IEC 61000-4-2 Air ISO 10605 150 pF/2 k Ω ISO 10605 330 pF/2 k Ω ISO 10605 330 pF/330 Ω | ESD | ± 25 ± 25 ± 30 ± 30 ± 20 | kV |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. FR-5 = 1.0 x 0.75 x 0.62 in.

See Application Note AND8308/D for further description of survivability specs.



ON Semiconductor®

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MARKING DIAGRAM



XDFN2
CASE 711AM



E = Specific Device Code
M = Date Code

ORDERING INFORMATION

| Device | Package | Shipping† |
|----------------|--------------------|--------------------|
| ESD7451N2T5G | XDFN2 (Pb-Free) | 8000 / Tape & Reel |
| SZESD7451N2T5G | XDFN2 (Pb-Free) | 8000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

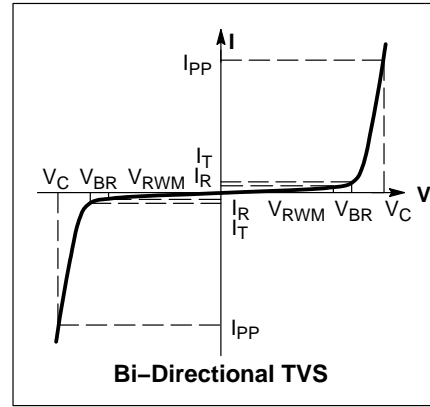
ESD7451, SZESD7451

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Symbol | Parameter |
|-----------|---|
| I_{PP} | Maximum Reverse Peak Pulse Current |
| V_C | Clamping Voltage @ I_{PP} |
| V_{RWM} | Working Peak Reverse Voltage |
| I_R | Maximum Reverse Leakage Current @ V_{RWM} |
| V_{BR} | Breakdown Voltage @ I_T |
| I_T | Test Current |

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|----------------------------|-----------|--|-------------------|--------------|--------------|----------|
| Reverse Working Voltage | V_{RWM} | | | | 3.3 | V |
| Breakdown Voltage (Note 2) | V_{BR} | $I_T = 1\text{ mA}$ | 5.0 | 6.0 | 7.5 | V |
| Reverse Leakage Current | I_R | | | < 1.0 | 50 | nA |
| Clamping Voltage (Note 3) | V_C | $I_{PP} = 1\text{ A}$ $I_{PP} = 3\text{ A}$ | | | 10 13 | V |
| Clamping Voltage, ESD | V_C | Per IEC61000-4-2 Waveform | See Figures 1 & 2 | | | |
| Clamping Voltage, TLP | V_C | $I_{PP} = \pm 8\text{ A}$ $I_{PP} = \pm 16\text{ A}$ | | 13.5 18 | | V |
| Dynamic Resistance | R_{DYN} | TLP Pulse | | 0.55 | | Ω |
| Junction Capacitance | C_J | $V_R = 0\text{ V}, f = 1\text{ MHz}$ $V_R = 0\text{ V}, f = 1\text{ GHz}$ | | 0.25 0.22 | 0.35 0.35 | pF |

- Breakdown voltage is tested from pin 1 to 2 and pin 2 to 1.
- Non-repetitive current pulse at $T_A = 25^\circ\text{C}$, per IEC61000-4-5 waveform shown in Figure 9.

TYPICAL CHARACTERISTICS

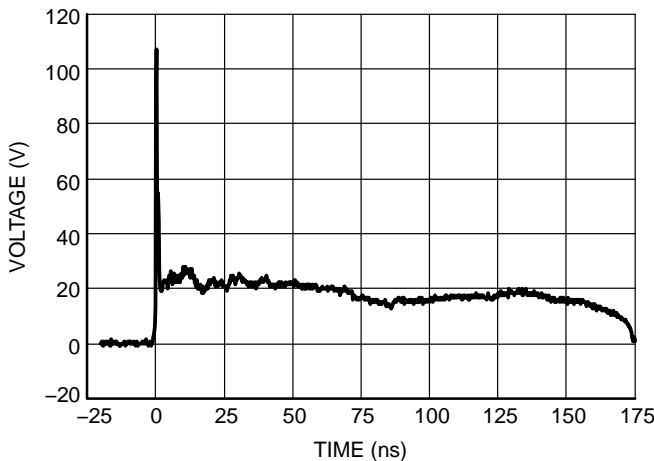


Figure 1. Typical IEC61000-4-2 + 8 kV Contact ESD Clamping Voltage

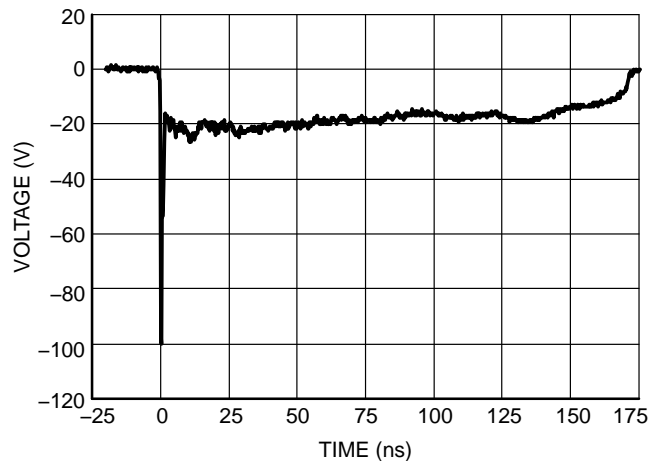


Figure 2. Typical IEC61000-4-2 - 8 kV Contact ESD Clamping Voltage

ESD7451, SZESD7451

IEC 61000-4-2 Spec.

| Level | Test Voltage (kV) | First Peak Current (A) | Current at 30 ns (A) | Current at 60 ns (A) |
|-------|-------------------|------------------------|----------------------|----------------------|
| 1 | 2 | 7.5 | 4 | 2 |
| 2 | 4 | 15 | 8 | 4 |
| 3 | 6 | 22.5 | 12 | 6 |
| 4 | 8 | 30 | 16 | 8 |



Figure 3. IEC61000-4-2 Spec

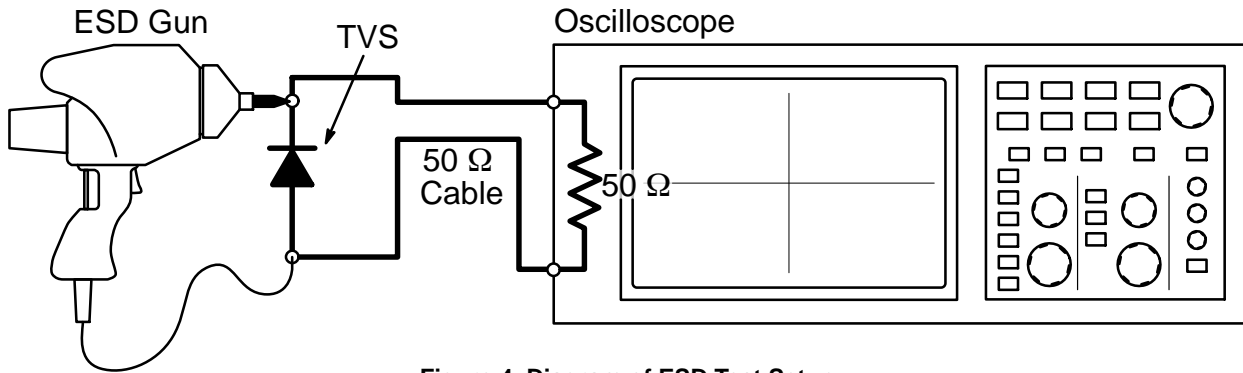


Figure 4. Diagram of ESD Test Setup

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage

at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

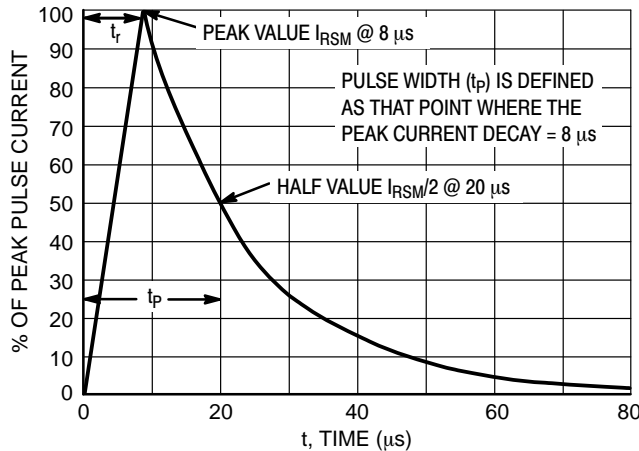


Figure 5. 8 X 20 μs Pulse Waveform

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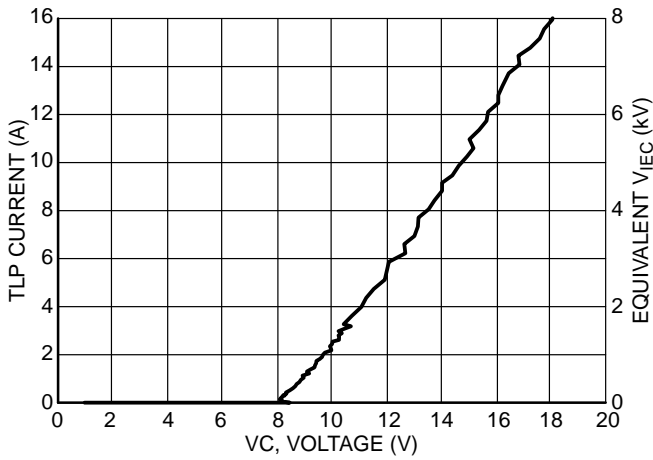


Figure 6. Typical Positive TLP IV Curve

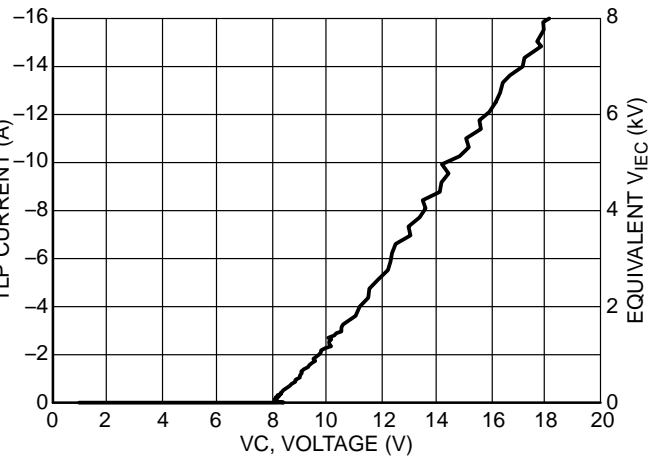


Figure 7. Typical Negative TLP IV Curve

NOTE: TLP parameter: $Z_0 = 50 \Omega$, $t_p = 100 \text{ ns}$, $t_r = 300 \text{ ps}$, averaging window: $t_1 = 30 \text{ ns}$ to $t_2 = 60 \text{ ns}$.

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I-V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 8. TLP I-V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 9 where an 8 kV IEC 61000-4-2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I-V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

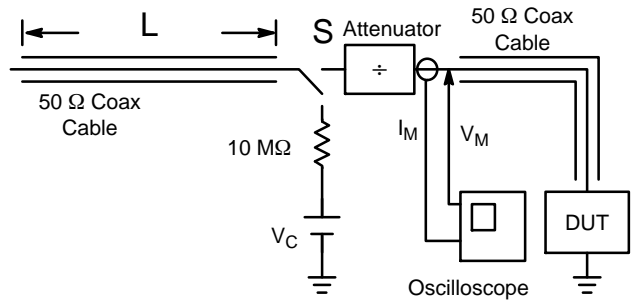


Figure 8. Simplified Schematic of a Typical TLP System

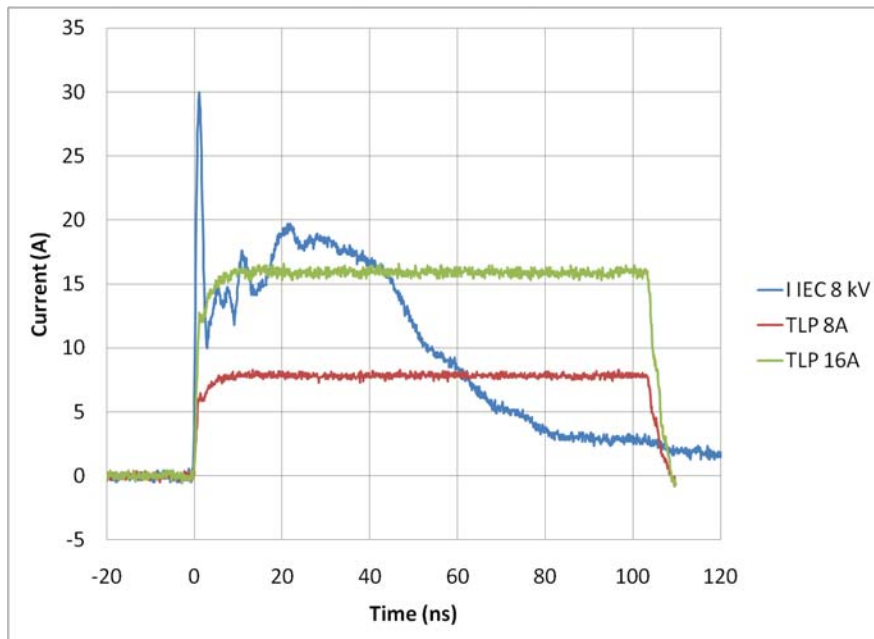


Figure 9. Comparison Between 8 kV IEC 61000-4-2 and 8 A and 16 A TLP Waveforms

ESD7451, SZESD7451

TYPICAL CHARACTERISTICS

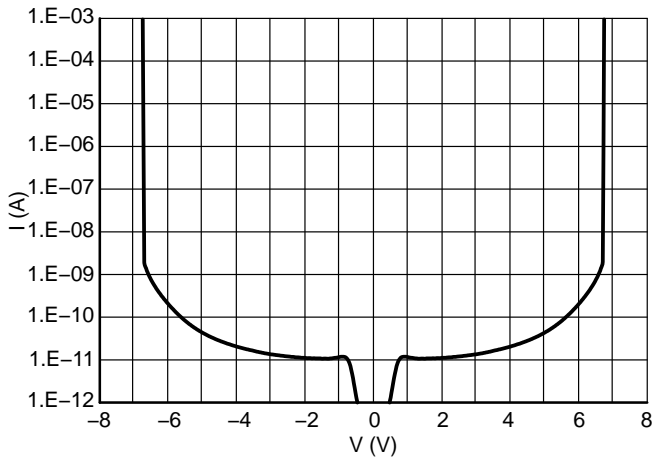


Figure 10. IV Characteristics

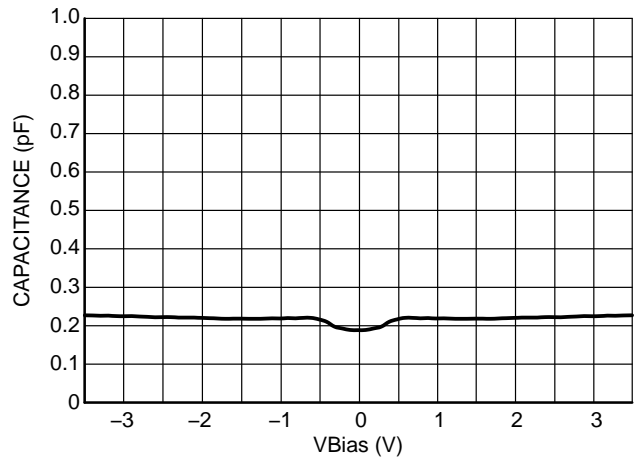


Figure 11. CV Characteristics

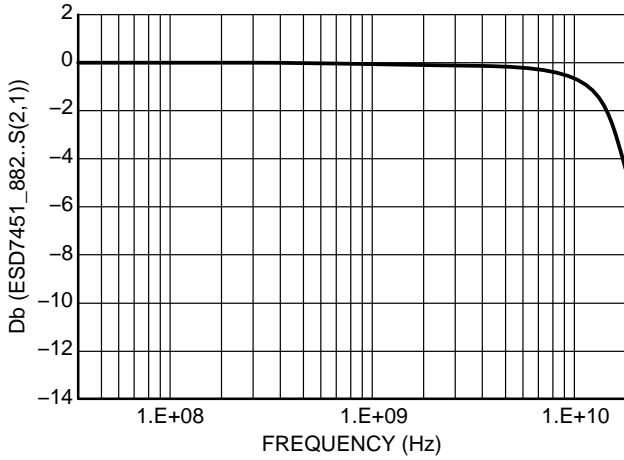


Figure 12. RF Insertion Loss

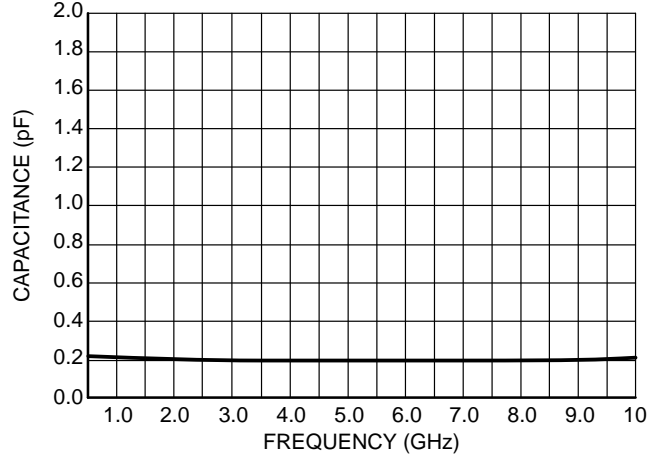
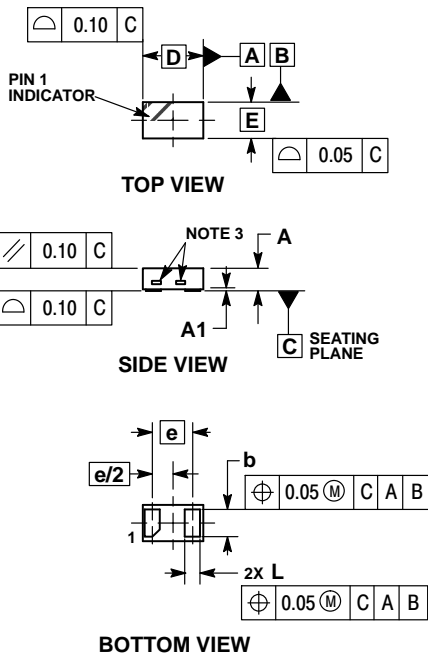


Figure 13. Capacitance over Frequency

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PACKAGE DIMENSIONS

XDFN2 1.0x0.6, 0.65P (SOD-882) CASE 711AM ISSUE O

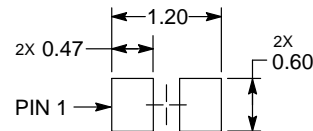


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. EXPOSED COPPER ALLOWED AS SHOWN.

| MILLIMETERS | | |
|-------------|----------|------|
| DIM | MIN | MAX |
| A | 0.34 | 0.44 |
| A1 | --- | 0.05 |
| b | 0.43 | 0.53 |
| D | 1.00 BSC | |
| E | 0.60 BSC | |
| e | 0.65 BSC | |
| L | 0.20 | 0.30 |

RECOMMENDED SOLDER FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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