

## P-Channel Enhancement Mode Field Effect Transistor

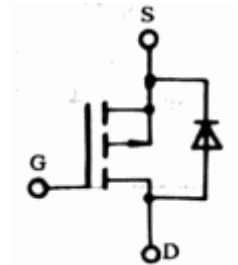
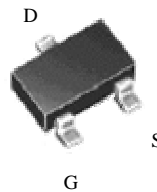
### FEATURES

- Super high dense cell design for low  $R_{DS(ON)}$
- Rugged and reliable
- Simple drive requirement
- SOT-23 package

PRODUCT SUMMARY		
$V_{DSS}$	$I_D$	$R_{DS(ON)}$ (m $\Omega$ ) Typ
-20V	-4.0A	95 @ $V_{GS}=-4.5V$
		115 @ $V_{GS}=-2.5V$



NOTE: The Si2305 is available in a lead-free package



### ABSOLUTE MAXIMUM RATINGS ( $T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-20	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	V
Drain Current-Continuous <sup>a</sup> @ $T_j=125^\circ C$ - Pulse $d^b$	$I_D$	-4.0	A
	$I_{DM}$	-12	A
Drain-source Diode Forward Current <sup>a</sup>	$I_S$	-1.25	A
Maximum Power Dissipation <sup>a</sup>	$P_D$	1.25	W
Operating Junction and Storage Temperature Range	$T_j, T_{STG}$	-55 to 150	$^\circ C$

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to Ambient <sup>a</sup>	$R_{th JA}$	100	$^\circ C/W$
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# Si2305



## ELECTRICAL CHARACTERISTICS (T<sub>A</sub>=25°C unless otherwise noted)

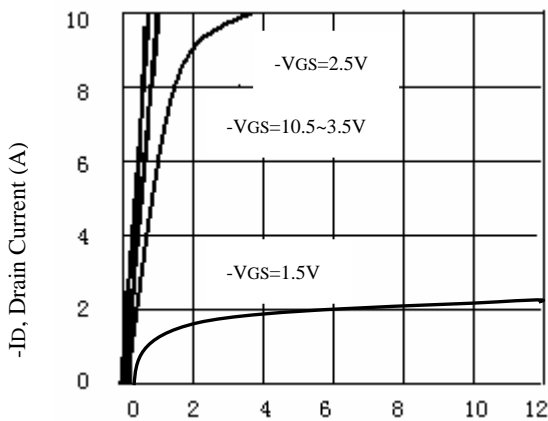
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =-250μA	-20			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-16V, V <sub>GS</sub> =0V			1	μA
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> =±10V, V <sub>DS</sub> =0V			±100	nA
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-0.5	-0.8	-1.5	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-4.0A		95	110	mΩ
		V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-2.0A		115	145	
Forward Transconductance	g <sub>FS</sub>	V <sub>GS</sub> =-5V, I <sub>D</sub> =-5A		5		S
<b>DAYNAMIC CHARACTERISTICS</b>						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =-10V, V <sub>GS</sub> =0V f=1.0MHz		586		pF
Output Capacitance	C <sub>OSS</sub>			101		pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			59		pF
<b>SWITCHING CHARACTERISISTICS</b>						
Turn-On Delay Time	t <sub>D(ON)</sub>	V <sub>DD</sub> =-10V I <sub>D</sub> =-4.0A, V <sub>GEN</sub> =-4.5V R <sub>L</sub> =10ohm R <sub>GEN</sub> =6ohm		6.5		ns
Rise Time	t <sub>r</sub>			32.1		ns
Turn-Off Delay Time	t <sub>D(OFF)</sub>			58.4		ns
Fall Time	t <sub>f</sub>			48		ns
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =-10V, I <sub>D</sub> =-3A V <sub>GS</sub> =-4.5V		6		nC
Gate-Source Charge	Q <sub>gs</sub>			1.35		nC
Gate-Drain Charge	Q <sub>gd</sub>			1.5		nC

## ELECTRICAL CHARACTERICS (TA=25°C unless otherwise noted)

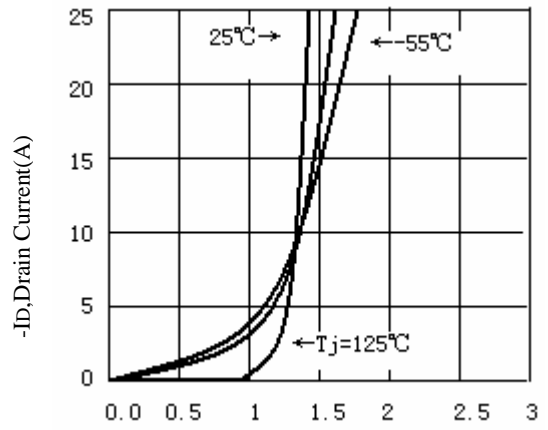
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b>						
Diode Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =-1.25A		-0.81	-1.2	V

### Notes

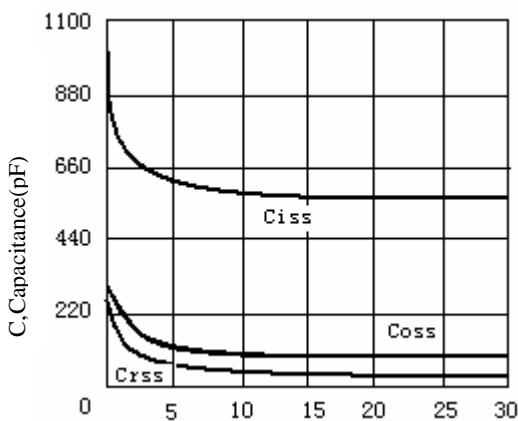
- Surface Mounted on FR4 Board,  $t \leq 10\text{sec}$
- Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty  $\leq 2\%$
- Guaranteed by design, not subject to production testing.



- V<sub>DS</sub>, Drain-to-Source Voltage (V)  
Figure 1. Output Characteristics



- V<sub>GS</sub>, Gate-to-source Voltage (V)  
Figure 2. Transfer Characteristics



- V<sub>GS</sub>, Drain-to Source Voltage  
Figure3. Capacitance

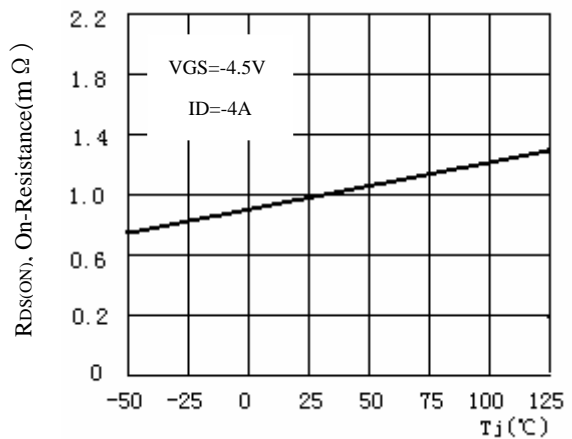
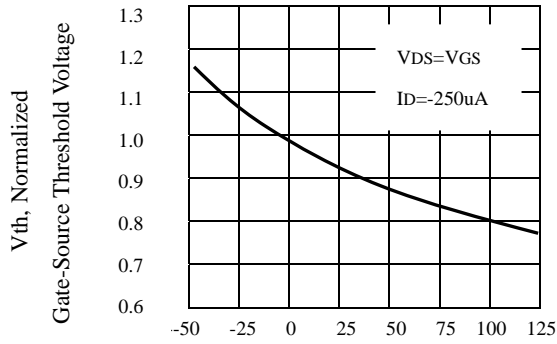
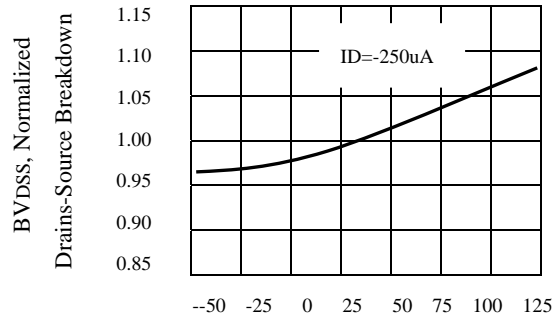


Figure4. On-Resistance Variation with Temperature

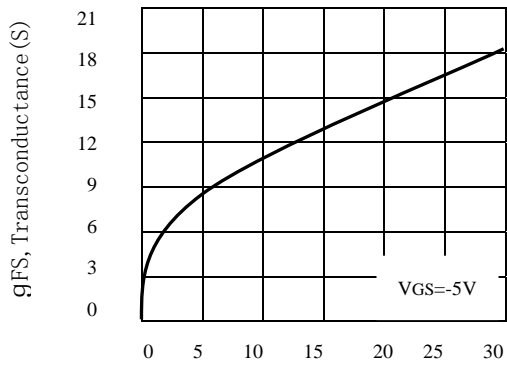
# Si2305



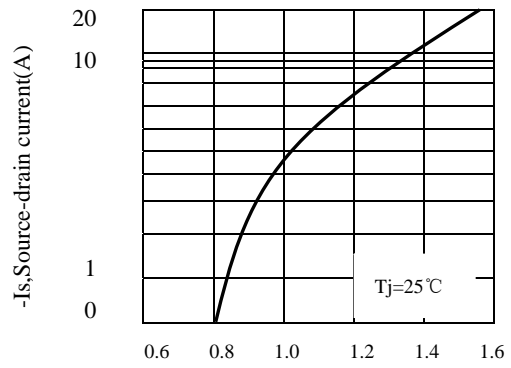
Tj, Junction Temperature(°C)  
Figure5.Gate Threshold Variation With Temperature



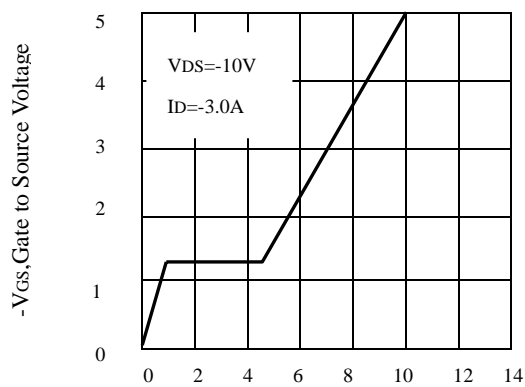
Tj, Junction Temperature (°C)  
Figure6.Breakdown Voltage Variation With Temperature



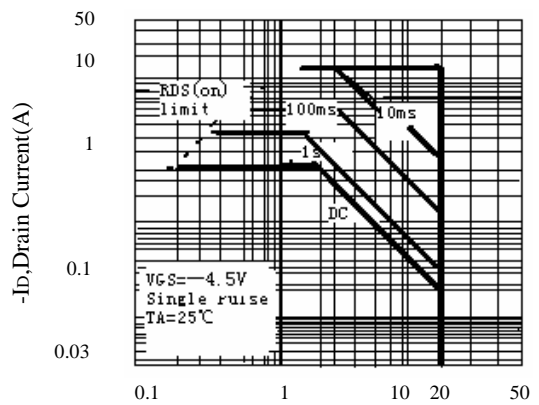
-IDS, Drain-Source Current (A)  
Figure7.Transconductance Variation With Drain Current



-VSD, Body Diode Forward Voltage  
Figure8.Body Diode Forward Voltage Variation with Source Current



Qg, Total Gate Charge (nC)  
Figure9. Gate Charge



-VDS, Drain-Source Voltage(V)  
Figure10.Maximum Safe Operating Area