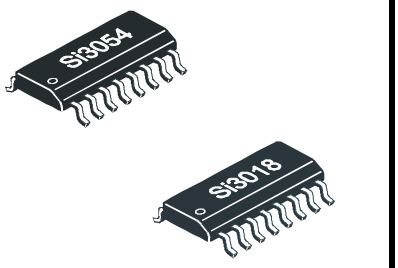
Si3054/Si3018

SYSTEM-SIDE REV E OR LATER

GLOBAL DUAL MODE HD AUDIO/AC'97 SILICON DAA

Features

- Intel® HD Audio and AC'97 2.3 compliant with patented serial bus autodetection
- Global phone line interface
- Compliant with FCC, TBR21, JATE, and other PTTs
- 80 dB dynamic range TX/RX paths
- 3.3 V digital power supply
- Greater than 5000 V isolation
- Caller ID support
- Integrated ring detector
- Integrated analog front end
- 2- to 4-wire hybrid
- Low-power standby mode
- Patented isolation technology
- Wake-on-ring and ring validation
- PnP EPROM interface
- Available in lead-free/RoHS-compliant packages



Ordering Information:

See page 113.

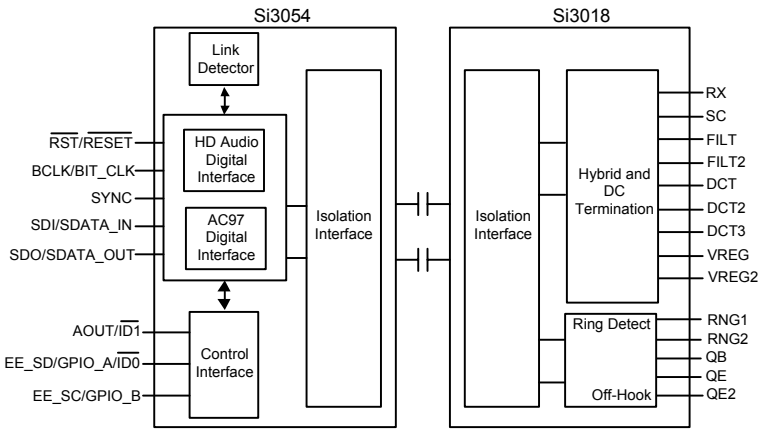
Applications

- Software modems
- Communications/network riser (CNR)
- Mobile daughter cards (MDC)
- Mini PCI cards
- Audio/modem riser cards

Description

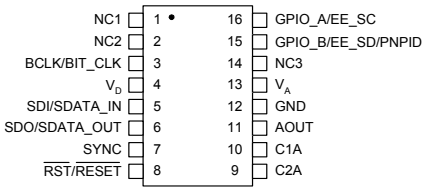
The Si3054/18 is an integrated direct access arrangement (DAA) chipset that provides a digital programmable line interface to meet global telephone line requirements. Available in two 16-pin small outline packages (Si3054 digital interface and Si3018 phone-line interface), the chipset eliminates the need for an analog front end (AFE), isolation transformer, relays, opto-isolators, and a 2- to 4-wire hybrid. The Si3054/18 dramatically reduces the number of discrete components and cost required to achieve compliance with global regulatory requirements. The digital dual interface Si3054 complies with both the AC'97 2.3 and Intel®HD Audio 1.0 specifications and automatically configures itself to support AC-link or HD Audio signalling through a patented serial bus autodetection block.

Functional Block Diagram

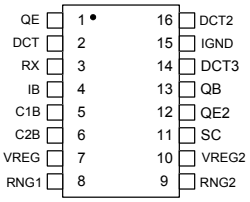


Pin Assignments

Si3054
(Revision E or Later)



Si3018



Patent # 5,870,046
Patent # 6,061,009
Other patents pending

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Section **Page**

1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter[1]	Symbol	Test Condition	Min[2]	Typ	Max[2]	Unit
Ambient Temperature[3]	T_A	F/K-Grade	0	25	70	°C
Si3054 Supply Voltage, Digital[4]	V_D	3.3 V Signaling	3.0	3.3	3.6	V

Notes:

1. The Si3054 specifications are guaranteed when the typical application circuit (including component tolerances) of the "2.Typical Application Schematic," on page 17 and any Si3054 and Si3018 are used.
2. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.
3. The temperature specifications are guaranteed when using the typical application circuit on a 4 sq. in. minimum FR4 PCB. For other materials and smaller form factors, heat dissipation factors may apply. Contact Silicon Laboratories for more details.
4. 3.3 V operation applies to the AC '97 Digital Interface, the HD Audio Digital Interface, and the $\overline{\text{RST}}$/$\overline{\text{RESET}}$ signals.

Table 2. Loop Characteristics

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C, See Figure 1)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Termination Voltage	V_{TR}	I_L = 20 mA, ILIM = 0, DCV = 00, MINI = 11, DCR = 0	—	—	6.0	V
DC Termination Voltage	V_{TR}	I_L = 120 mA, ILIM = 0, DCV = 00, MINI = 11, DCR = 0	9	—	—	V
DC Termination Voltage	V_{TR}	I_L = 20 mA, ILIM = 0, DCV = 11, MINI = 00, DCR = 0	—	—	7.5	V
DC Termination Voltage	V_{TR}	I_L = 120 mA, ILIM = 0, DCV = 11, MINI = 00, DCR = 0	9	—	—	V
DC Termination Voltage	V_{TR}	I_L = 20 mA, ILIM = 1, DCV = 11, MINI = 00, DCR = 0	—	—	7.5	V
DC Termination Voltage	V_{TR}	I_L = 60 mA, ILIM = 1, DCV = 11, MINI = 00, DCR = 0	40	—	—	V
DC Termination Voltage	V_{TR}	I_L = 50 mA, ILIM = 1, DCV = 11, MINI = 00, DCR = 0	—	—	40	V
DC Termination Voltage	V_{TR}	I_L = 20 mA, ILIM = 0, DCV = 11, MINI = 00, DCR = 1	—	—	16	V
DC Termination Voltage	V_{TR}	I_L = 60 mA, ILIM = 0, DCV = 11, MINI = 00, DCR = 1	40	—	—	V
On Hook Leakage Current	I_{LK}	V_{TR} = –48V	—	—	35	µA
Operating Loop Current	I_{LP}	MINI = 00, ILIM = 0	10	—	120	mA
Operating Loop Current	I_{LP}	MINI = 00, ILIM = 1	10	—	60	mA
DC Ring Current		dc current flowing through ring detection circuitry	—	1.5	3	µA
Ring Detect Voltage*	V_{RD}	RT = 0	13.5	15	16.5	V_{rms}
Ring Detect Voltage*	V_{RD}	RT = 1	19.35	21.5	23.65	V_{rms}
Ring Frequency	F_R		15	—	68	Hz
Ringer Equivalence Number	REN		—	—	0.2	

***Note:** The ring signal is guaranteed not to be detected below the minimum. The ring signal is guaranteed to be detected above the maximum.

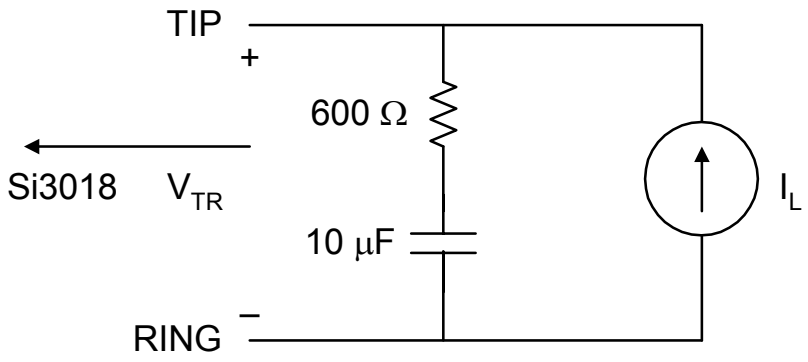


Figure 1. Test Circuit for Loop Characteristics

Table 3. AC Characteristics

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Sample Rate	F_S		7.2	—	16	kHz
Receive Frequency Response		Low –3 dBFS Corner	—	5	—	Hz
Transmit Full Scale Level[1]	V_{FS}	0 dBm	—	1.1	—	V_{PEAK}
Receive Full Scale Level[1,2]	V_{FS}	0 dBm	—	1.1	—	V_{PEAK}
Dynamic Range[3,4,5]	DR	ILIM = 0, DCV = 11, MINI = 00, DCR = 0, IL = 100 mA	—	80	—	dB
Dynamic Range[3,4,5]	DR	ILIM = 0, DCV = 00, MINI = 11, DCR = 0, IL = 20 mA	—	80	—	dB
Dynamic Range[3,4,5]	DR	ILIM = 0, DCV = 11, MINI = 00, DCR = 0, IL = 50 mA	—	80	—	dB
Transmit Total Harmonic Distortion[5,6]	THD	ILIM = 0, DCV = 11, MINI = 00, DCR = 0, IL = 100 mA	—	72	—	dB
Transmit Total Harmonic Distortion[5,6]	THD	ILIM = 0, DCV = 00, MINI = 11, DCR = 0, IL = 20 mA	—	78	—	dB
Receive Total Harmonic Distortion[5,6]	THD	ILIM = 0, DCV = 00, MINI = 11, DCR = 0, IL = 20 mA	—	78	—	dB
Receive Total Harmonic Distortion[5,6]	THD	ILIM = 1, DCV = 11, MINI = 00, DCR = 0, IL = 50 mA	—	78	—	dB
Dynamic Range (Caller ID mode)[7]	DR_{CID}	VIN = 1 kHz, –13 dBm	—	50	—	dB
Caller ID Full Scale Level	V_{CID}		—	6	—	V_{PP}

Notes:

1. Measured at TIP and RING with 600 Ω termination at 1 kHz, as shown in Figure 1.
2. Receive full scale level produces –0.9 dBFS at SDO/SDATA_OUT.
3. DR = 20 x log (RMS V_{FS}/RMS V_{IN}) + 20 x log (RMS V_{IN} / RMS noise). The RMS noise measurement excludes harmonics. V_{FS} is the 0 dBm full-scale level.
4. Measurement is 300 to 3400 Hz. Applies to both transmit and receive paths.
5. Vin = 1 kHz, –3 dBFS.
6. THD = 20 x log (RMS distortion/RMS signal).
7. DR_{CID} = 20 x log (RMS V_{CID}/RMS V_{IN}) + 20 x log (RMS V_{IN} / RMS noise). V_{CID} is the 6 V full-scale level

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_D	–0.5 to 6.0	V
Input Current, Si3054 Digital Input Pins	I_{IN}	±10	mA
Digital Input Voltage	V_{IND}	–0.3 to (V_D + 0.3)	V
Operating Temperature Range	T_A	–40 to 100	°C
Storage Temperature Range	T_{STG}	–65 to 150	°C

Note: Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. AC Link DC Characteristics

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.4	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	I_O = –2 mA	2.4	—	—	V
Low Level Output Voltage	V_{OL}	I_O = 2 mA	—	—	0.35	V
Input Leakage Current	I_L		–10	—	10	µA
Power Supply Current, Digital (D0)	I_D	No load, No external components	—	12	14.5	mA
Total Supply Current, Sleep Mode (D3)	I_D	No load, No external components	—	—	2	mA
Total Supply Current, Sleep Mode (D3)	I_D	Using typical application circuit	—	1.2	—	mA

Table 6. AC Link Timing Characteristics—Cold Reset

(V_D = 3.0 to 3.6 V, T_A = 25°C, C_L = 50 pF)

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{\text{RESET}}$ Active Low Pulse Width	T_{rst_low}	1.0	—	—	µs
$\overline{\text{RESET}}$ Inactive to BIT_CLK Startup Delay	$T_{rst2clk}$	162.8	—	—	ns

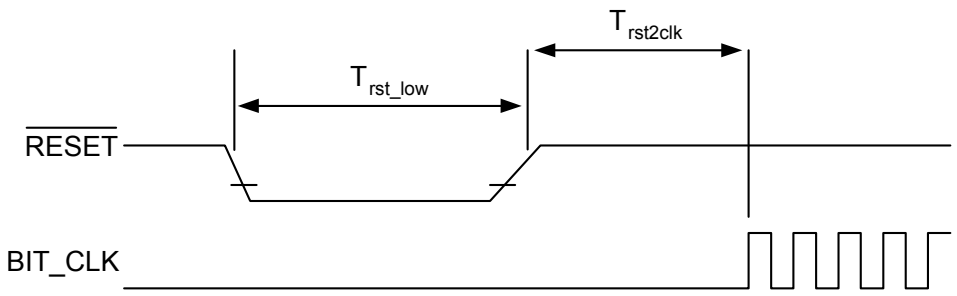


Figure 2. Cold Reset Timing Diagram

Table 7. AC Link Timing Characteristics—Warm Reset

(V_D = 3.0 to 3.6 V, T_A = 25 °C, C_L = 50 pF)

Parameter	Symbol	Min	Typ	Max	Unit
SYNC Active High Pulse Width	T_{sync_high}	1.0	—	—	µs
SYNC Inactive to BIT_CLK Startup Delay	$T_{sync2clk}$	162.8	—	—	ns

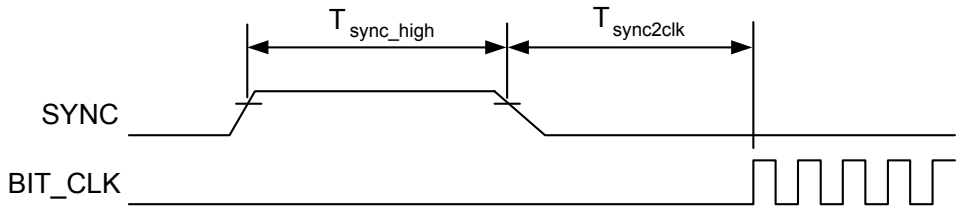


Figure 3. Warm Reset Timing Diagram

Table 8. AC Link Timing Characteristics—Clocks

(V_D = 3.0 to 3.6 V, T_A = 25 °C, C_L = 50 pF)

Parameter	Symbol	Min	Typ	Max	Unit
BIT_CLK Frequency		—	12.288	—	MHz
BIT_CLK Period	T_{clk_period}	—	81.4	—	ns
BIT_CLK High Pulse Width*	T_{clk_high}	—	40.7	—	ns
BIT_CLK low Pulse Width*	T_{clk_low}	—	40.7	—	ns
SYNC Frequency		—	48.0	—	kHz
SYNC Period	T_{sync_period}	—	20.8	—	µs
SYNC High Pulse Width	T_{sync_high}	—	1.3	—	µs
SYNC Low Pulse Width	T_{sync_low}	—	19.5	—	µs
***Note:** Worst case duty cycle restricted to 45/55.					

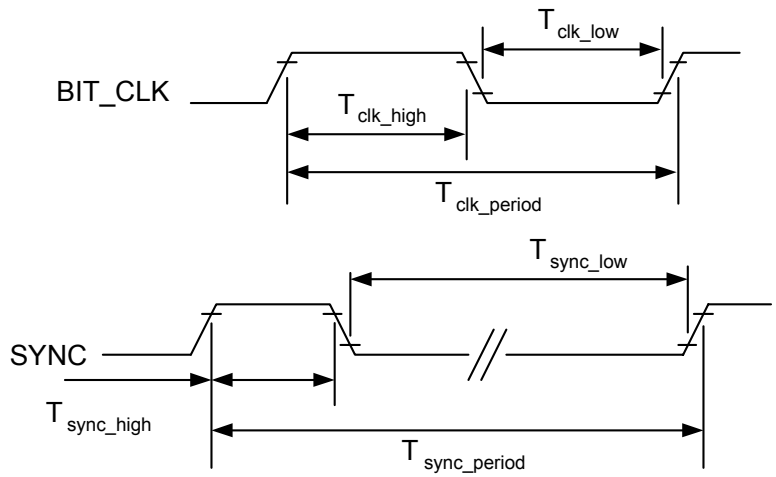


Figure 4. Clocks Timing Diagram

Table 9. AC Link Timing Characteristics—Data Setup and Hold

(V_D = 3.0 to 3.6 V, T_A = 25 °C, C_L = 50 pF)

Parameter	Symbol	Min	Typ	Max	Unit
Setup to Falling Edge of BIT_CLK	T_{setup}	15.0	—	—	ns
Hold from Falling Edge of BIT_CLK	T_{hold}	5.0	—	—	ns

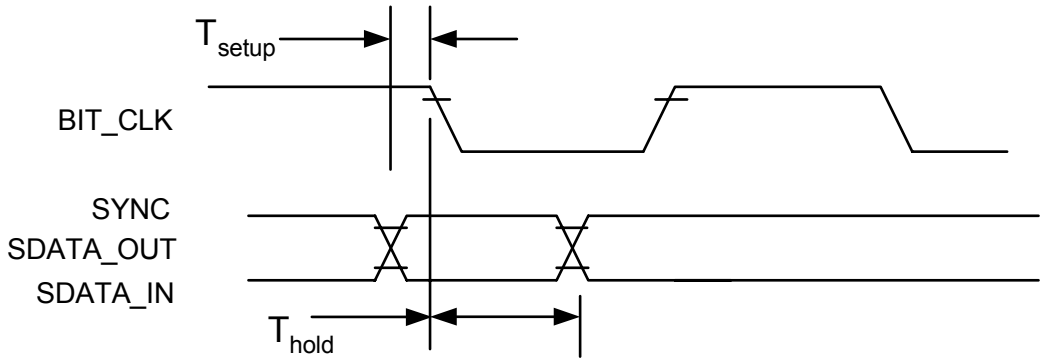


Figure 5. Data Setup and Hold Timing Diagram

Table 10. AC Link SDATA_IN Rise and Fall Times*

(V_D = 3.0 to 3.6 V, T_A = 25 °C, C_L = 50 pF)

Parameter	Symbol	Min	Typ	Max	Unit
SDATA_IN Rise Time	$Trise_{din}$	—	—	6	ns
SDATA_IN Fall Time	$Tfall_{din}$	—	—	6	ns
***Note:** Other ac link signals are inputs to Si3054 Rev. E or later.					

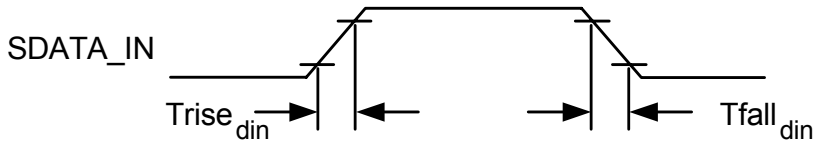
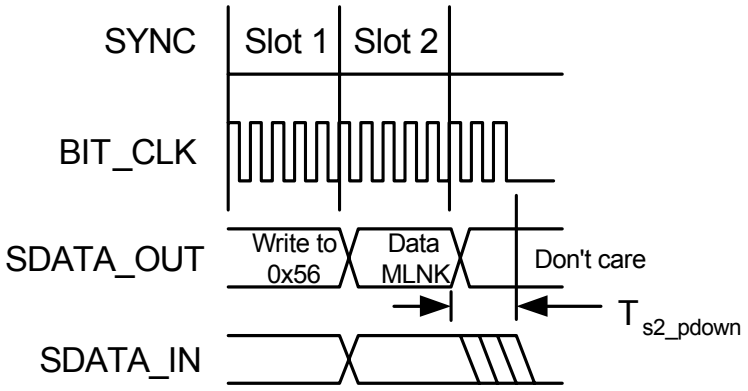


Figure 6. Signal Rise and Fall Timing Diagram

Table 11. AC Link Timing Characteristics—Low Power Mode Timing
(V_D = 3.0 to 3.6 V, T_A = 25 °C, C_L = 50 pF)

Parameter	Symbol	Min	Typ	Max	Unit
End of Slot 2 to BIT_CLK, SDATA_IN Low	T_{s2_pdown}	—	—	1.0	µs



Note: BIT_CLK not to scale

Figure 7. AC-Link Low Power Mode Timing Diagram

Table 12. HD Audio Interface DC Characteristics
(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage	V_D		3.0	—	3.6	V
Input High Voltage	V_{IH}		0.65 V_D	—	—	V
Input Low Voltage	V_{IL}		—	—	0.35 V_D	V
Output High Voltage	V_{OH}	I_{OUT} = –500 µA	0.9 V_D	—	—	V
Output Low Voltage	V_{OL}	I_{OUT} = 1500 µA	—	—	0.1 V_D	V
Input Leakage Current[1]	L_{IL}	0 < V_{IN} < V_{CC}	—	—	±10	µA
Power Supply Current, Digital (D0)	I_D	No load, no external components	—	12	14.5	mA
Total Supply Current, Sleep Mode (D3)	I_D	No load, no external components	—	—	2	mA
Total Supply Current, Sleep Mode (D3)	I_D	Using typical application circuit	—	2.4	—	mA

Notes:
1. For SDI buffers (or in general, any bidirectional buffer with tri-state output), input leakage current also includes hi-Z output leakage.

Table 13. HD Audio Timing Characteristics—Link Reset (Powerup)
(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
RST, SYNC, SDO Low after BCLK Startup	T_{RST_d}	100	—	—	µs
DELAY TIME, SYNC High after RST	T_{SYNC_d}	166.7	—	—	ns
HOLD TIME, SYNC High	T_H	—	166.7	—	ns
HOLD TIME, SDI High	T_{H2}	—	41.7	—	ns
DELAY TIME, SDI Low after SYNC High	T_{SDI_d}	—	125	—	ns
Note: The SDI initialization request on SDI must be coincident with the first Frame Sync (falling edge of SYNC and SDI align).					

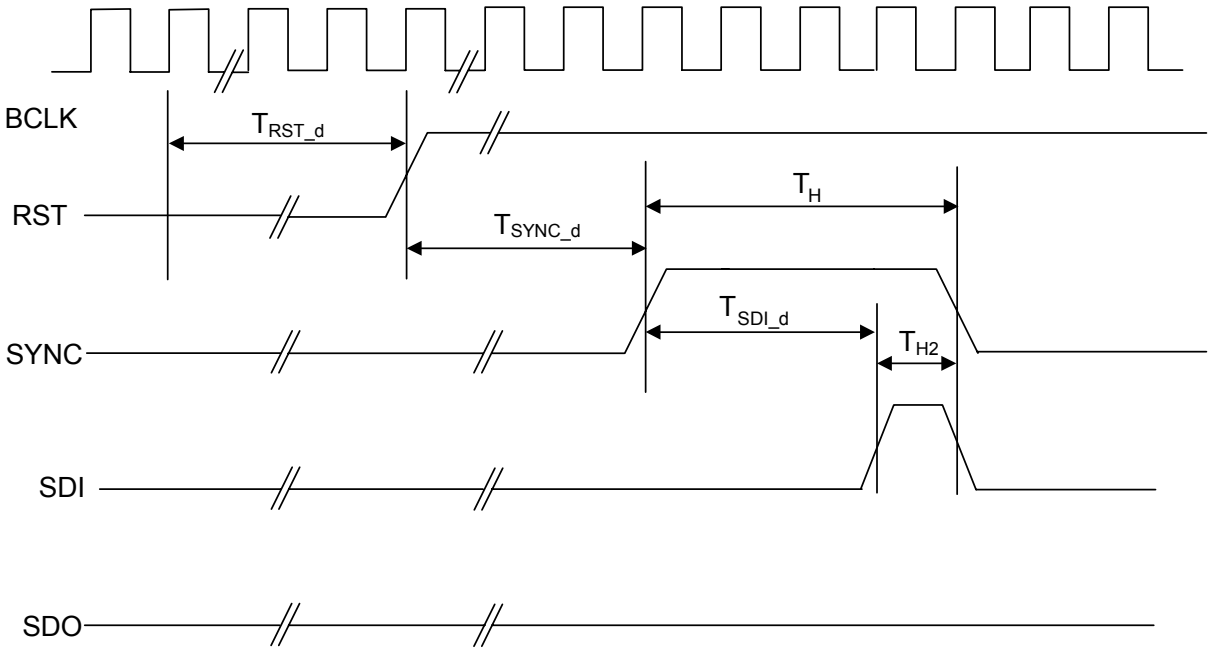


Figure 8. Link Reset Timing Diagram

Table 14. HD Audio Timing Characteristics

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
BCLK Frequency		23.9976	24	24.0012	MHz
Total Period of BCLK including jitter	T_{cyc}	41.163	41.67	42.171	ns
High Phase of BCLK[1]	T_{high}	17.5	—	24.16	ns
Low Phase of BCLK[1]	T_{low}	17.5	—	24.16	ns
BCLK Jitter		—	150	500	ps
SYNC Frequency		—	48.0	—	kHz
SYNC Period	T_{sync_period}	—	20.8	—	µs
SYNC High Pulse Width	T_{sync_high}	—	166.7	—	ns
SYNC Low Pulse Width	T_{sync_low}	—	20.63	—	µs
Time after Rising Edge of BCLK that SDI Becomes Valid	T_{tco}	3	—	11	ns
Setup for SDO[2] at both Rising and Falling Edge of BCLK	T_{su}	5	—	—	ns
Hold for SDO[2] at both Rising and Falling Edge of BCLK	T_h	5	—	—	ns

Notes:
1. 42/58% is the worst case duty cycle at the codec, as measured at v_test in Figure 9.
2. SYNC and RST have the same timing definitions as SDO.

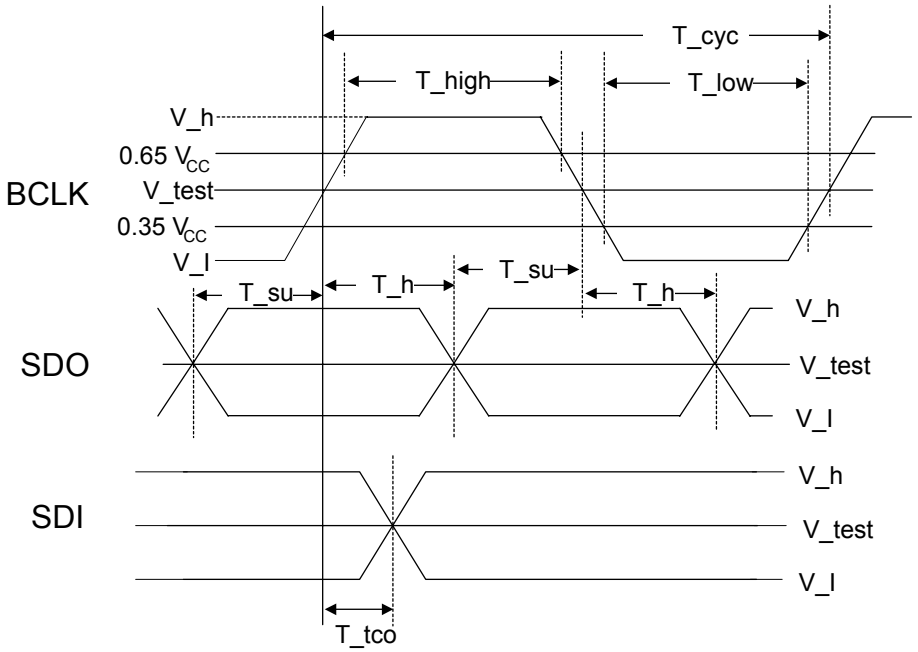


Figure 9. HD Audio Timing Diagram

Table 15. Digital FIR Filter Characteristics—Transmit and Receive

(V_D = 3.0 to 3.6 V, Sample Rate = 8 kHz, T_A = 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Passband (0.1 dB)	$F_{(0.1\ dB)}$	0	—	3.3	kHz
Passband (3 dB)	$F_{(3\ dB)}$	0	—	3.6	kHz
Passband Ripple Peak-to-Peak		–0.1	—	0.1	dB
Stopband		—	4.4	—	kHz
Stopband Attenuation		–74	—	—	dB
Group Delay	t_{gd}	—	12/Fs	—	sec
Note: Typical FIR filter characteristics for Fs = 8000 Hz are shown in Figures 10, 11, 12, and 13.					

Table 16. Digital IIR Filter Characteristics—Transmit and Receive

(VD = 3.0 to 3.6 V, Sample Rate = 8 kHz, T_A = 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Passband (3 dB)	$F_{(3\ dB)}$	0	—	3.6	kHz
Passband Ripple Peak-to-Peak		–0.2	—	0.2	dB
Stopband		—	4.4	—	kHz
Stopband Attenuation		–40	—	—	dB
Group Delay	t_{gd}	—	1.6/Fs	—	sec
Note: Typical IIR filter characteristics for Fs = 8000 Hz are shown in Figures 14, 15, and 16. Figures 18 and 19 show group delay versus input frequency.					

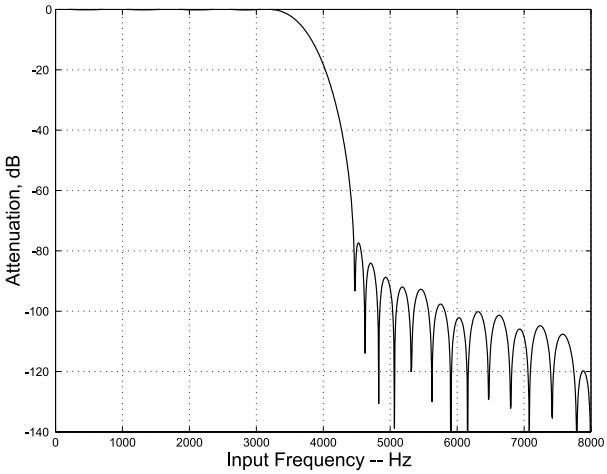


Figure 10. FIR Receive Filter Response

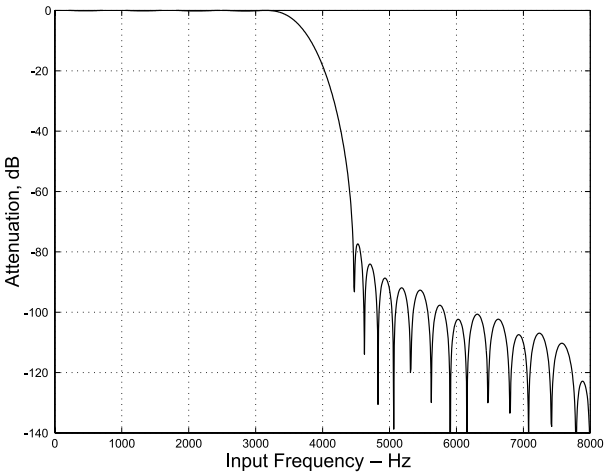


Figure 12. FIR Transmit Filter Response

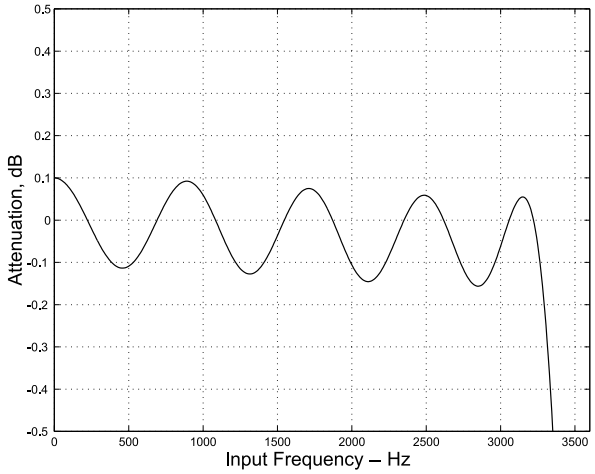


Figure 11. FIR Receive Filter Passband Ripple

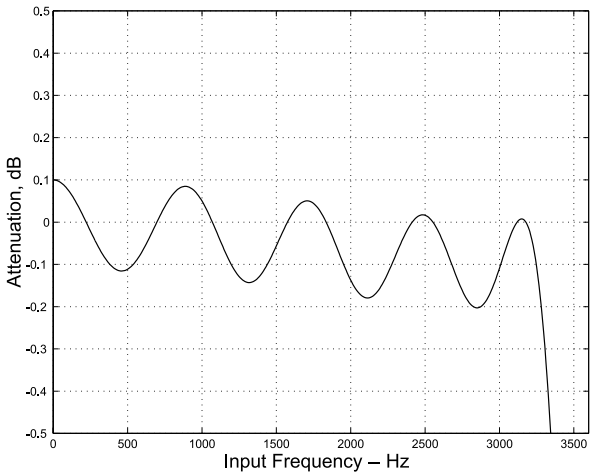


Figure 13. FIR Transmit Filter Passband Ripple

For Figures 10–13, all filter plots apply to a sample rate of Fs = 8 kHz.

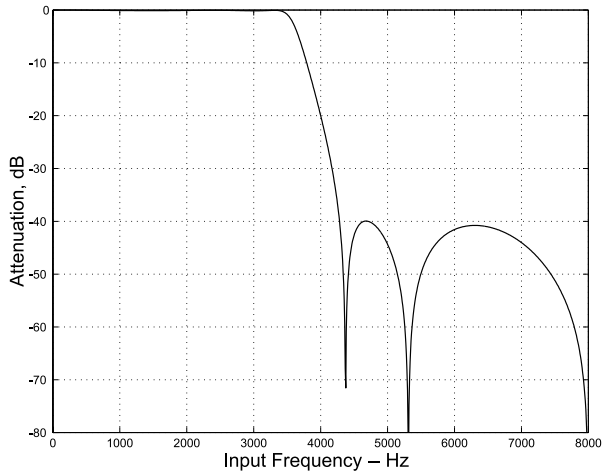


Figure 14. IIR Receive Filter Response

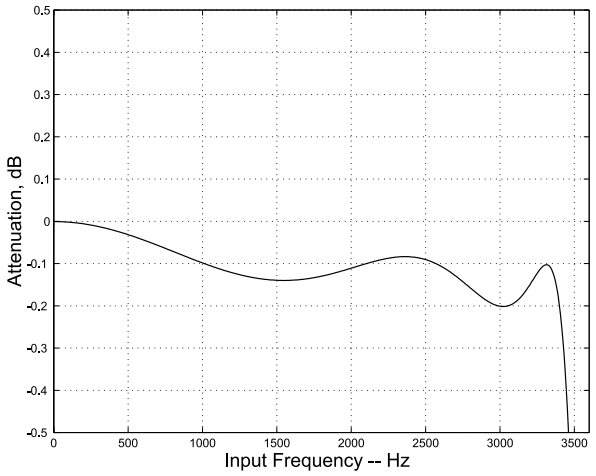


Figure 17. IIR Transmit Filter Passband Ripple

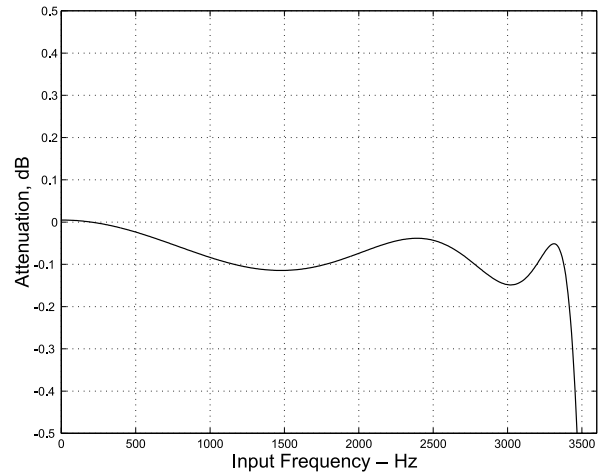


Figure 15. IIR Receive Filter Passband Ripple

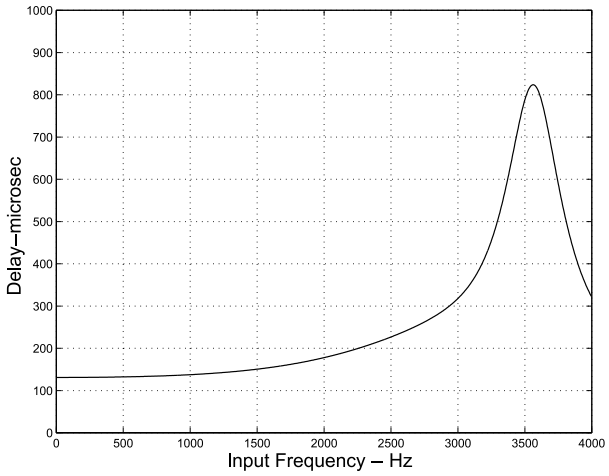


Figure 18. IIR Receive Group Delay

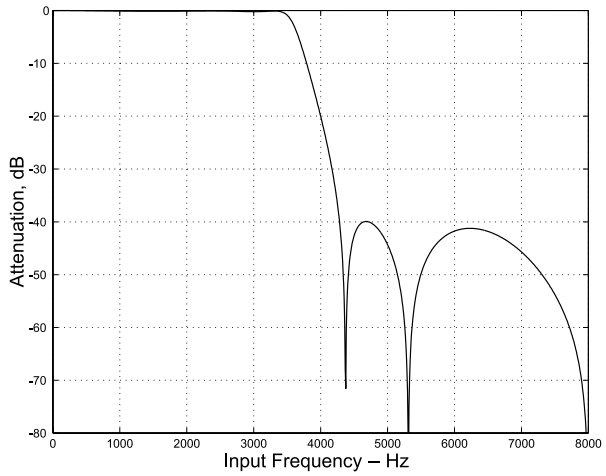


Figure 16. IIR Transmit Filter Response

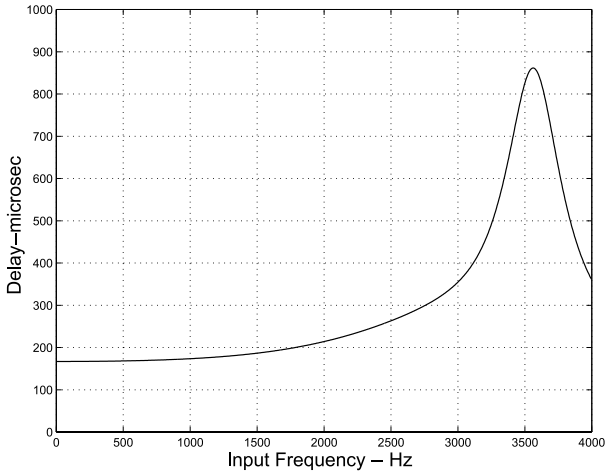
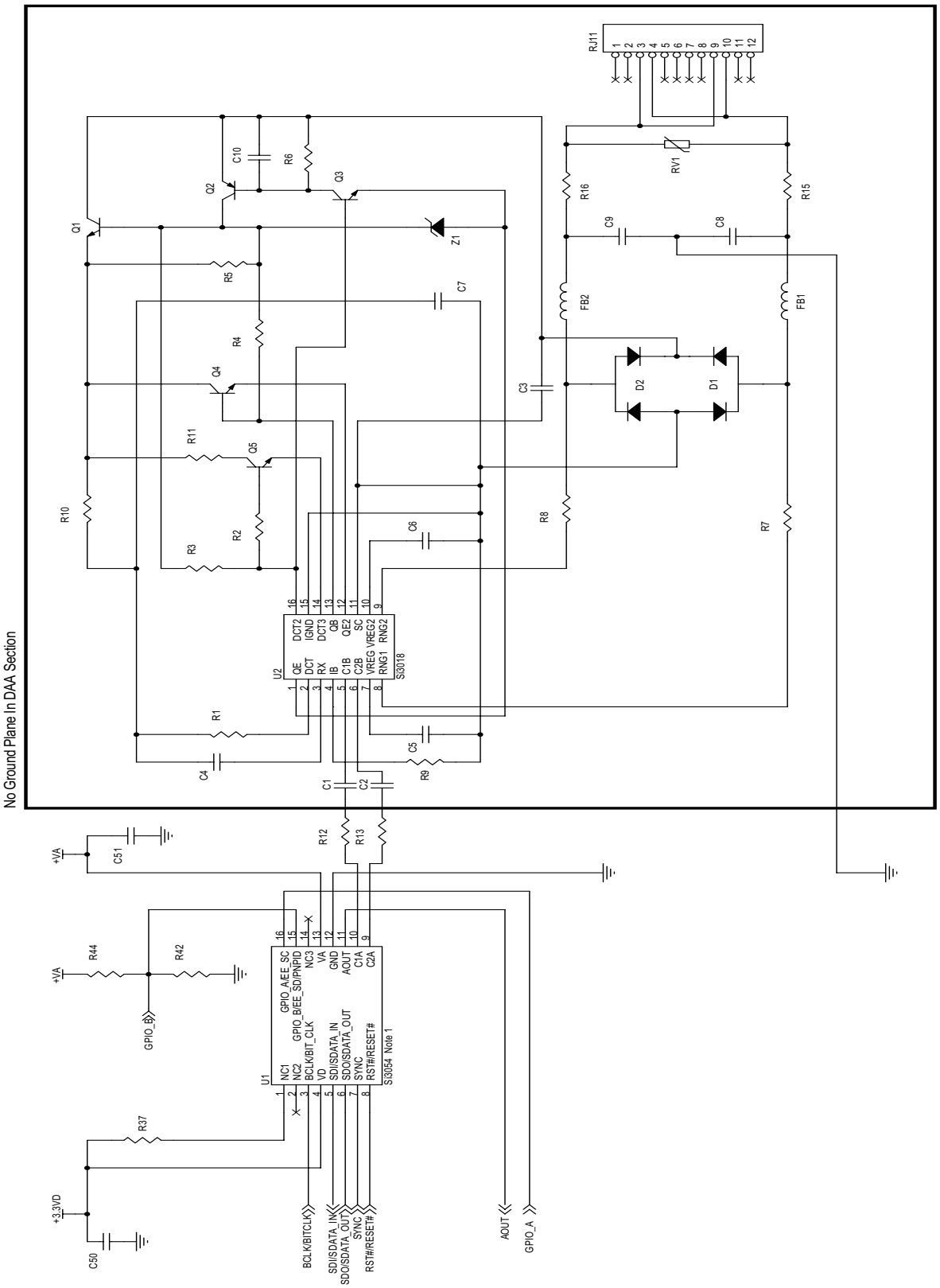


Figure 19. IIR Transmit Group Delay

2. Typical Application Schematic



3. Bill of Materials

Symbol	Value	Supplier(s)
C1, C2[1]	33 pF, Y2, X7R, ±20%	Murata, Johanson, Panasonic
C3	10 nF, 250 V, X7R, ±20%	Venkel, SMEC, Panasonic
C4[2]	1.0 µF, 50 V, X7R, ±20%	Venkel, SMEC, Panasonic
C5, C6	0.1 µF, 16 V, X7R, ±20%	Venkel, SMEC, Panasonic
C7	2.7 nF, 50 V, X7R, ±20%	Venkel, SMEC, Panasonic
C8, C9[1]	680 pF, Y2, X7R, ±10%	Murata, Johanson, Panasonic
C10	0.01 µF, 16 V, X7R, ±20%	Venkel, SMEC, Panasonic
C50, C51	0.1 µF, 16 V, X7R, ±20%	Venkel, SMEC, Panasonic
D1, D2[3]	Dual Diode, 225 mA, 300 V	Central Semiconductor
FB1, FB2, R15, R16	Ferrite Bead (BLM18AG601SN1B)	Murata
Q1, Q3	NPN, 300 V (MMBTA42)	On Semi, Fairchild
Q2	PNP, 300 V (MMBTA92)	On Semi, Fairchild
Q4, Q5	NPN, 80 V, 330 mW, MMBTA06	On Semi, Fairchild
RV1	Sidactor, 275 V, 100 A	Teccor, Diodes Inc., Shindengen
R1	1.07 kΩ, 1/2 W, ±1%	Venkel, SMEC, Panasonic
R2	150 Ω, 1/16 W, ±5%	Venkel, SMEC, Panasonic
R3	3.65 kΩ, 1/2 W, ±1%	Venkel, SMEC, Panasonic
R4	2.49 kΩ, 1/2 W, ±1%	Venkel, SMEC, Panasonic
R5, R6	100 kΩ, 1/16 W, ±5%	Venkel, SMEC, Panasonic
R7, R8	20 MΩ, 1/16 W, ±5%	Venkel, SMEC, Panasonic
R9	1 MΩ, 1/16 W, ±1%	Venkel, SMEC, Panasonic
R10	536 Ω, 1/4 W, ±1%	Venkel, SMEC, Panasonic
R11	73.2 Ω, 1/2 W, ±1%	Venkel, SMEC, Panasonic
R12, R13	56.2 Ω, 1/16 W, 1%	Venkel, SMEC, Panasonic
R37	Not Installed	Venkel, SMEC, Panasonic
R42	4.99 kΩ, 1/16 W, ± 1%	Venkel, SMEC, Panasonic
R43, R44	Not Installed	Venkel, SMEC, Panasonic
U1	Si3054	Silicon Labs
U2	Si3018	Silicon Labs
Z1	Zener Diode, 43 V, 1/2 W	Diodes, Inc.

Notes:

1. X2/Y3 or Y2 rated capacitors can be used to comply with Nordic supplemental insulation requirements. Additional vendors of X2/Y3 or Y2 rated capacitors include Novacap, Syfer, and Kyocera.
2. On small form-factor designs, a value of 0.47 µF, 50 V, X7R, ±20% may be used for C4.
3. Several diode bridge configurations are acceptable. Parts such as a single DF-04S or four 1N4004 diodes may be used (suppliers include General Semiconductor, Diodes Inc., etc.)

4. Resistor ID Configuration

The AC'97 Revision 2.3 and HD Audio specification require all codecs to implement specific vendor identification. In AC'97 mode, this information can be obtained by reading registers 62h and 64h. In HD Audio mode, the subsystem ID verb, "get parameter/vendor ID", parameter control returns the device and vendor ID values used to identify the codec to the PnP subsystem. Vendor ID and device ID are each 16-bit values. Silicon Laboratories defines customer-specific vendor ID values hardwired in the Si3054. The device ID is hardwired as "3054" in AC'97 mode and as "3055" in HD Audio mode.

The AC'97 2.3 and HD Audio specifications also provide support for PnP subsystem information.

- PnP Subsystem Vendor ID (SVID)—a unique number assigned to the card manufacturer.
- PnP Subsystem ID (SID)—a unique number defined by the card manufacturer for the hardware and software combination (the product).

The PnP SVID and PnP SID values are typically loaded from a strapping option at powerup. For the Si3054 DAA, a single-pin resistor strapping option programs 11 predefined 4-byte values into the PnP SVID and PnP SID registers. Resistors R44 and R42 are strapped to the Si3054 ID PIN between VA and GND for ID1 to ID9. For ID0 and ID10, a single resistor is used to strap to GND and VA respectively. This is diagrammed in Figure 20.

The voltage created by the resistive R44/R42 divider generates an ID number between 0 and 10. This ID number is translated into a predefined 16-bit PnP SID value that is loaded into the corresponding DAA registers. If the resistor ID feature is not used, the PnP ID pin should be pulled to Gnd through a 4.99 kΩ or 4.7 kΩ resistor. A no-connect on the ID PIN is an invalid configuration.

Note: For ID10, strap R44 to V_A or 3.3 V. Do not strap to 5 V.

Additionally, resistors R44 and R42 have the following requirements:

- R42 < 5 kΩ
- V_{DD} max/(R44+R42) < 1 mA
- Standard 1% tolerance values

See Table 17 for resistor value to ID value translation data.

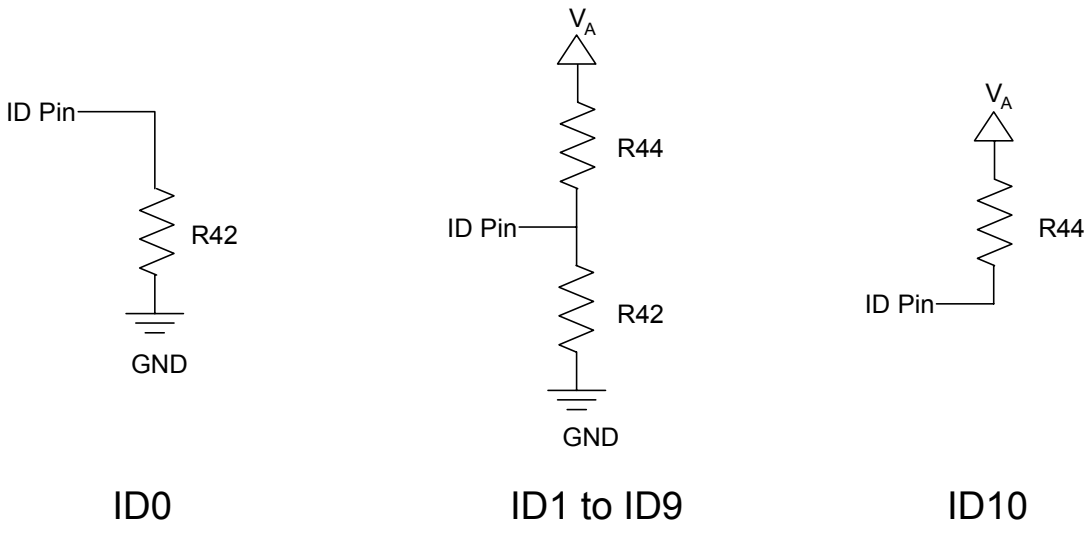


Figure 20. Resistor ID Pin Strapping Diagram

Table 17. Resistor Value to ID Number Translation Table

R44 Value (Ω)	R42 Value (Ω)	ID Number	PnP SVID	PnP SID
—	4990	0	Bond option customer-specific values defined in Si3054 ROM table.	
3570	590	1		
3320	1020	2		
4750	2320	3		
2740	2000	4		
1870	2000	5		
1870	2940	6		
1740	4120	7		
887	3480	8		
523	4220	9		
4990	—	10		

5. AOUT PWM Output

Figure 21 illustrates an optional circuit to support the pulse width modulation (PWM) output capability of the Si3054 for call progress monitoring purposes. This mode is enabled by setting the PWME bit (Register 6Ah or NID 19).

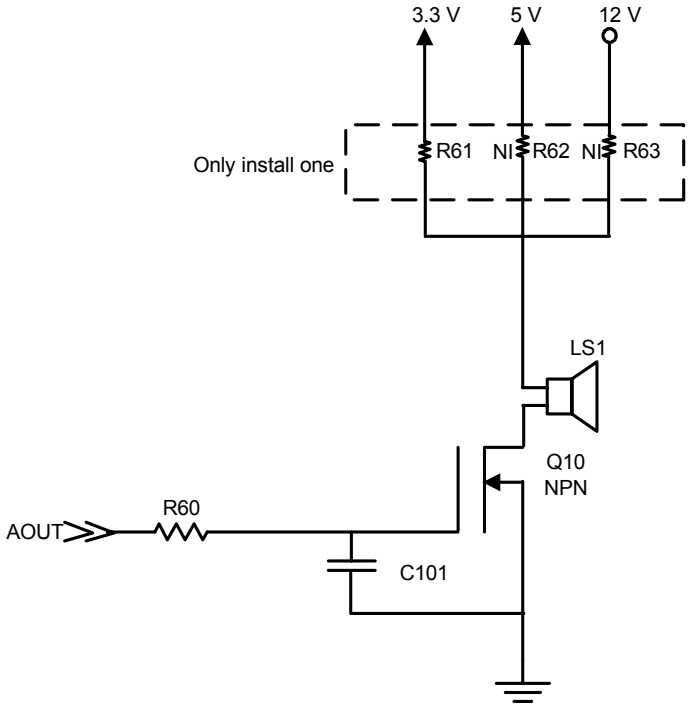


Figure 21. AOUT PWM Circuit for Call Progress

Table 18. Component Values—AOUT PWM

Component	Value	Supplier
LS1	Speaker BRT1209PF-06	Intervox
Q10	NPN KSP13	Fairchild
C101	0.1 µF, 16 V, X7R, ±20%	Venkel, SMEC
R60	150 Ω, 1/10 W, ±5%	Venkel, SMEC, Panasonic
R61	0 Ω, 1/10 W, ±5%	Venkel, SMEC, Panasonic

The signal is a standard digital output from AOUT, which represents the sum of independently scalable receive and transmit call progress contents in pulse-width modulation (PWM) form. The sampling rate of the audio path signals is 32 kHz. The format of the PWM is configurable by the PWMM bits. In AC ’97 mode, register 5Ch controls receive and transmit gains in 6 dB steps, and also controls muting. For both HD Audio and AC ‘97 modes, NID17 or Register 68h can be used to control AOUT muting and fine resolution receive and transmit gain control. These registers allow the receive and transmit paths to be independently controlled and gained/attenuated linearly. Setting these 8-bit registers to all 0s mutes the receive and transmit paths. These registers affect the call progress output only and do not affect transmit and receive operations on the telephone line.

6. Functional Description

The Si3054 and Si3018 comprise an integrated direct access arrangement (DAA) that provides a low-cost, isolated, silicon-based interface to the telephone line. The Si3054 complies with either the AC'97 2.3 or HD Audio 1.0 specifications and requires only a few low-cost discrete components to achieve global PTT compliance. The device implements Silicon Laboratories' patented capacitive communications link technology, which offers the highest level of integration by replacing an analog front end (AFE), an isolation transformer, relays, opto-isolators, and a 2- to 4-wire hybrid with two 16-pin small outline packages (SOIC).

The Si3018 can be fully programmed to meet international requirements and is compliant with FCC, TBR21, JATE, and various other country-specific PTT specifications as shown in Table 19. In addition, the Si3018 has been designed to meet the most stringent worldwide requirements for out-of-band energy, emissions, immunity, lightning surges, and safety.

Table 19. Country Specific Register Settings

Register	HD Audio or AC'97 Mode								AC'97 MAP = 0 Only	
	NID16 or Page 2: 64h					NID15 or Page 2: 62h			5Ch	62h
Country	OHS	RZ	RT	ACT	OHS2	DCV[1:0]	MINI[1:0]	ILIM	DCT[1:0]	VOL[1:0]
Argentina	0	0	0	0	0	11	00	0	10	00
Australia[3]	1	0	0	1	0	01	01	0	01	00
Austria	0	0	0	0 or 1	1	11	00	1	11	00
Bahrain	0	0	0	0	1	11	00	1	10	00
Belgium	0	0	0	0 or 1	1	11	00	1	11	00
Brazil	0	0	0	0	0	11	00	0	10	00
Bulgaria	0	0	0	0 or 1	1	11	00	1	11	00
Canada	0	0	0	0	0	11	00	0	10	00
Chile	0	0	0	0	0	11	00	0	10	00
China	0	0	0	1	0	11	00	0	01 or 10	00
Colombia	0	0	0	0	0	11	00	0	10	00
Croatia	0	0	0	0 or 1	1	11	00	1	11	00
Cyprus	0	0	0	0 or 1	1	11	00	1	11	00
Czech Republic	0	0	0	0 or 1	1	11	00	1	11	00
Denmark	0	0	0	0 or 1	1	11	00	1	11	00
Ecuador	0	0	0	0	0	11	00	0	10	00
Egypt	0	1	0	0 or 1	0	11	00	1	01	00
El Salvador	0	0	0	0	0	11	00	0	10	00
Finland	0	0	0	0 or 1	1	11	00	1	11	00
France	0	0	0	0 or 1	1	11	00	1	11	00

Notes:

1. TBR21 includes the following countries: Austria, Belgium, Denmark, Finland, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Luxembourg, Netherlands, Norway, Poland, Portugal, Romania, Slovenia, Slovakia, Spain, Sweden, Switzerland, and the United Kingdom.
2. Supported for loop current ≥ 20 mA.
3. See "6.9.DC Termination," on page 27 for more information.

Table 19. Country Specific Register Settings (Continued)

Register	HD Audio or AC'97 Mode								AC'97 MAP = 0 Only	
	NID16 or Page 2: 64h					NID15 or Page 2: 62h			5Ch	62h
Country	OHS	RZ	RT	ACT	OHS2	DCV[1:0]	MINI[1:0]	ILIM	DCT[1:0]	VOL[1:0]
Germany	0	0	0	0 or 1	1	11	00	1	11	00
Greece	0	0	0	0 or 1	1	11	00	1	11	00
Guam	0	0	0	0	0	11	00	0	10	00
Hong Kong	0	0	0	0	0	11	00	0	10	00
Hungary	0	0	0	0 or 1	1	11	00	1	11	00
Iceland	0	0	0	0 or 1	1	11	00	1	11	00
India	0	0	0	0	0	11	00	0	10	00
Indonesia	0	0	0	0	0	11	00	0	10	00
Ireland	0	0	0	0 or 1	1	11	00	1	11	00
Israel	0	0	0	0 or 1	1	11	00	1	11	00
Italy	0	0	0	0 or 1	1	11	00	1	11	00
Japan	0	0	0	0	0	01	01	0	01	00
Jordan	0	0	0	0	0	01	01	0	01	00
Kazakhstan	0	0	0	0	0	11	00	0	10	00
Kuwait	0	0	0	0	0	11	00	0	10	00
Latvia	0	0	0	0 or 1	1	11	00	1	11	00
Lebanon	0	0	0	0 or 1	1	11	00	1	11	00
Luxembourg	0	0	0	0 or 1	1	11	00	1	11	00
Macao	0	0	0	0	0	11	00	0	10	00
Malaysia[2]	0	0	0	0	0	01	01	0	01	00
Malta	0	0	0	0 or 1	1	11	00	1	11	00
Mexico	0	0	0	0	0	11	00	0	10	00
Morocco	0	0	0	0 or 1	1	11	00	1	11	00
Netherlands	0	0	0	0 or 1	1	11	00	1	11	00
New Zealand	0	0	0	1	0	11	00	0	10	00
Nigeria	0	0	0	0 or 1	1	11	00	1	11	00
Norway	0	0	0	0 or 1	1	11	00	1	11	00
Oman	0	0	0	0	0	01	01	0	01	00
Pakistan	0	0	0	0	0	01	01	0	01	00

Notes:

1. TBR21 includes the following countries: Austria, Belgium, Denmark, Finland, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Luxembourg, Netherlands, Norway, Poland, Portugal, Romania, Slovenia, Slovakia, Spain, Sweden, Switzerland, and the United Kingdom.
2. Supported for loop current ≥ 20 mA.
3. See "6.9.DC Termination," on page 27 for more information.

Table 19. Country Specific Register Settings (Continued)

Register	HD Audio or AC'97 Mode								AC'97 MAP = 0 Only	
	NID16 or Page 2: 64h					NID15 or Page 2: 62h			5Ch	62h
Country	OHS	RZ	RT	ACT	OHS2	DCV[1:0]	MINI[1:0]	ILIM	DCT[1:0]	VOL[1:0]
Peru	0	0	0	0	0	11	00	0	10	00
Philippines	0	0	0	0	0	01	01	0	01	00
Poland	0	0	0	0 or 1	1	11	00	1	11	00
Portugal	0	0	0	0 or 1	1	11	00	1	11	00
Romania	0	0	0	0 or 1	1	11	00	1	11	00
Russia	0	0	0	0	0	11	00	0	10	00
Saudi Arabia	0	0	0	0	0	11	00	0	10	00
Singapore	0	0	0	0	0	11	00	0	10	00
Slovakia	0	0	0	0 or 1	1	11	00	1	11	00
Slovenia	0	0	0	0 or 1	1	11	00	1	11	00
South Africa	0	1	0	0	0	11	00	0	10	00
South Korea	0	1	0	0	0	11	00	0	10	00
Spain	0	0	0	0 or 1	1	11	00	1	11	00
Sweden	0	0	0	0 or 1	1	11	00	1	11	00
Switzerland	0	0	0	0 or 1	1	11	00	1	11	00
Taiwan	0	0	0	0	0	11	00	0	01	00
TBR21[1]	0	0	0	0 or 1	0	11	00	1	11	00
Thailand	0	0	0	0	0	01	01	0	10	00
UAE	0	0	0	0	0	11	00	0	10	00
United Kingdom	0	0	0	0 or 1	1	11	00	1	11	00
USA	0	0	0	0	0	11	00	0	10	00
Yemen	0	0	0	0	0	11	00	0	10	00

Notes:

1. TBR21 includes the following countries: Austria, Belgium, Denmark, Finland, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Luxembourg, Netherlands, Norway, Poland, Portugal, Romania, Slovenia, Slovakia, Spain, Sweden, Switzerland, and the United Kingdom.
2. Supported for loop current ≥ 20 mA.
3. See "6.9.DC Termination," on page 27 for more information.

6.1. Upgrading from Si3054 Revision D to Revision E or Later

The Si3054 Revision E or later offers customers currently shipping Si3054 Revision D modems, or customers designing new modems, a DAA solution for modems intended to ship with either AC‘97 or HD Audio motherboards. Due to the inclusion of both the AC‘97 and HD Audio digital interface blocks along with patented autodetection circuitry, the Si3054 Revision E or later system-side allows one modem design to support both AC‘97 and HD Audio applications. This flexible architecture allows a single modem SKU to ship with any PC motherboard without any hardware changes. This architecture further reduces cost by eliminating the need to homologate multiple modem cards. The Si3054 Revision E or later is well-suited to MDC1.0, MDC1.5, CNR, or other custom small form factor PCBs.

The Si3054 Revision E or later is pin compatible with the Si3054 Revision D. An Si3054 Revision D could be replaced with an Si3054 Revision E or later device without any hardware changes to an existing Si3054 Revision D based modem board. Furthermore, no changes to the AC‘97 modem driver are required to transition from Si3054 Revision D to Revision E or later for use in AC‘97 mode.

6.2. Initialization

When the Si3054 is initially powered up, the $\overline{\text{RST}}$/$\overline{\text{RESET}}$ pin should be asserted. After initial power up or when the software issues a register reset, all Si3054 registers take on their default values. This reset condition guarantees the line-side chip is powered down with no possibility of loading the line (i.e., off-hook).

6.2.1. Initialization Procedure for AC-Link

AC-Link reset is initiated by the AC’97 controller. An example AC’97 initialization procedure is outlined below:

1. Execute a register reset by writing (any value) to Register 3Ch.
2. Program the desired sample rate with Register 40h (42h). See Register 40h (42h) description on page 59 for allowable sample rates.
3. Write 0x0000 to Register 3Eh to power up the Si3054.
4. Wait for the Si3054 to complete power up. The lower 8 bits indicate that the Si3054 is ready. If the Si3054 is configured as line #1 codec, 3Eh[7:0] = 0x0F indicates readiness. If the codec is configured as line #2, 3Eh[7:0] = 0x33 indicates readiness.
5. Program GPIO registers to desired modes (registers 4Ch–54h).
6. Program DAC/ADC levels with Register 46h (48h).
7. Program desired line interface parameters (i.e., DCT[1:0], ACT, OHS, RT, RZ, and VOL[1:0] as defined in Table 19, “Country Specific Register Settings,” on page 22.)
8. Wait until the FDT bit in Register 5Eh is set, indicating that the line-side device PLL is locked.

After this procedure is complete, the Si3054 chipset is ready for ring detection and off-hook operation.

6.2.2. Initialization Procedure for HD Audio

Two types of reset can occur within an HD Audio system: link reset and codec reset. Link reset is initiated by the HD Audio controller through assertion of the $\overline{\text{RST}}$ signal and affects all HD Audio link interface logic in both the controller and codecs on the link. Codec reset is a command generated by the bus driver or the modem function driver to the Si3054 and thus only affects the targeted codec and nothing else on the HD Audio link. A single initialization sequence always follows either reset sequence. An example initialization procedure is outlined below:

1. Issue the Function_Reset command verb.
2. Issue the Set_Converter_Format command verb to set the link sample rate and the sample format (16 or 24 bits).
3. Program the desired sample rate in NID 3.
4. Program the stream tags and DAC/ADC levels in NID4.
5. Write 0x0000 to NID 2 to power up the Si3054.
6. Wait for the Si3054 to complete power up. The lower eight bits of NID 2 indicate when the Si3054 is ready. NID 2[7:0] = 0x0F indicates readiness.
7. Program GPIO registers to desired modes (NIDs 5–9).
8. Program desired line interface parameters.
9. Wait until the FDT bit in NID 14 is set, indicating that the line-side device PLL is locked.

After this procedure is complete, the Si3054 chipset is ready for ring detection and off-hook operation.

6.3. Link Detection

The Si3054 uses patented link detection circuitry to determine whether the communication between the Si3054 and the audio/modem bus controller is through an AC'97 or HD Audio digital serial interface. If the Si3054 detects the presence of AC'97 signaling, the DAA is configured as a secondary AC'97 codec. If the Si3054 detects the presence of HD Audio signaling, the DAA is configured as an HD Audio codec.

6.4. AC-Link

AC-link is a bidirectional, fixed rate, serial PCM digital stream. It handles multiple input and output audio streams and control register accesses employing a time-division multiplexing (TDM) scheme. The ac-link architecture divides each audio frame into 12 outgoing and 12 incoming data streams, each with 20-bit sample resolution.

6.5. HD Audio

HD Audio is a bidirectional, fixed rate, serial PCM digital stream. HD Audio improves the AC'97 architecture by providing a HW abstraction layer to minimize modem driver dependencies on the link controller. In the HD Audio architecture, the modem driver communicates Si3054 status and control with verbs to the HD Audio bus driver, which in turn communicates directly to the HD Audio controller.

In contrast to the slot-based AC-Link architecture, HD Audio supports more independent and flexible data streams. The new architecture supports improved stream rates, widths, formats, and bandwidth. For modem AFE, a number of required sample rates are natively supported in HD Audio. The Si3054 supports additional non-natively supported modem sample rates through a patented 24-bit control and data transfer mode (see "8.HD Audio Digital Interface," on page 44).

6.6. Isolation Barrier

The Si3054 chipset achieves an isolation barrier through low-cost, high-voltage capacitors in conjunction with Silicon Laboratories' patented signal processing techniques. These techniques eliminate any signal degradation due to capacitor mismatches, common mode interference, or noise coupling. As shown in "2.Typical Application Schematic," on page 17, the C1, C2, C8, and C9 capacitors isolate the Si3054 (system side) from the Si3018 (line side). All transmit, receive, control, ring detect, and caller ID data are communicated through this barrier. Y2 class capacitors may be used for the isolation barrier to achieve surge performance of 5 kV or greater.

The capacitive communications link is disabled by default. To enable it, the PR bits (in Register 3Eh or NID 2) must be cleared, and the sample rate must be set (in Register 40h or NID 3). No communication between the Si3054 and Si3018 can occur until these conditions are set.

6.7. Off-Hook

The off-hook state is used to seize the line for an incoming/outgoing call and can also be used for pulse dialing. When in the on-hook state, negligible dc current flows through the hookswitch. In the off-hook state, the hookswitch transistor pair, Q1 and Q2, turn on. The net effect of the off-hook signal is the application of a termination impedance across TIP and RING and the flow of dc loop current. The termination impedance has both an ac and dc component.

Several events occur internally to the DAA when the OH bit is set. There is a 250 µs latency for the off-hook command to communicate to the line-side device.

When the line-side device goes off-hook, an off-hook counter forces a delay before transmission or reception occurs for line transients to settle. This off-hook counter time is controlled by the FOH[1:0] bits. The default setting for the off-hook counter time is 128 ms, but can be adjusted up to 512 ms or down to either 64 or 8 ms. After the off-hook counter expires, a resistor calibration is performed for 17 ms. This allows the DAA to adjust internally to the exact conditions present at the time of going off-hook. Disable the resistor calibration by setting the RCALD bit. After the resistor calibration is performed, an ADC calibration is performed for 256 ms. This calibration helps to remove offset in the A/D sampling of the telephone line. Disable the ADC calibration by setting the CALD bit. See “6.8.Calibration” on page 26. for more information on automatic and manual calibration.

Silicon Laboratories® recommends that the resistor and ADC calibrations not be disabled except when a fast response is needed after going off-hook, such as when responding to a Type II caller-ID signal. See “6.20.Caller ID” on page 33.

To calculate the total time required to go off-hook and start transmission or reception, the digital filter delay (typically 1.5 ms with the FIR filter) should be included in the calculation.

When configured as an AC‘97 codec, the communication system generates an off-hook command by writing a logic 1 to bit 0 of slot 12.

When configured as an HD Audio codec, one of two methods will generate an off-hook command depending on whether the codec is configured to use 16-bit or 24-bit data mode. In 16-bit mode, the software generates an off-hook command by writing a logic 1 to bit 0 of NID 10. In 24-bit mode, go off-hook by setting bit 16 of the 24-bit SDO sample.

6.8. Calibration

The Si3054 initiates two auto-calibrations by default when the device goes off-hook or experiences a loss of line power. A 17 ms resistor calibration is performed to allow circuitry internal to the DAA to adjust to the exact line conditions present at that time. This resistor

calibration can be disabled by setting the RCALD bit (Register 25, bit 5).

A 256 ms ADC calibration is also performed to remove offsets that might be present in the on-chip A/D converter which could affect the A/D dynamic range. The ADC auto-calibration is initiated after the DAA dc termination stabilizes and the resistor calibration completes**.** Because large variations in line conditions and line card behavior exist, it could be beneficial to use manual calibration instead of auto-calibration.

Execute manual ADC calibration as close as possible to 256 ms before valid transmit/receive data is expected.

Take the following steps to implement manual ADC calibration:

1. The CALD (auto-calibration disable—Register 17) bit must be set to 1.
2. The MCAL (manual calibration) bit must be toggled to 1 and then 0 to begin and complete the calibration.
3. The calibration is completed in 256 ms.

6.9. DC Termination

The Si3054 has programmable dc termination modes. The dc termination selection defines the I/V characteristics of the Si3054 and has a direct relationship to the transmit level supported by the DAA.

FCC mode, shown in Figure 22, is the default dc termination mode. This mode meets FCC requirements and the requirements of many other countries.

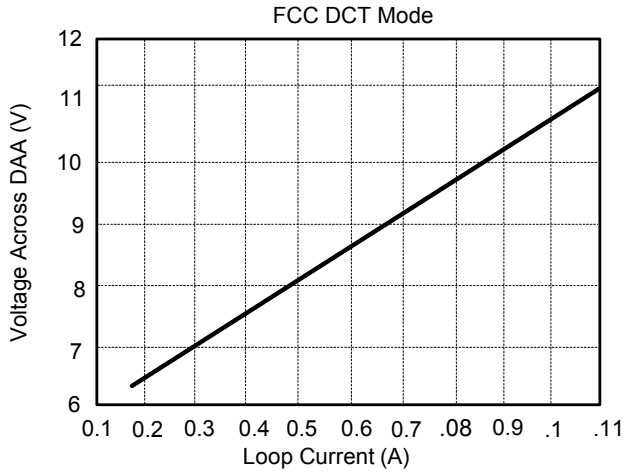


Figure 22. FCC Mode I/V Characteristics

TBR21 mode, shown in Figure 23, provides current limiting before reaching 60 mA.

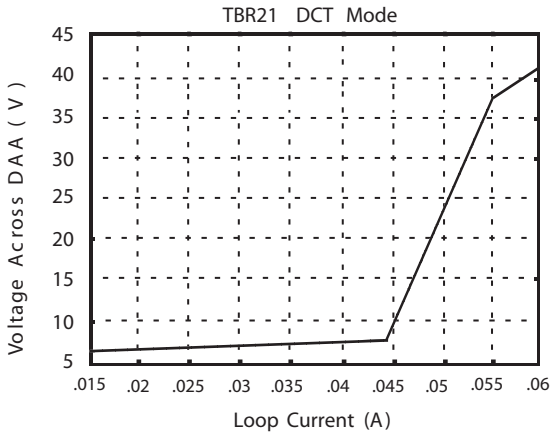


Figure 23. TBR21 Mode I/V Characteristics

Japan mode, shown in Figure 24, is a lower voltage mode and supports a transmit full scale level of –2.71 dBm. Higher transmit levels for DTMF dialing also are supported. The low voltage requirement is dictated by countries, such as Japan and Malaysia.

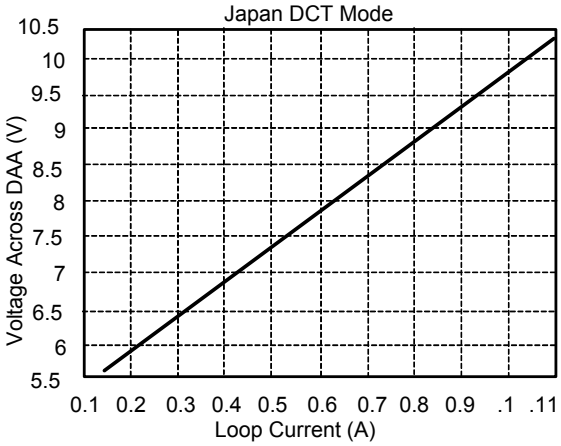


Figure 24. Japan Mode I/V Characteristics

A low-voltage mode is also supported by the Si3054. Higher transmit levels for DTMF dialing also are supported. This low-voltage mode is offered for situations that require low line voltage operation. Use this mode when necessary, as the dynamic range is significantly reduced and thus the Si3054 cannot transmit or receive large signals without clipping them.

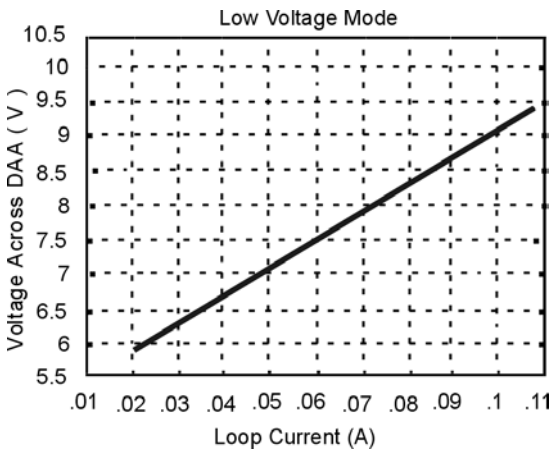


Figure 25. Low Voltage Mode I/V Characteristics

In AC'97 mode (when MAP = 0), dc termination is set with the DCT[1:0] bits in register 5Ch. In either HD Audio Mode or AC'97 mode (when MAP = 1), DCV[1:0], MINI[1:0], and ILIM are used to set the dc termination.

The MINI[1:0] bits select the minimum operational loop current for the DAA, and the DCV[1:0] bits adjust the DCT pin voltage, which affects the TIP/RING voltage of the DAA. These bits permit important trade-offs for the system designer. Increasing the TIP/RING voltage provides more signal headroom, while decreasing the TIP/RING voltage allows compliance to PTT standards in low-voltage countries such as Japan. Increasing the minimum operational loop current above 10 mA also increases signal headroom and prevents degradation of the signal level in low-voltage countries. The dc impedance of the DAA is normally represented with a 50 Ω slope, as shown in Figure 22, but can be changed to an 800 Ω slope by setting the DCR bit.

Under certain line conditions, it may be beneficial to use other dc termination modes not intended for a particular world region.

For very low voltage countries, such as Japan and Malaysia, the following procedure may be used to optimize distortion characteristics and maximize transmit levels:

1. When first going off-hook, use the Japan mode.
2. Measure the loop current using the LCS[4:0] bits.
3. If LCS[3:0] ≤ 6, maintain the current settings and proceed with normal operation.
4. If LCS[3:0] ≥ 10, switch to FCC mode.

Note: A single decision of dc termination mode following off-hook is appropriate for most applications. However, during PTT testing, a false dc termination I/V curve may be generated if the dc I/V curve is determined following a single off-hook event.

Finally, Australia has separate dc termination requirements for line seizure versus line hold. Japan mode may be used to satisfy both requirements. However, if a higher transmit level for modem operation is desired, switch to FCC mode 500 ms after the initial off-hook. This satisfies the Australian dc termination requirements.

6.10. AC Termination

The Si3054 has four ac termination impedance settings. The ACT and ACT2 bits select the ac impedance. The available ac termination settings are listed in Table 20.

Table 20. AC Termination Settings

ACT2	ACT	AC Termination
0	0	Real, nominal 600 Ω termination that satisfies the impedance requirements of FCC part 68, JATE, and other countries.
0	1	Complex impedance that satisfies global impedance requirements.
1	0	Complex impedance that satisfies global impedance requirements EXCEPT New Zealand. Achieves higher return loss for countries requiring complex ac termination. [220 Ω + (820 Ω || 120 nF) and 220 Ω + (820 Ω || 115 nF)]
1	1	Complex impedance for use in New Zealand. [370 Ω + (620 Ω || 310 nF)

6.11. Transhybrid Balance

The Si3054 contains an on-chip analog hybrid that performs the 2- to 4-wire conversion and near-end echo cancellation. This hybrid circuit is adjusted for each ac termination setting selected.

6.12. Ring Detection

The ring signal is capacitively coupled from TIP and RING to the RNG1 and RNG2 pins. The Si3054 supports either full- or half-wave ring detection. With full-wave ring detection, the designer can detect a polarity reversal as well as the ring signal. See "6.20.Caller ID," on page 33. The ring detection threshold is programmable with the RT bit in Register 5Ch or NID13.

The ring detector output can be monitored in one of three ways. The first method uses the GPIO. When configured as an AC'97 codec, the GPIO1 bit of slot 12 can be monitored to detect a ring. When configured as an HD Audio codec, GPI1 and GPI2 can be used to detect a ring in 16-bit and 24-bit modes, respectively. The second method uses the register bits RDTP and

RDTN in Register 5Eh (or NID14). The final method uses the SDI/SDATA_IN output.

The digital bus controller must detect the ring signal frequency in order to distinguish a ring from pulse dialing by telephone equipment connected in parallel.

Alternatively, hardware ring validation can be used. See “6.13.Ring Validation” .

The ring detector mode is controlled by the RFWE bit (Register 5Ch or NID13). When the RFWE is 0 (default mode), the ring detector operates in half-wave rectifier mode. In this mode, only positive ringing signals are detected. A positive ringing signal is defined as a voltage greater than the ring threshold across RNG1-RNG2. Conversely, a negative ringing signal is defined as a voltage less than the negative ring threshold across RNG1-RNG2.

When the RFWE is 1, the ring detector operates in full-wave rectifier mode. In this mode, both positive and negative ring signals are detected.

When RFWE is 0, the GPIO1 bit is set for a period of time. The GPIO1 bit is not set for a negative ringing signal. The GPIO1 bit acts as a one shot. Whenever a new ring signal is detected, the one shot is reset. If no new ring signals are detected prior to the one shot counter counting down to zero, the GPIO1 bit returns to zero. The length of this count (in seconds) is 65536 divided by the sample rate. The GPIO1 bit is also reset to zero by an off-hook event.

When RFWE is 1, the GPIO1 bit toggles active low when the ring signal is positive or negative. This makes the ring signal appear to be twice the frequency of the ringing waveform.

The RDTP and RDTN behavior is based on the RNG1-RNG2 voltage. Whenever the signal, RNG1-RNG2, is above the positive ring threshold, the RDTP bit is set. Whenever the signal, RNG1-RNG2, is below the negative ring threshold, the RDTN bit is set. When the signal, RNG1-RNG2, is between these thresholds, neither bit is set.

If the communications link is active and the device is not off-hook or not in on-hook line monitor mode, the ring data will be presented on SDI/SDATA_IN. The waveform on SDI/SDATA_IN depends on the state of the RFWE bit.

When RFWE is 0, SDI/SDATA_IN is –32768 (8000h) while the RNG1-RNG2 voltage is between the thresholds. When a ring is detected, SDI/SDATA_IN transitions rather quickly to +32767 while the ring signal is positive, then goes back to –32768 while the ring is near zero and negative. Thus, a near square wave is presented on SDI/SDATA_IN that swings from –32768 to +32767 in cadence with the ring signal.

When RFWE is 1, SDI/SDATA_IN sits at approximately +1228 while the RNG1-RNG2 voltage is between the thresholds. When the ring goes positive, SDI/SDATA_IN transitions to +32767. When the ring signal goes near zero, SDI/SDATA_IN remains near 1228. Then, as the ring goes negative, the SDI/SDATA_IN transitions to –32768. This will repeat in cadence with the ring signal.

The best way to observe the ring signal on SDI/SDATA_IN is simply to observe the MSB of the data. The MSB toggles in cadence with the ring signal independent of the ring detector mode. This is adequate information for determining the ring frequency. The MSB of SDI/SDATA_IN toggles at the same frequency as the ring signal.

6.13. Ring Validation

This feature prevents false triggering of a ring detection by validating the ring frequency. Invalid signals, such as a loop current change when a parallel handset goes off-hook, pulse dialing, or a high-voltage line test, are ignored. Ring validation can be used during normal operation and in low-power sleep mode.

The ring validation circuit operates by calculating the time between alternating crossings of positive and negative ring thresholds to validate that the ring frequency is within tolerance. High- and low-frequency tolerances are programmable in the RAS[5:0] and RMX[5:0] fields. The RCC[2:0] bits define how long the ring signal must be within tolerance.

Once the duration of the ring frequency is validated by the RCC bits, the circuitry stops checking for frequency tolerance and begins checking for the end of the ring signal, which is defined by a lack of additional threshold crossings for a period of time configured by the RTO[3:0] bits. When the ring frequency is first validated, a timer defined by the RDLY[2:0] bits is started. If the RDLY[2:0] timer expires before the ring timeout, the ring is validated, and a valid ring is indicated. If the ring timeout expires before the RDLY[2:0] timer, a valid ring is not indicated.

Ring validation requires five parameters:

- Timeout parameter to place a lower limit on the frequency of the ring signal on the RAS[5:0] bits (Register 6Eh). This is measured by calculating the time between crossings of positive and negative ring thresholds.
- Minimum count to place an upper limit on the frequency on the RMX[5:0] bits (Register 6Eh or NID21).
- Time interval over which the ring signal must be the correct frequency on the RCC[2:0] bits (Register

6Ch or NID20).

- Timeout period that defines when the ring pulse has ended with the most recent ring threshold crossing on the RTO [3:0] bits (Register 6Eh or NID21).
- Delay period between when the ring signal is validated and when a valid ring signal is indicated to accommodate distinctive ringing.

The RNGV bit (Register 6Ch or NID20) enables or disables the ring validation feature in normal operating mode and low-power sleep mode.

6.14. Ringer Impedance and Threshold

The ring detector in many DAAs is ac-coupled to the line with a large 1 µF, 250 V decoupling capacitor. The ring detector in the Si3054 chipset is resistively-coupled to the line. The network produces a high ringer impedance to the line of approximately 20 mΩ to meet the majority of country PTT specifications, including FCC and TBR21.

Several countries including Poland, South Africa, and Slovenia, require a maximum ringer impedance that can be met with an internally-synthesized impedance by setting the RZ bit (Register 5Ch or NID13).

Countries also specify ringer thresholds differently. The RT bit (Register 5ch or NID13) selects between two different ringer thresholds: 15 V ±10% and 21.5 V ±10%. These two settings satisfy ringer threshold requirements worldwide. The thresholds are set so that a ring signal is guaranteed to not be detected below the minimum, and a ring signal is guaranteed to be detected above the maximum.

6.15. Wake-on-Ring

Ring is an example of an event that might need to wake up a PC that has suspended into a low-power state. Power management or wake event support for a modem is a key feature of current PC industry standards.

6.15.1. AC‘97 Version 2.3 Wake-on-Ring

The Si3054 chipset provides wake-up on ring through the AC-link as defined by the AC ’97 version 2.3 specification. In an implementation designed for wake-up on ring, where the Si3054 and AC-link are both completely powered by V_{aux}, a ring detected at the RNG1 and RNG2 pins of the Si3054 causes the assertion of the power management signal to the system. The power management signal is the rising edge of the SDATA_IN signal when the Si3054 is in low-power mode. The power management event signal assertion causes the system to resume so that the modem event (ring) can be serviced. The first thing that the device driver must do to reestablish communications with the Si3054 is to command the AC ’97 Digital Controller to execute a warm reset to the AC-link. Figure 26 illustrates the entire sequence.

The rising edge of SDATA_IN causes the AC ’97 Digital Controller to assert its power management signal to the system’s ACPI controller. The Si3054 keeps SDATA_IN high until it has sampled SYNC having gone high, and then low (warm reset). The power management event is cleared out in the AC ’97 Digital Controller by system software asynchronous to AC-link activity. The AC ’97 Digital Controller should always monitor the Si3054’s ready bit before sending data to it. The modem driver should read the GPIO Pin Status register to determine if the wake event was due to the ring signal before executing a register reset.

Before entering low-power mode, the Si3054 must be enabled to cause the wake signal when receiving a ring. This is done by programming the GPIO Pin Sticky (50h) and GPIO Wake Up Mask (52h) registers and clearing previous sticky GPIO events. Before setting the MLNK bit, the driver should do the following:

1. Set the GS1 bit in Register 50h
2. Set the GW1 bit in Register 52h
3. Clear a possible old sticky event by writing a 0 to the GI1 (GI11 for line #2) bit in read-only register GPIO Pin Status register (54h).

If the AC ’97 Digital Controller allows the $\overline{\text{RESET}}$ signal to go low during the low-power mode of the Si3054, the wake event will be a cold reset (rising edge of $\overline{\text{RESET}}$) and the modem driver should re-program the GPIO Pin Sticky register to set the GS1 (or GS11) bit. This will allow the modem driver to read the sticky value of the GPIO Pin Status register.

The Si3054 can also be programmed to wake up on events due to GPIO_A and GPIO_B.

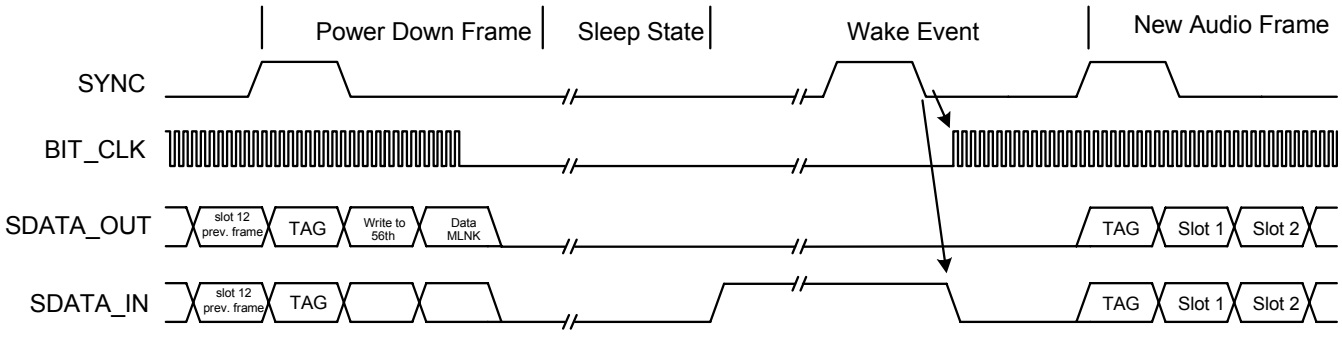


Figure 26. AC-Link Powerdown/Up Sequence

6.15.2. HD Audio Wake-on-Ring

The Si3054 chipset provides wake-up on Ring support when configured as an HD Audio codec as defined by the HD Audio specification. In an implementation designed for wake-up on ring, where the Si3054 is powered by V_{aux}, a ring detected at the RNG1 and RNG2 pins of the Si3054 causes the generation of a power management event to the system. The power management event signal assertion causes the system to resume so that the modem event (ring) can be serviced.

6.16. Pulse Dialing and Spark Quenching

Pulse dialing is accomplished by going off and on hook to generate make and break pulses. The nominal rate is 10 pulses per second. Some countries have very tight specifications for pulse fidelity, including make and break times, make resistance, and rise and fall times. In a traditional solid-state dc holding circuit, there are a number of issues in meeting these requirements.

The Si3054 dc holding circuit has active control of the on-hook and off-hook transients to maintain pulse dialing fidelity.

Spark quenching requirements in countries, such as Italy, the Netherlands, South Africa, and Australia, deal with the on-hook transition during pulse dialing. These tests provide an inductive dc feed resulting in a large voltage spike. This spike is caused by the line inductance and the sudden decrease in current through the loop when going on-hook. The traditional solution to the problem is to put a parallel resistive capacitor (RC) shunt across the hookswitch relay. However, the required capacitor is large (~1 µF, 250 V) and relatively expensive. In the Si3054, loop current can be controlled to achieve three distinct on-hook speeds to pass spark quenching tests without additional BOM components. Through settings of four bits in three registers, OHS (Register 5Ch or NID13), OHS2 (see Page 2: R64h or NID16), SQ1 and SQ0 (Page 2: Register 6Eh or NID18), a slow ramp-down of loop current can be achieved inducing a delay between the time OH bit is cleared and the time the DAA actually goes on-hook.

To ensure proper operation of the DAA during pulse dialing, disable the automatic resistor calibration that is performed each time the DAA enters the off-hook state by setting the RCALD bit.

6.17. Billing Tone Protection and Receive Overload

"Billing tones" or "Metering Pulses" generated by the central office can cause modem connection difficulties.

The billing tone is typically either a 12 kHz or 16 kHz signal and is sometimes used in Germany, Switzerland, and South Africa. Depending on line conditions, the billing tone may be large enough to cause major errors in modem data. The Si3054 chipset can provide feedback indicating the beginning and end of a billing tone.

Billing tone detection is enabled by setting the BTE bit (Register 5Ch or NID13). Billing tones less than 1.1 V_{PK} on the line are filtered out by the low-pass digital filter on the Si3054. The ROV bit is set when a line signal is greater than 1.1 V_{PK}, indicating an ADC overload condition. The BTD bit is set when a line signal (billing tone) is large enough to excessively reduce the internal power supply of the line-side device (Si3018). When the BTD bit is set, the dc termination is changed to an 800 Ω dc impedance to ensure minimum line voltage levels even in the presence of billing tones.

The OVL bit should be monitored (polled) following a billing tone detection. When the OVL bit returns to zero, indicating that the billing tone has passed, the BTE bit should be written to zero to return the dc termination to its original state. It takes approximately one second to return to normal dc operating conditions. The ROV bit is sticky and must be written to zero to be cleared. The BTD bit is read-only and can be cleared by clearing BTE. After the BTE, ROV, and BTD bits are all cleared,

the BTE bit can be set to reenable billing tone detection.

Certain line events, such as an off-hook event on a parallel phone or a polarity reversal, may trigger the ROV or the BTD bits, after which the billing tone detector must be reset. The user should look for multiple events before qualifying whether billing tones are actually present.

Although the DAA remains off-hook during a billing tone event, the received data from the line will be corrupted when a billing tone occurs. If the user wishes to receive data through a billing tone, an external LC filter must be added. A modem manufacturer can provide this filter to users in the form of a dongle that connects on the phone line before the DAA. This keeps the manufacturer from having to include a costly LC filter internal to the modem when it may only be necessary to support a few countries. Alternatively, when a billing tone is detected, the system software may notify the user that a billing tone has occurred. This notification can be used to prompt the user to contact the telephone company and have the billing tones disabled or to purchase an external LC filter.

Disturbances on the line other than billing tones can also cause a receive overload. Some conditions may result in a loop current collapse to a level below the minimum required operating current of the DAA. When this occurs, the dropout detect bit (DOD) is set, and an interrupt will be generated if the dropout detect interrupt mask bit (DODM) is set.

6.18. Billing Tone Filter (Optional)

In order to operate without degradation during billing tones in Germany, Switzerland, and South Africa, an external LC notch filter is required. The Si3054 can remain off-hook during a billing tone event, but modem data is lost in the presence of large billing tone signals. The notch filter design requires two notches, one at 12 kHz and one at 16 kHz. Because these components are fairly expensive and few countries supply billing tone support, this filter is typically placed in an external dongle or added as a population option for these countries. Figure 27 shows an example billing tone filter.

L1 must carry the entire loop current. The series resistance of the inductors is important to achieve a narrow and deep notch. This design has more than 25 dB of attenuation at both 12 kHz and 16 kHz.

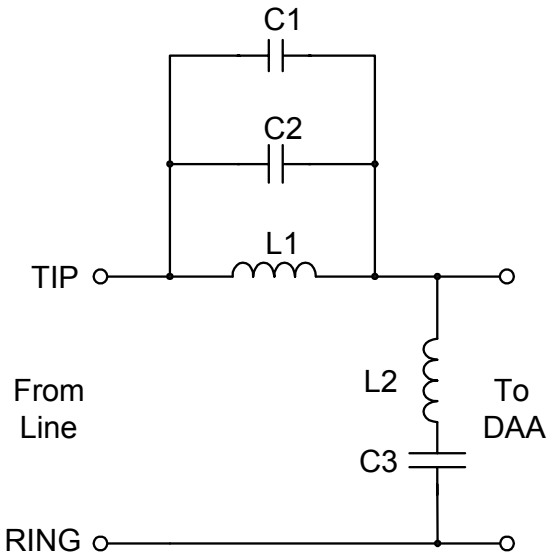


Figure 27. Billing Tone Filter

Table 21. Component Values—Optional Billing Tone Filters

Symbol	Value
C1,C2	0.027 μF, 50 V, ±10%
C3	0.01 μF, 250 V, ±10%
L1	3.3 mH, >120 mA, <10 Ω, ±10%
L2	10 mH, >40 mA, <10 Ω, ±10%

The billing tone filter effects the ac termination and return loss. The current complex ac termination passes worldwide return loss specifications both with and without the billing tone filter by at least 3 dB.

6.19. On-Hook Line Monitor

The on-hook line monitor mode of the Si3054 allows the user to receive line activity when in the on-hook state. A low-power ADC located in the line-side device digitizes the analog signal passed across the RNG1/2 pins and then sends the signal digitally across the communications link to the digital controller. The low-power ADC can be enabled through the LINE1_CID bit in slot 12 (when connected to an AC‘97 controller) or through the CID bit in NID10 (when connected to an HD Audio controller). This mode is typically used to detect caller ID data (see the “6.20.Caller ID” section).

The on-hook line monitor can also be used to detect whether a phone line is physically connected to the Si3018 and associated circuitry. If a line is present and the LINE1_CID or CID bit is set, SDI/SDATA_IN will

have a near-zero value, and the LCS[4:0] bits will read 11111_b. Due to the architecture of the low-power ADC, the data presented on SDI/SDATA_IN may have up to a 15% dc offset.

If no line is connected, the output of SDI/SDATA_IN moves towards a negative full scale value (–32768). The value is guaranteed to be at least 89% of negative full scale. In addition, the LCS[4:0] bits are zero when no line is connected to the DAA.

Caller ID data can be gained up or attenuated using the receive gain or attenuation bits in Register 46h or NID4.

6.20. Caller ID

The Si3054 can pass caller ID data from the phone line to a software caller ID decoder.

6.20.1. Type I Caller ID

Type I Caller ID sends the CID data while the phone is on-hook. In systems where the caller ID data is passed on the phone line between the first and second rings, utilize the following method to capture the caller ID data:

1. After identifying a ring signal using one of the methods described in “Ring Detection” on page 27, determine when the first ring has completed.
2. Assert the LINE1_CID or CID bit to enable the low current caller ID ADC.
3. The low-current ADC, which is powered from the system-side device, digitizes the caller ID data passed across the RNG 1/2 pins.
4. Clear the LINE1_CID or CID bit after the caller ID data is received.

In systems where the caller ID data is preceded by a line polarity (battery) reversal, use the following method to capture the caller ID data.

1. Enable full-wave rectified ring detection (RFWE bit, Register 5Ch or NID13).
2. Monitor the RDTP and RDTN register bits to identify if a polarity reversal or a ring signal has occurred. A polarity reversal trips either the RDTP or RDTN ring detection bits, and thus the full-wave ring detector must be used to distinguish a polarity reversal from a ring. The lowest specified ring frequency is 15 Hz; therefore, if a battery reversal occurs, the DSP software should wait a minimum of 40 ms to verify that the event observed is a battery reversal and not a ring signal. This time is greater than half the period of the longest ring signal. If another edge is detected during this 40 ms pause, this event is characterized as a ring signal and not a battery reversal.
3. Assert the LINE1_CID or CID bit to enable the low current caller ID ADC. The low-current ADC, which is powered from the system-side device, digitizes the caller ID data passed across the RNG 1/2 pins.
4. Clear the LINE1_CID or CID bit after the caller ID data is received.

6.20.2. Type II Caller ID

Type II Caller ID sends the CID data while the phone is off-hook and is often referred to as caller ID/call waiting (CID/CW). To receive the CID data while off-hook, use the following procedure (refer to Figure 28):

1. The Caller Alert Signal (CAS) tone is sent from the Central Office (CO) and is digitized along with the line data. The software must detect the presence of this tone.
2. Since the Si3054 is the only device on the line and is Type II CID compliant, the software must mute its upstream data output to avoid propagation of its reply tone and the subsequent CID data. After muting its upstream data output, the DSP software must then return an acknowledgement (ACK) tone to the CO to request the transmission of the CID data.
3. The CO then responds with the CID data and the software unmutes the upstream data output and continues with normal operation.
4. The muting of the upstream data path by the software mutes the handset in a telephone application so the user cannot hear the acknowledgement tone and CID data being sent.

Because of the nature of the low-power ADC, the data presented to the DSP software could have up to a 10% dc offset. The software caller ID decoder must use either a high-pass or band-pass filter to accurately retrieve the caller ID data.

6.21. Loop Current Sensing

The Si3054 measures loop current. The 5-bit LCS register reports loop current measurements when off-hook. The following can be determined with LCS bits:

- When off-hook, detect if a parallel phone goes on- or off-hook.
- Detect if enough loop current is available to operate.
- Detect if there is an overload condition that could damage the DAA (see “6.23.Overload Protection”).

6.21.1. Loop Current Measurement

When the Si3054 is off-hook, the LCS bits measure loop current in 3.3 mA/bit resolution. These bits detect another phone going off-hook by monitoring the dc loop current. The line voltage current sense transfer function is shown in Figure 28.

The LCS and LCS2 bits report loop current down to the minimum operating loop current for the DAA. Below this threshold, the reported value of loop current is

unpredictable.

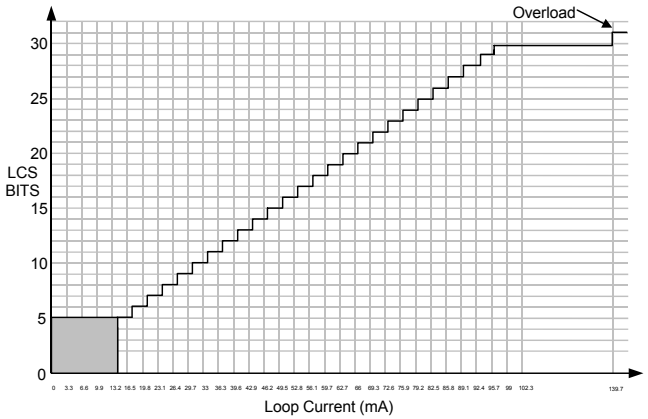


Figure 28. Typical LCS Transfer Function

Table 22. Loop Current Transfer Function

LCS[4:0]	Condition
00000	Insufficient line current for normal operation. Use the DOD bit to determine if a line is still connected.
00100	Minimum line current for normal operation.
11111	Loop current may be excessive. Use the OPD bit to determine if an overload condition exists.

6.22. Parallel Handset Detection

The Si3054 chipset can detect a parallel handset going off-hook. When the Si3054 is off-hook, the loop current can be monitored via the LCS bits. A significant drop in loop current can signal a parallel handset going off-hook. If a parallel handset causes the LCS bits to read 0s, the drop-out detect (DOD) bit can be checked to verify that a valid line exists.

For the Si3054 to operate in parallel with another handset, the parallel handset must have a sufficiently high dc termination to support two off-hook DAAs on the same line. Improved parallel handset operation can be achieved by changing the dc impedance from 50 to 800 Ω and reducing the DCT pin voltage with the DCV[1:0] bits.

6.23. Overload Protection

The Si3054 chipset can detect if an overload condition that could damage the DAA circuit is present. The DAA might be damaged if excessive line voltage or loop current is sustained. When off-hook, if the LCS[4:0] bits are all 1s, an overload condition may exist. If the OPE bit is set (Register 5Eh or NID14) and an overload condition occurs, the OPD bit is set, a dc termination of 800 Ω is automatically presented to the line, and the hookswitch current is reduced. The OPE bit should only be enabled after going off-hook to prevent false activation of this circuit.

6.24. Gain Control

The Si3054 chipset supports multiple gain and attenuation settings (in Register 46h or NID4) for the receive and transmit paths, respectively. The receive path can support gains of 0, 3, 6, 9, and 12 dB, as selected by ADC[3:1] bits. The receive path can also be muted by setting bit 7. The transmit path can support attenuations of 0, 3, 6, 9, and 12 dB, as selected by DAC[3:1] bits. The transmit path can also be muted by setting bit 15.

6.25. Sample Rate Converter

To achieve varying sample rates, the sample rate converter register is programmed to achieve the following sample rates: 7200, 8000, 8229, 8400, 9000, 9600, 10286, 12000, 13714, and 16000 Hz.

6.26. Filter Selection

The Si3054 chipset supports additional filter selections for the receive and transmit signals as defined in Table 15 on page 14 and Table 16 on page 14. The IIRE bit selects between the IIR and FIR filters. The IIR filter provides a lower, but non-linear, group delay than the default FIR filter.

6.27. In-Circuit Testing

The Si3054's advanced design provides the modem manufacturer with increased ability to determine system functionality during production line tests, as well as user diagnostics. Several loopback modes exist allowing thorough coverage of the system components.

The Capacitive Communications Link loopback mode allows the data pump to provide a digital input test pattern on SDO/SDATA_OUT and receive a corresponding digital test pattern back on SDI/SDATA_IN. To enable this mode, set LB = 101 (in Register 56h or NID11). In this mode, the communication link is being tested. The digital stream is delivered across the capacitive communications link (C1 and C2 of "2.Typical Application Schematic," on page 17) to the line-side device and returned across the same path.

The digital DAC loopback mode allows data to be sent on the digital path from SDO/SDATA_OUT to the digital section of DAC, looped back through the AOL, to SDI/SDATA_IN. This loopback mode is used when the line-side chip is in powerdown mode. To enable this mode, set LB = 011.

The remote analog loopback mode allows an external

device to drive the receive pins of the line-side chip and receive the signal from the transmit pins. This mode allows testing of the external components from the RJ-11 (TIP and RING) to the line side device. To enable this mode, set LB = 100 in Register 56h.

The ADC loopback mode allows an external device to drive the receive pins of the Si3018. The signal is then digitized on the Si3018 and sent to the Si3054, which sends the data back to the Si3018. The signal is then converted back to analog, and the external device receives the signal on the transmit pins. This mode allows testing of the Si3054's converters as well as the external components between the Si3018 and RJ-11. To enable this mode, set the LB = 001.

The final two testing modes, local analog loopback and external analog loopback, allow the system to test the operation of the converters in the line side device and the functionality of the external components. In local analog loopback mode, the companion digital controller (AC '97 or HD Audio) provides a digital test waveform through SDO/SDATA_OUT. This data is passed across the communications link, converted to analog, internally looped to the receive path, converted to digital, passed back across the isolation barrier, and presented to the controller. To enable local and analog loopback, set LB = 010. External analog loopback mode tests the entire signal path, including the external components by passing data from SDI/SDATA_IN across the communications link, through the line-side device and external components onto the line. The signal is then received back through the external components and line-side device, across the communications link, and is presented to the digital controller. To enable external analog loopback, set LB = 110. Note that all three analog loopback modes require a line feed for the Si3018.

6.28. Revision Identification

The LREV[3:0] bits identify the revision of the Si3018. Table 23 lists the revision values.

Table 23. Revision Values

Revision	Si3018
C	0011
D	0100
E	0101
F	0110
G	0111

7. AC‘97 Digital Interface

The AC-link serial interconnect defines a digital data and control pipe between the controller and the codec. The AC-link supports 12 20-bit slots at 48 kHz on SDATA_IN and SDATA_OUT. The TDM “slot-based” architecture supports a per-slot valid tag infrastructure that is the source of each slot’s data sets or clears to indicate the validity of the slot data within the current frame. For modem AFE, data streams at a variety of required sample rates can be supported.

7.1. Si3054 as Secondary Device

The Si3054 (Revision E and later) can only operate as a secondary Line 1 device. The primary device is generally an AC ’97 Rev. 2.1-compatible codec that generates BIT_CLK. BIT_CLK is always an input to the Si3054 and is used as the Si3054’s master clock.

7.2. Si3054 Connection to the Digital AC ’97 controller

The Si3054 communicates with its companion AC ’97 controller through a digital serial link called the AC-link. All digital audio streams, optional modem line codec streams, and command/status information is communicated over this point-to-point serial interconnect. Figure 29 illustrates the breakout of the connecting signals.

7.3. Clocking

Clock jitter at the DACs and ADCs is a fundamental impediment to high-quality output, and an internally-generated clock derived from BIT_CLK provides the Si3054 with a clean clock that is independent of the physical proximity of the Si3054’s companion AC ’97 controller.

The beginning of all audio sample packets, or Audio Frames, transferred over AC-link is synchronized to the rising edge of the SYNC signal. SYNC is driven by the AC ’97 controller. The AC ’97 controller takes BIT_CLK as an input and generates SYNC by dividing BIT_CLK by 256 and applying some conditioning to tailor its duty cycle. This yields a 48 kHz SYNC signal whose period defines an audio frame. Data is transitioned on AC-link on each rising edge of BIT_CLK, and subsequently sampled on the receiving side of AC-link on each immediately following falling edge of BIT_CLK.

7.4. Resetting the Si3054

There are three types of reset:

- **Cold reset**—Initializes all Si3054 logic (registers included) to its default state. Initiated by bringing RESET low at least 1 µs during a time when BIT_CLK is inactive.
- **Warm reset**—Leaves the register contents unaltered. Initiated by bringing SYNC high for at least 1 µs in the absence of BIT_CLK.
- **Register reset**—Initializes only the registers to their default states. Initiated by a write to Register 3Ch.

After signaling a reset to the Si3054 chipset, the AC ’97 controller should not attempt to play or capture modem data until it has sampled a Codec Ready indication from the Si3054 chipset. See "7.5.3.AC-Link Audio Input Frame (SDATA_IN)," on page 39.

7.5. AC-Link Digital Serial Interface Protocol

The Si3054 incorporates a 5-pin digital serial interface that links it to the AC ’97 controller. AC-link is a bidirectional, fixed rate, serial PCM digital stream. It handles multiple input and output audio streams (including modems) as well as control register accesses employing a TDM scheme. The AC-link architecture divides each audio frame into 12 outgoing and 12 incoming data streams, each with 20-bit sample resolution.

The Si3054 data streams are as follows:

- **Control**—Control register write port; two output slots
- **Status**—Control register read port; two input slots
- **Modem Line Codec Output**—Modem line codec DAC input stream; one output slot per line
- **Modem Line Codec Input**—Modem line codec ADC output stream; one input slot per line
- **I/O Control**—DAA control and GPIO; one output slot
- **I/O Status**—DAA status and GPIO; one input slot

Synchronization of all AC-link data transactions is signaled by the AC ’97 controller. The Si3054 drives the serial bit clock onto AC-link, which the AC ’97 controller then qualifies with a synchronization signal to construct audio frames.

The SYNC signal, fixed at 48 kHz, is derived by dividing down the serial bit clock (BIT_CLK). BIT_CLK, fixed at 12.288 MHz, provides the necessary clocking granularity to support 12 20-bit outgoing and incoming time slots. AC-link serial data is transitioned on each rising edge of BIT_CLK. The receiver of AC-link data (the Si3054 for outgoing data and the AC ’97 controller for incoming data) samples each serial bit on the falling edges of BIT_CLK.

The AC-link protocol provides for a special 16-bit time slot (Slot 0) wherein each bit conveys a valid tag for its corresponding time slot within the current audio frame. A 1 in a given bit position of slot 0 indicates that the corresponding time slot within the current audio frame

has been assigned to a data stream and contains valid data. If a slot is tagged invalid, it is the responsibility of the data source (the Si3054 for the input stream and the AC '97 controller for the output stream) to populate all bit positions with 0s during that slot's active time.

SYNC remains high for a total duration of 16 BIT_CLKs at the beginning of each audio frame. The portion of the audio frame where SYNC is high is called the Tag Phase. The remainder of the audio frame where SYNC is low is called the data phase. See Figure 30.

Additionally, for power savings, all clock, sync, and data signals can be halted. The Si3054 chipset maintains its register contents intact when entering a power-savings mode.

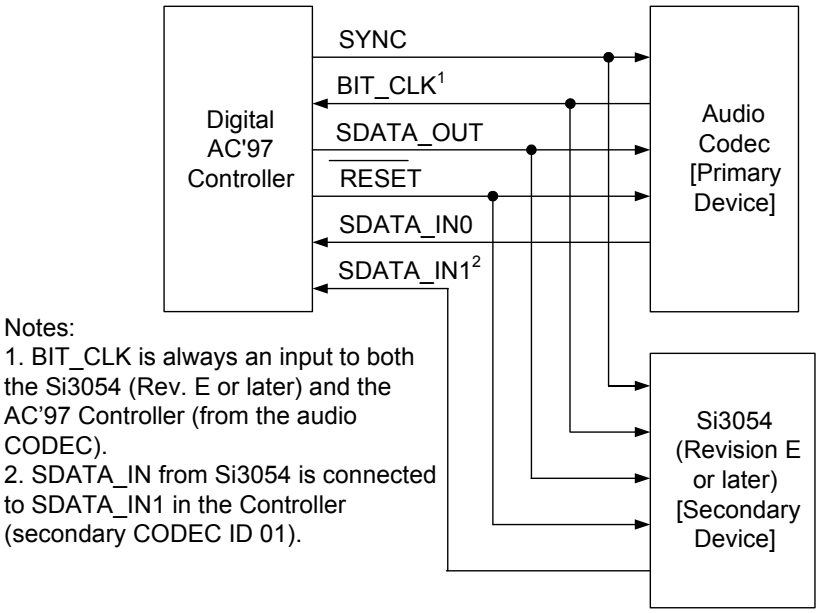


Figure 29. Si3054 Connection To AC '97 Controller

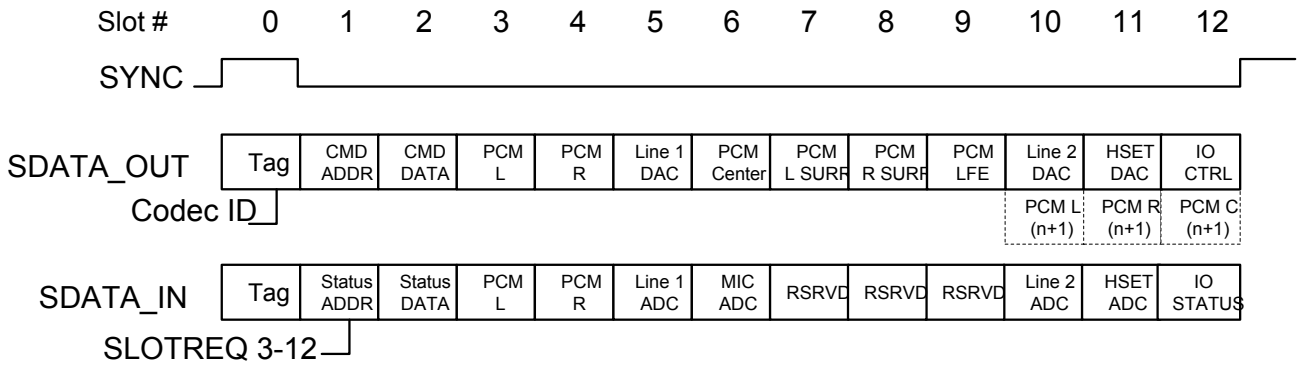


Figure 30. Standard Bidirectional Audio Frame

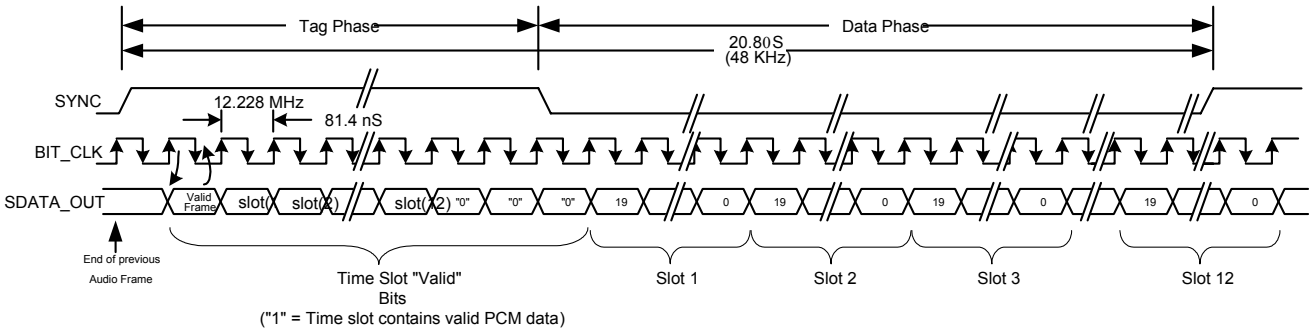


Figure 31. AC-Link Audio Output Frame

7.5.1. AC-Link Audio Output Frame (SDATA_OUT)

The audio output frame data streams correspond to the multiplexed bundles of all digital output data targeting the Si3054's DAC inputs and control registers. Each audio output frame supports up to 12 20-bit outgoing data time slots. Slot 0 is a special reserved time slot containing 16 bits used for AC-link protocol infrastructure.

Within slot 0, the first bit is a global bit (SDATA_OUT slot 0, bit 15) which flags the validity for the entire audio frame. If the Valid Frame bit is a 1, the current audio frame contains at least one slot time of valid data.

The next 12 bit positions sampled by the Si3054 indicate which of the corresponding 12 time slots contain valid data. In this way, data streams of differing sample rates can be transmitted across AC-link at its fixed 48 kHz audio frame rate. Figure 31 illustrates the time slot-based AC-link protocol.

A new audio output frame begins with a low-to-high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, the Si3054 samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising of BIT_CLK, the AC '97 controller transitions SDATA_OUT into the first bit position of slot 0 (Valid Frame bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK and subsequently sampled by the Si3054 on the following falling edge of BIT_CLK. This sequence ensures that data transitions and subsequent sample points for both incoming and outgoing data streams are time-aligned. See Figure 32.

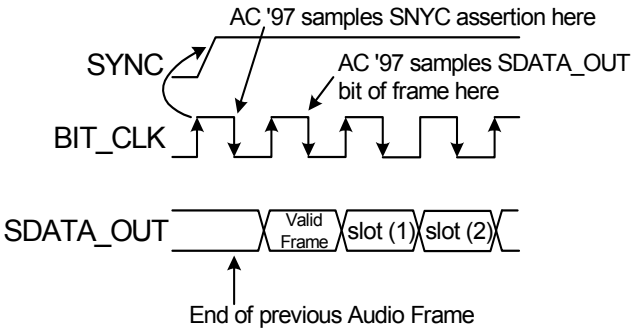


Figure 32. Start of an Audio Output Frame

SDATA_OUT's composite stream is MSB justified (MSB first) with all non-valid slots' bit positions padded with 0s by the AC '97 controller.

In the event that there are less than 20 valid bits within an assigned and valid time slot, the AC '97 controller always pads all trailing non-valid bit positions of the 20-bit slot with 0s.

7.5.2. Variable Sample Rate Signaling Protocol

For variable sample rate output, the codec examines its sample rate control registers, the state of its FIFOs, and the incoming SDATA_OUT tag bits at the beginning of each audio output frame to determine which SLOTREQ bits (bit 4 or 9 in SDATA_IN Slot 1) to set active (low). SLOTREQ bits asserted during the current audio input frame signal which active output slots require data from the AC '97 Digital Controller in the next audio output frame. An active output slot is defined as any slot supported by the codec that is not in a powerdown state.

The SLOTREQ signal is dependent on the current power state. The following is a list of conditions in which the SLOTREQ for slot 5 is active and conditions in which it is inhibited:

- SLOTREQ is active every frame when the PRD/PRF is set (Reg 3E, bit 11/13). (DAC is powered down.) This is required by the AC ’97 specification for compatibility with 48 kHz AC ’97 rev. 1.03 codecs.
- SLOTREQ is inhibited (high) if the MLNK bit is set (Register 56, bit 12), and AC-Link halt is impending.

7.5.2.1. Slot 1: Command Address Port

The Command Address Port controls features and monitors status (see Audio Input Frame Slots 1 and 2) for Si3054 chipset functions including, but not limited to, sample rate, AFE configuration, and power management.

The control interface architecture supports up to 64 16-bit read/write registers addressable on even byte boundaries. Only the even registers (00h, 02h, etc.) are valid; odd register (01h, 03h, etc.) writes are ignored, and reads return 0. Note that shadowing of the control register file on the AC ’97 controller is an option left open to the implementation of the AC ’97 controller. The Si3054’s control register file is readable as well as writable to provide more robust testability.

Audio output frame slot 1 communicates control register address and write/read command information to the Si3054 chipset.

Command Address Port bit assignments:

- Bit(19)—Read/Write command (1 = read, 0 = write)
- Bit(18:12)—Control Register Index (64 16-bit locations, addressed on even byte boundaries)
- Bit(11:0)—Reserved (padded with 0s)

The first bit (MSB) sampled by the Si3054 indicates whether the current control transaction is a read or a write operation. The following seven bit positions communicate the targeted control register address. The trailing 12 bit positions within the slot are reserved and must be padded with 0s by the AC ’97 controller.

7.5.2.2. Slot 2: Command Data Port

The Command Data Port delivers 16-bit control register write data in the event that the current command port operation is a write cycle as indicated by Slot 1, bit 19.

Command Data Port bit assignments:

- Bit(19:4)—Control Register Write Data (padded with 0s if the current operation is a read)
- Bit(3:0)—Reserved (padded with 0s)

7.5.2.3. Slot 5: Modem Line 1 DAC

Audio output frame slot 5 contains MSB-justified modem DAC output data. The modem DAC output resolution is 16 bits.

The Si3054 receives its DAC data MSB first.

Slot 5 data is sent by the controller at a rate below the 48 kHz rate of the AC-Link. Therefore, “tags” are used to mark when there is valid data in slot 5. The tag for slot 5 is bit 10 in slot 0. Tag bits are sent by the controller in response to a SLOTREQ on SDATA_IN.

7.5.2.4. Slot 12: Modem GPIO Control

Slot 12 contains latency critical signals for the Si3018 and the GPIO of the Si3054. See Table 24.

7.5.2.5. Slots 3, 4, 6–9, 11: Not Used

The Si3054 always pads audio output frame slots 3, 4, 6–9, and 11 with 0s.

7.5.3. AC-Link Audio Input Frame (SDATA_IN)

The audio input frame data streams correspond to the multiplexed bundles of all digital input data targeting the AC ’97 controller. This is the case with the audio output frame; each AC-link audio input frame consists of 12 20-bit time slots. Slot 0 is a special reserved time slot containing 16 bits that are used by the AC-link protocol infrastructure.

Within slot 0, the first bit is a global bit (SDATA_IN slot 0, bit 15) that flags whether the Si3054 is in the Codec Ready state or not. If the Codec Ready bit is a 0, the Si3054 is not ready for normal operation. This condition is normal following the deassertion of reset (e.g., while the Si3054’s voltage references settle). When the AC-link Codec Ready indicator bit is a 1, the AC-link and Si3054 control and status registers are in a fully-operational state. The AC ’97 controller must further probe the Powerdown Control/Status register to determine exactly which subsections, if any, are ready.

Before any attempts to put the Si3054 chipset into operation, the AC ’97 controller should poll the first bit in the audio input frame (SDATA_IN slot 0, bit 15) for an indication that the Si3054 is Codec Ready. When the Si3054 is sampled Codec Ready, the next 12 bit positions sampled by the AC ’97 controller indicate which of the corresponding 12 time slots are assigned to input data streams and that they contain valid data. Figure 33 illustrates the time-slot-based AC-link protocol.

A new audio input frame begins with a low-to-high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the next falling edge of BIT_CLK, the Si3054 samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame.

On the next rising of BIT_CLK, the Si3054 transitions SDATA_IN into the first bit position of slot 0 (Codec Ready bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK and subsequently sampled by the AC ’97 controller on the following falling edge of BIT_CLK. This sequence ensures that data transitions and subsequent sample points for both incoming and

outgoing data streams are time aligned.

SDATA_IN's composite stream is MSB justified (MSB first) with all non-valid bit positions (for assigned and unassigned time slots) padded with 0s by the Si3054. SDATA_IN data is sampled on the falling edges of BIT_CLK by the AC '97 controller.

Table 24. Slot 12

GPIO	Name	Sense	Description
GPIO15:8	Reserved		
GPIO7	LINE1_DAAINT	Out	DAA Interrupt, Line 1
GPIO6	LINE1_LCSOVL	In	LCS Overload, Line 1
GPIO5	LINE1_GPIO_B	In/Out	GPIO pin B, Line 1
GPIO4	LINE1_GPIO_A	In/Out	GPIO pin A, Line 1
GPIO3	LINE1_DLCS	In	Delta Loop Current Sense, Line 1
GPIO2	LINE1_CID	Out	Caller ID path enable, Line 1
GPIO1	LINE1_RI	In	Ring Detect, Line 1
GPIO0	LINE1_OH	Out	Off Hook, Line 1
Vendor Optional			
Bit 3	Reserved		
Bit 2	Reserved		
Bit 1	LINE1_FDT	In	Frame Detect, Line 1
Bit 0	GPIO_INT	In	GPIO state change

7.5.3.1. Slot 1: Status Address Port

The Status Address Port monitors status for Si3054 functions including, but not limited to, line-side configuration.

Audio input frame slot 1's stream echoes the control register index for historical reference and for the data to be returned in slot 2. (Assuming that slots 1 and 2 have been tagged "valid" by the Si3054 during slot 0).

Status Address Port bit assignments:

- Bit(19)—Reserved (padded with 0)
- Bit(18:12)—Control Register Index (Echo of register index for which data is being returned)
- Bit(11:2)—SLOTREQ bits, bit 9 for Line 1 and bit 4 for Line 2. (See "7.5.2.Variable Sample Rate Signaling Protocol," on page 38 for more details.)
- Bit(1,0)—Reserved (padded with 0s)

The first bit (MSB) generated by the Si3054 is always padded with a 0. The following seven bit positions communicate the associated control register address and the trailing 12 bit positions are padded with 0s by the Si3054.

7.5.3.2. Slot 2: Status Data Port

The Status Data Port delivers 16-bit control register read data.

Status Data Port bit assignments:

- Bit(19:4)—Control Register Read Data (padded with 0s if tagged invalid by the Si3054)
- Bit(3:0)—Reserved (padded with 0s)

If Slot 2 is tagged invalid by the Si3054, the entire slot is padded with 0s by the Si3054.

7.5.3.3. Slot 5: Modem Line 1 ADC

Audio input frame slot 5 contains MSB-justified modem ADC output data. The modem ADC output resolution is 16 bits.

The Si3054 ships out its ADC output data MSB first and pads any trailing non-valid bit positions with 0s to fill out its 20-bit time slot.

Slot 5 data is sent by the controller at a rate below the 48 kHz rate of the AC-link. Therefore, "tags" are used to mark when there is valid data in slot 5. The tag for slot 5 is bit 10 in slot 0.

The tag for slot 5 is dependent on the current power state. Slot 5 is inhibited by the following:

- PRC/PRE bit is set (Register 3E, bit 10/12); ADC is powered down.
- MLNK bit is set (Register 56, bit 12); AC-Link halt is impending.

Note that slot 5 is active when the DAA is on-hook in order to pass ringer and caller-ID data.

7.5.3.4. SSlot 12: Modem GPIO Status

Slot 12 contains latency-critical signals for the Si3018 and the GPIO of the Si3054. Slot 12 also reflects the status of the link between the Si3054 and Si3018. See Table 24.

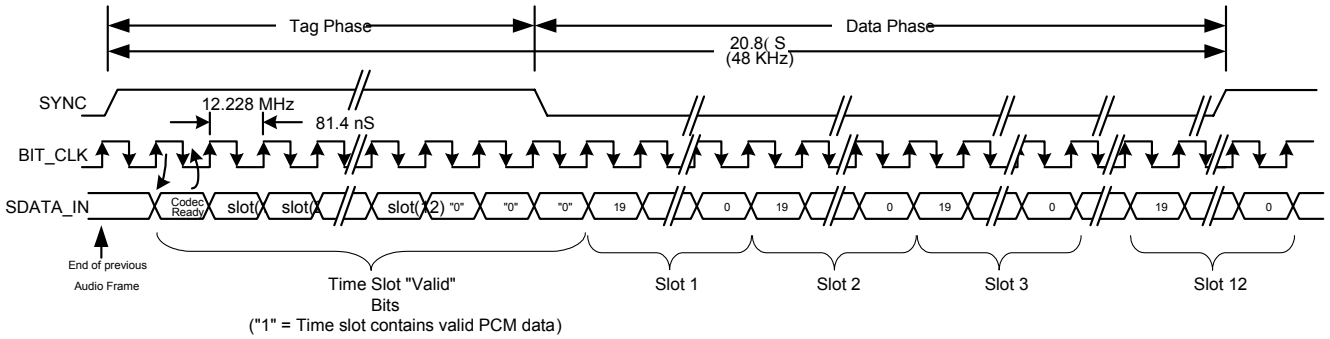


Figure 33. AC-Link Audio Input Frame

7.6. Codec Register Access

When the AC '97 Digital Controller addresses the Si3054 as a secondary codec, the Slot 0 Tag bits for Address and Data must be zero. A non-zero, 2-bit codec ID in the LSBs of Slot 0 indicates a valid Read or Write Address in Slot 1, and the Slot 1 R/W bit indicates presence or absence of valid Data in Slot 2. See Table 25.

In order for the AC '97 Digital Controller to independently access Primary and Secondary Codec registers, a 2-bit Codec ID field (chip select) is used in the LSBs of Output Slot 0.

For Secondary Codec access, the AC '97 Digital Controller must invalidate the tag bits for Slot 1 and 2 Command Address and Data (Slot 0, bits 14 and 13) and place a non-zero value (01) into the Codec ID field (Slot 0, bits 1 and 0).

When configured as a secondary codec, the Si3054 disregards the Command Address and Command Data (Slot 0, bits 14 and 13) tag bits when a 2-bit Codec ID value (Slot 0, bits 1 and 0) is sent that matches the ID configuration. In a sense, the Secondary Codec ID field functions as an alternative Valid Command Address (for Secondary reads and writes) and Command Data (for Secondary writes) tag indicator.

The Si3054 monitors the Frame Valid bit and ignores the frame (regardless of the state of the Secondary Codec ID bits) if it is not valid. The AC '97 Digital Controllers should set the frame valid bit for a frame with a secondary register access, even if no other bits in the output tag slot except the Secondary Codec ID bits are set. See Table 26.

Table 25. Secondary Codec Addressing: Slot 0 Tag Bits

Function	Slot 0, bit 15 (Valid Frame)	Slot 0, bit 14 (Valid Slot 1 Address)	Slot 0, bit 13 (Valid Slot 2 Data)	Slot 0, Bits 1–0 (Codec ID)
AC '97 Digital Controller Secondary Read Frame N, SDATA_OUT	1	0	0	01 or 10
AC '97 Digital Controller Secondary Write Frame N, SDATA_OUT	1	0	0	01 or 10
Si3054 Status Frame N + 1, SDATA_IN	1	1	1	00

Table 26. Secondary Codec Register Access Slot 0 Bit Definitions

Output Tag Slot (16-bits)	
Bit	**Description**
15	Frame Valid
14–13	Reserved (Set to 0)
12–3	Slot 3: 12 Valid bits as defined by AC '97
2	Reserved (Set to 0)
1–0	2-bit Codec ID field (00 reserved for Primary; 01 indicates Secondary)

7.7. AC-Link Low Power Mode

The AC-link signals can be placed in a low-power mode. When AC '97's Powerdown Register is programmed to the appropriate value, both BIT_CLK and SDATA_IN are brought to and held at a logic low voltage level.

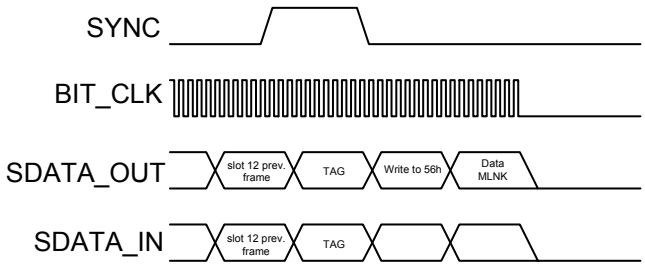


Figure 34. AC-Link Powerdown Timing

BIT_CLK and SDATA_IN are transitioned low immediately following the decode of the write to the Register 56h with MLNK. When the AC '97 controller driver is at the point where it is ready to program the AC-link into its low-power mode, slots 1 and 2 *are* assumed to be the only valid stream in the audio output frame.

The AC '97 controller should also drive SYNC and SDATA_OUT low after programming the Si3054 to this low-power mode.

When the primary codec on the link has halted BIT_CLK, a special wakeup protocol must be used to bring the AC-link to the active mode because normal audio output and input frames cannot be communicated in the absence of BIT_CLK. See Figure 34.

Note: The Si3054's PLL must be initialized before being placed in sleep mode. PLL is initialized by writing a sample rate in Register 40h (42h).

7.7.1. Waking Up the AC-Link

There are two methods for bringing the AC-link out of a low-power, halted mode. Regardless of the method, the AC '97 controller performs the wake-up task.

AC-link protocol provides for a cold reset and a warm reset. The current power-down state ultimately dictates which form of reset is appropriate. Unless a cold or register reset (a write to the Reset register) is performed (wherein the registers are initialized to their default values), registers are required to keep state during all powerdown modes.

When powered down, reactivation of the AC-link through reassertion of the SYNC signal must not occur for a minimum of four audio frame times following the frame in which the power-down was triggered. When AC-link powers up, the Si3054 indicates readiness through the Codec Ready bit (input slot 0, bit 15).

The Si3054 can be enabled to indicate a power management event has occurred (e.g., ring detection) while in low-power mode. See Register 52h on page 62 for more details.

7.7.1.1. Si3054 Cold Reset

A cold reset is achieved by asserting $\overline{\text{RESET}}$ for the minimum specified time. By driving $\overline{\text{RESET}}$ low, BIT_CLK and SDATA_OUT are activated, or re-activated as the case may be, and all Si3054 control registers are initialized to their default power-on reset values. It should be noted that while $\overline{\text{RESET}}$ is low, the Si3054 remains active. Upon the rising edge of $\overline{\text{RESET}}$, the Si3054 performs a cold reset. $\overline{\text{RESET}}$ is an asynchronous Si3054 input.

7.7.1.2. Si3054 Warm Reset

A warm reset reactivates the AC-link without altering the current Si3054 register values. A warm reset is signaled by driving SYNC high for a minimum of 1 µs in the absence of BIT_CLK.

Within normal audio frames, SYNC is a synchronous Si3054 input. However, in the absence of BIT_CLK, SYNC is treated as an asynchronous input used in the generation of a Warm reset to the Si3054.

8. HD Audio Digital Interface

The building blocks of the HD Audio architecture are shown in Figure 35. The Si3054 is connected to the HD Audio controller via a 5-pin HD Audio Link digital serial interface. Like its predecessor AC-Link, HD Audio is a bidirectional, fixed rate, serial PCM digital stream. In contrast to AC'97, HD Audio provides for an additional HW abstraction layer to minimize modem driver dependencies on the link controller. In the HD Audio architecture, the modem driver communicates Si3054 status and control with verbs to the HD Audio bus driver, which in turn communicates directly to the HD Audio controller.

8.1. HD Audio Signal Definitions

The HD Audio architecture supports up to 15 codecs connected to the HD Audio controller. Figure 36 illustrates the connection of one Si3054 to an HD Audio controller. BCLK, SYNC, SDO, and $\overline{\text{RST}}$ are all driven by the controller and connected as a single multi-drop network when multiple codecs are connected. Each codec has its own point-to-point SDI signal connected separately to the HD Audio controller.

- BCLK—24.00 MHz clock sourced from the HD Audio controller.
- SYNC—This signal marks input and output frame boundaries and identifies outbound data streams (stream tags). SYNC is sourced from the HD Audio controller.
- SDO—Bussed serial data output signal driven by the HD Audio controller. Data is double-pumped (data is driven and sampled with respect to every edge of BCLK).
- SDI—Point-to-point serial data input signal driven by the Si3054. Data is single-pumped (data is driven and sampled with respect to the rising edge of BCLK).
- $\overline{\text{RST}}$—Active low link reset signal sourced from the HD Audio controller.

8.2. Digital Signaling

The HD Audio Link is the digital serial interface that connects the Si3054 to the HD Audio Controller. The HD Audio link protocol is controller-synchronous, based on a fixed 24.00 MHz clock, and is purely isochronous (no flow control) with a 48 kHz framing period. Separate input and output serial digital signals support inbound and outbound streams and fixed command and response channels as shown in Figure 37.

8.3. Relative Signal Timing

The HD Audio Link defines 500 input bit cells on SDI and 1000 output bit cells on SDO in each isochronous frame. Figure 38 shows these bit streams numbered from 499 to 0 and from 999 to 0. Notice that bit 499 on SDI aligns with bits 999 and 998 on SDO, all beginning with the falling edge of SYNC, which marks the beginning of a new frame.

The timing of SDI, SDO, and SYNC are all defined with respect to BCLK. Note that Figure 38 shows output bit cell 999 and input bit cell 499 as well as the falling edge of Frame Sync, all driven relative to a rising edge of BCLK.

Since the HD Audio link is a purely isochronous transport mechanism, all link data transmission occurs within periodic time frames. A frame is a 20.833 µs window of time marked by the falling edge of the Frame Sync marker, which identifies the start of each frame. The HD Audio controller is responsible for generating the Frame Sync marker, which is a high-going pulse on SYNC, exactly 4 BCLK cycles (8 SDO bit times) in width, as shown in Figure 38.

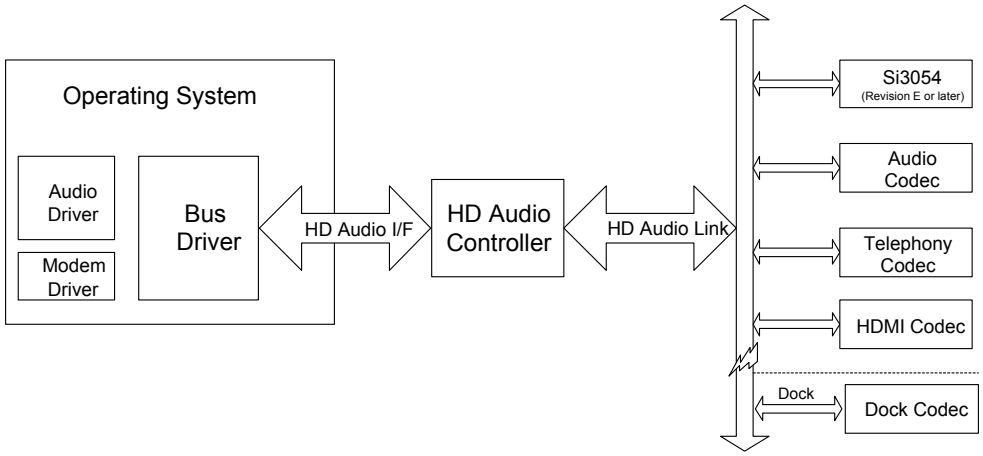


Figure 35. HD Audio Architecture

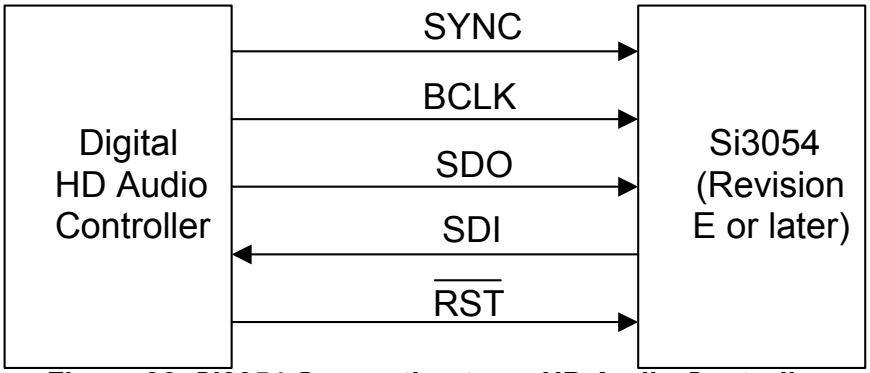


Figure 36. Si3054 Connection to an HD Audio Controller

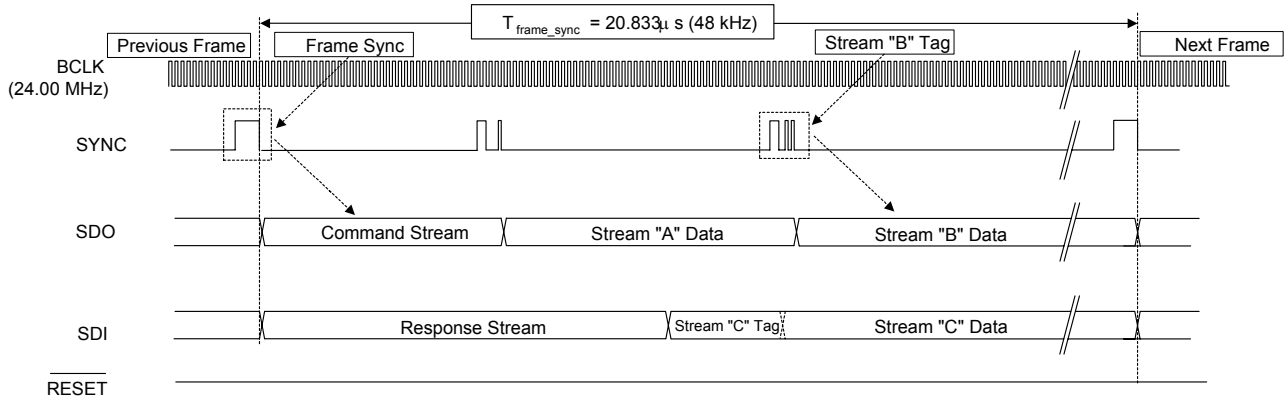


Figure 37. HD Audio Link Conceptual View

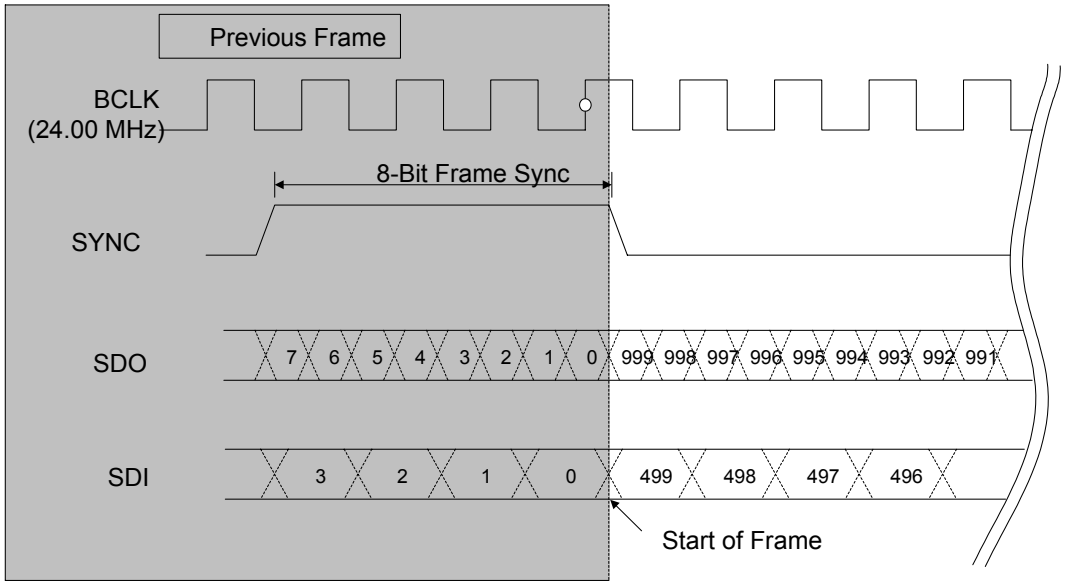


Figure 38. SDO and SDI Bit Timing

8.4. SDO Stream Tags

SDO Stream Tags are 8 bits in length and are transmitted at a double-pumped rate as side band information on SYNC. SDO stream tags delineate the beginning of each new outbound stream packet. SDO stream tags are transmitted on SYNC so as to align with the last eight (data) bits of the preceding stream packet or command field. The format of an SDO tag is shown in Figure 39. It is comprised of a 4-bit preamble that is signaled as three SDO bit times high followed by one SDO bit time low. This is immediately followed by a 4-bit Stream ID, MSB justified, which identifies the specific stream to which the subsequent sample blocks are associated. Samples are transmitted on SDO immediately following the LSB of the SDO tag.

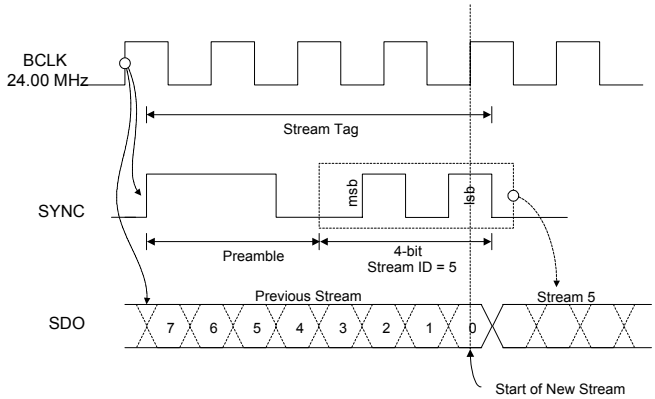


Figure 39. Outbound Stream Tag Format and Transmission

8.5. SDI Stream Tags

An SDI Stream Tag is 10 bits in length and is transmitted at a single-pumped rate on SDI immediately preceding the associated inbound sample data. The Inbound Stream Tag specifies the length of each inbound stream packet and identifies the associated stream ID. The format of an SDI Stream Tag is shown in Figure 40. The 4-bit Stream ID and the 6-bit data length fields are transmitted MSB justified.

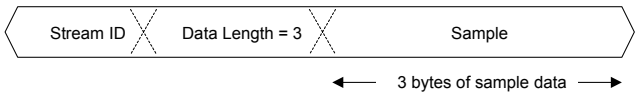


Figure 40. SDI Stream Tag Format

8.6. SDO Frame Composition

SDO is comprised of command and sample data outbound from the controller to the Si3054 and other codecs. SDO frames start and end between the falling edges of successive Frame Syncs. The first 40 bits of an SDO frame are dedicated for the Command field to send commands from the HD Audio Controller to the Si3054. Sample data for the first stream is transmitted on SDO immediately following the command field. The HD Audio controller is required to transmit a null field for the remaining bits within an SDO frame when the transmission of the stream packets completes before the end of the frame. Null fields are only permitted after all outbound stream packets have been transmitted. Figure 41 shows a typical SDO frame. Link sample rates are programmed in NID 3.

8.7. SDI Frame Composition

SDI is comprised of a command response stream (status), stream tags, and the associated sample data transmitted from the Si3054 to the HD Audio Controller. SDI frames start and end between the falling edges of successive Frame Syncs. The first 36 bits of an SDI frame are dedicated to the Response field, which the Si3054 uses for sending responses to controller commands or unsolicited responses to events detected by the Si3054. The Si3054 transmits sample data on SDI immediately following the Response field. A termination tag must immediately follow the sample data to mark the completion of data transmission within the frame. A termination tag is comprised of a stream packet length of zero. The remainder of valid bit positions following the termination tag must be set to the null field (logical zeros). Figure 42 shows a typical outbound frame.

8.8. Sample Rates

V.9x modem sample rates can be different than the common audio sample rates natively supported by the HD Audio link. Due to the relatively low data rates associated with V.9x modems and the unlikelihood that modem codecs will be grouped with other codecs, the HD Audio Link does not natively support many modem-specific sample rates in the TX direction. Since the codec initiates data transfers in the RX direction, HD Audio effectively supports any sample rate in the RX direction. The signaling method described below is used to compensate for the lack of some modem transmit sample rates on the HD Audio link.

HD Audio Link sample rates of 8000 Hz, 9600 Hz, 12 kHz, and 16 kHz are available; thus, modem sampling at these same rates is natively supported. In order to use the other modem transmit sample rates in Table 27, the modem codec sample length must be increased from the standard 16-bit to 24-bit. In the 24-bit protocol, the MSB of the top eight bits in the 24-bit modem codec sample is used to indicate the presence (MSB = 1) or absence (MSB = 0) of a valid sample. In

conjunction with programming the Si3054 for 24-bit sample length, the modem driver must select a link sample rate at least as high as the actual modem sample rate.

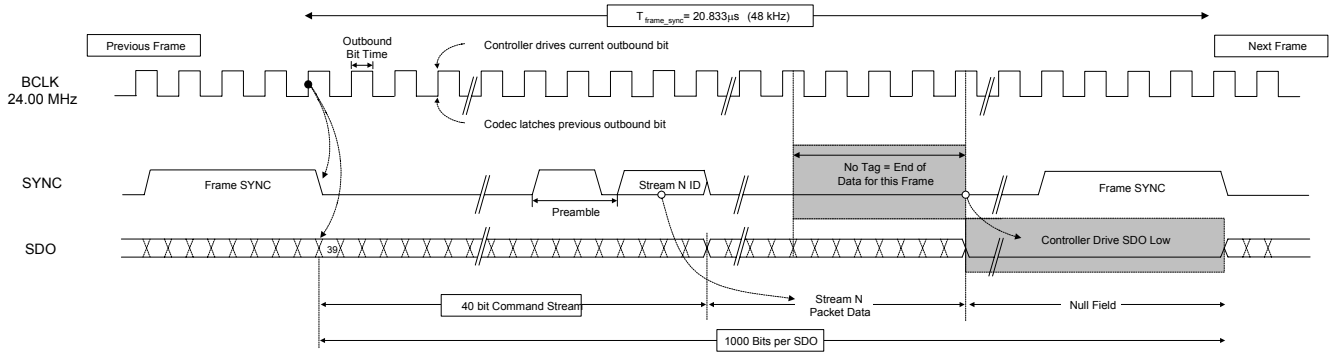


Figure 41. SDO Frame with Null Field

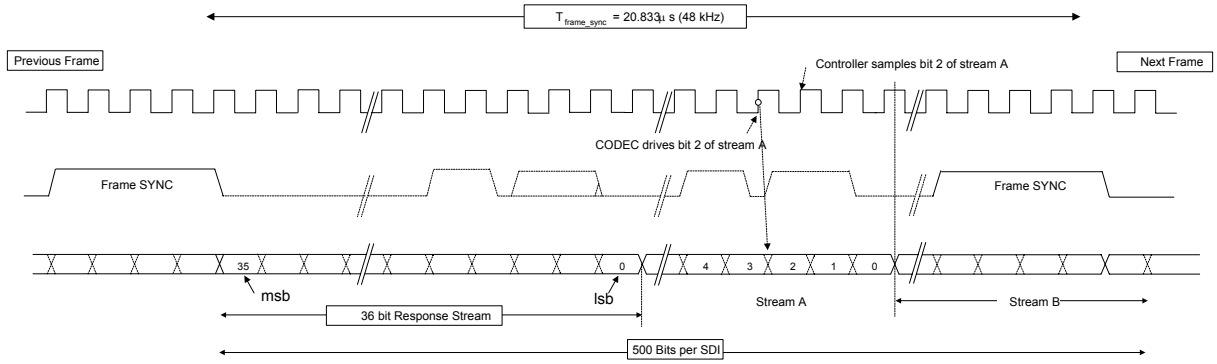


Figure 42. Typical SDI Frame

Table 27. Modem Transmit Sample Patterns

Modem Transmit Sample Rate	Link Sample Rate	Sample pattern (based on link sample rate) p – present, a – absent
7200	8000	xxxxxxxxx-xxxxxxxxx- (9p,1a)
8000	8000	All p
8228.57 (57600/7)	9600	xxxxxx-xxxxxx- (6p, 1a)
8400	9600	xxxxxxx-xxxxxxx- (7p, 1a)
9000	9600	xxxxxxxxxxxxxxx-xxxxxxxxxxxxxxx-(15p,1a)
9600	9600	All p
10285.71(72000/7)	12000	xxxxxx-xxxxxx- (6p, 1a)
12000	12000	All p
13714.28(96000/7)	16000	xxxxxx-xxxxxx- (6p, 1a)
16000	16000	All p

Table 27 shows how the modem driver has to pack samples into memory before they are transferred using DMA and transmitted. For example, when selecting a modem sample rate of 7200 Hz, the modem driver would program the link sample rate to 8000, and the DMA buffer would look like Figure 43:

DMA byte offset 0:	
10..00	Sample n
10..00	Sample n+1
10..00	Sample n+2
10..00	...
10..00	Sample n+8
00..00	
10..00	Sample n+10
10..00	Sample n+11
10..00	Sample n+12
10..00	...
10..00	Sample n+19
00..00	
8 bits	16 bits

Figure 43. Modem Transmit DMA Buffer with MSB Signaling (modem sample rate = 7200 Hz)

Note that some HD Audio DMA controllers may require additional padding of the TX samples to 32-bits when the sample size is 24-bit. Consult the documentation for the HD Audio bus driver for additional packing requirements.

8.9. Commands and Status on HD Audio

To issue a Codec command in the HD Audio architecture, software accesses a shared command buffer (CORB), and the contents are transferred via DMA directly to the link. This means that under HD Audio, it is up to software to guarantee fair use of the serial interface. The bus driver for HD Audio can be responsible for this; it does not have to be distributed among the Codec function drivers. The modem function driver calls the bus driver, which puts the commands in the CORB. It is important to note that in the HD Audio architecture, writing GPIO data is no different than any other command. In contrast, AC'97 dedicates one slot per output frame (slot 12) to the modem; thus, the modem driver has a mechanism to access the link whose latency is independent of whether commands are being sent to other codecs. In HD Audio, GPIO output data is written to the CORB just like any other command. This means that the latency in changing GPIO pins is higher on HD Audio than it is on AC'97.

Analogous to commands, in the HD Audio architecture, status is transferred directly to a shared buffer (RIRB) using DMA. Since each Codec has its own SDATA_IN signal, fair use of the serial interface is not an issue as it is with commands. However, response latency is higher on HD Audio than it is on AC'97 due to the fact that the RIRB is shared between all Codecs. So, even though fair use of the link isn't an issue for returning status on HD Audio, fair use of the RIRB is; the RIRB can contain a different number of responses per Codec.

The command and status fields appear exactly once per frame on SDO and SDI respectively. The 40-bit command field and the 36-bit status field are always the first fields within a frame and are both formatted MSB-first. The 40-bit command field is defined in Table 28. The top eight bits in the command field are either reserved or special-purpose bits. The 36-bit response field is defined in Table 29. The UnSol and response field bits are only meaningful if the valid bit is set to 1. Bits [33:32] are reserved on special-purpose bits transmitted as zeros.

Table 28. HD Audio Link Command Field Format

39:32	31:28	27:20	19:0
Reserved	CAd	NID	Verb

Notes:
Reserved = Transmitted as zeros
CAd = Codec Address
NID = Register Address
Verb[19:0] = Verb encoding and payload

Table 29. HD Audio Link Response Field Format

35	34	33:32	31:0
Valid	UnSol	Reserved	Response

Notes:
Valid = A "1" in this bit position indicates the response field contains a valid response, which the controller will place in the RIRB. A "0" indicates there is no response.
UnSol = A "1" indicates the response is unsolicited. A "0" indicates the response is a reply to a verb.
Reserved = Transmitted as zeros.

8.10. Modem GPIO Control

The Si3054 supports two schemes for GPIO control. GPO bits are either embedded in the data stream in 24-bit data mode, or GPI bits are available from Unsolicited Response (GPI and GPO are also R/W through regular register access). To avoid conflict or confusion between these two schemes (embedded and unsolicited response) of reporting GPI status, the verb "set unsolicited response" is used to set the unsol_enable register bit to enable the unsolicited response mode of GPI control.

8.10.1. Modem GPIO Embedded in Data Stream

Si3054 GPIO embedded in the data stream provides for real-time command or status reporting. This scheme of GPIO control minimizes latency in changing GPIO pins (in contrast with regular register access through commands transferred from the shared HD Audio command buffer). In order to support this mode, data for both transmit and receive must be programmed to be 24-bits using the "Set Converter Format" command. The formatting for 24-bit outbound and inbound data streams with embedded GPIO bits is shown in Tables 30 and 31.

Table 30. SDI Data Format for 24-Bit Data with Embedded GPI Bits

Bit	Name	GPI	Description
23	GPIO_A	GPI7	Pin 16 general purpose I/O
22	GPIO_B	GPI6	Pin 15 general purpose I/O
21	DAAINT	GPI5	DAA interrupt
20	LCSOVL	GPI4	LCS overload
19	DLCS	GPI3	Delta Loop Current Sense
18	RDT	GPI2	Ring detect
17	FDT	GPI1	Frame detect
16	GPIO_INT	GPI0	GPIO state change
15:0	Data[15:0]		16-bit RX data

Table 31. SDO Data Format for 24-Bit Data with Embedded GPO Bits

Bit	Name	GPO	Description
23	Data_valid		Indication of valid data stream
22	GPIO_valid*		Indication of valid GPIO bits*
21	Reserved		Returns zero
20	OPE	GPO4	Overload protect enable
19	GPIO_B	GPO3	
18	GPIO_A	GPO2	
17	CID	GPO1	Caller ID path enable
16	OH	GPO0	Off hook
15:0	Data[15:0]		16-bit TX data
***Note:** Independent of data valid.			

8.10.2. Unsolicited Response Modem GPIO Control

The “Unsolicited Response” control determines whether the Si3054 is enabled to send an unsolicited response, as well as what the tag will be for the response. The HD Audio unsolicited response verb is used to set the Si3054 to generate unsolicited responses. If the Enable bit in the Set Unsolicited response verb is a one, a status change on enabled GPI bits triggers an unsolicited response. The response is sent in the SDI response field when there is no response requested in that frame. The format of the unsolicited response on SDI is shown in Table 33. The GPI unsolicited enable mask is controlled by the GPI pin wake-up mask register. The value programmed into the Tag field of the unsolicited response verb is returned in the top six bits of every unsolicited response generated by the Si3054. The six-bit Tag value is opaque to the codec and is used by software to determine what codec node generated the unsolicited response. Si3054 GPIOs are listed in Table 32. When unsolicited response GPIO control is enabled, data for both transmit and receive must be programmed to be 16-bits using the “Set Converter Format” command. The formatting for 16-bit outbound and inbound data streams without embedded GPIO bits is demonstrated in Table 34.

Table 32. Si3054 GPIO

GPIO	Name	Description
GPO4	OPE	Overload Protect Enable
GPO3	GPO_B	GPIO Pin A, controlled by GCI7
GPO2	GPO_A	GPIO Pin B, controlled by GCI6
GPO1	CID	Caller ID Path Enable
GPO0	OH	Off Hook
GPI7	GPIO A	GPIO Pin A
GPI6	GPIO B	GPIO Pin B
GPI5	DAA INT	DAA Interrupt
GPI4	LCSOVL	Loop Current Sense Overload
GPI3	DLCS	Delta Loop Current Sense
GPI2	RDT	Ring Detect
GPI1	FDT	Frame Detect
GPI0	GPIO INT	GPIO State Change

Table 33. Data Format for Unsolicited Response (sent in SDI)

31:26	25:21	20:13	12	11	10	9	8	7:0
Tag	Returns 0	LCS[7:0]	Returns 0	ROV	BTD	DOD	Returns 0	GPI[7:0]
Note: Refer to GPIO definitions in register descriptions for NIDs 5–10 and 14.								

Table 34. Data Format for 16-Bit Data without Embedded GPI Bits

Stream	Bit	Name	Description
SDO	15:0	Data[15:0]	16-bit TX data
SDI	15:0	Data[15:0]	16-bit RX data

Table 35. Parameter Requests Supported in the Si3054

Verb Name	Encoding	Node Name	NID	Default	Parameter #	Parameter Name
Get Parameter	F00h	Root Node	0	NA	00h	Vendor ID
		Root Node	0	0x1007	02h	Revision ID
		Root Node	0		04h	Subordinate Node Count
		Modem FnGrp	1	0x0102	05h	Function group type
		Modem FnGrp	1	0x000F	0Fh	Supported power states
		Modem FnGrp	1		04h	Subordinate Node Count

8.11. Modem Codec Verbs

The list of parameters and controls supported in the Si3054 are described in Tables 35 and 36. Parameters return static read-only information about the capabilities or configuration options of the Si3054 registers. Controls have an effect on the behavior of the Si3054. Most controls are readable and writable using separate verbs defined for accessing each specific control, but some controls (such as RST) are essentially write-only, and there is no associated verb to read a value. The Converter Format control determines the format that the Si3054 codec will use. This setting must match the format programmed into the Stream descriptor on the controller so that the data being transmitted on the link matches what is expected by the modem function driver (format information includes link sample rate and bits per sample). The Power State control determines the power state of the Si3054 (Power states for the Si3054 can also be selected by setting the appropriate bits in NID 2). Si3054 Function Reset, Power States, and GPIO controls (Unsolicited Response verb) are described in more detail in the appropriate functional description section.

Table 36. Controls Supported in the Si3054

Verb Type	Verb Name	Encoding	Node Name	NID	Default
Control	Get Converter Format	Ah	Modem FnGrp	1	0x0020
	Set Converter Format	2h	Modem FnGrp	1	
	Get Power State	F05h	Modem FnGrp	1	0x0101
	Set Power State	705h	Modem FnGrp	1	
	Function Reset	7FFH	Modem FnGrp	1	
	Read Node	9h	Widget Nodes	2–39	
	Write Node	1h	Widget Nodes	2–39	
	Get Subsystem ID	F20h	Modem FnGrp	1	
Unsolicited Response	Get Unsolicited Response	F08h	Modem FnGrp	1	0x0000
	Set Unsolicited Response	708h	Modem FnGrp	1	

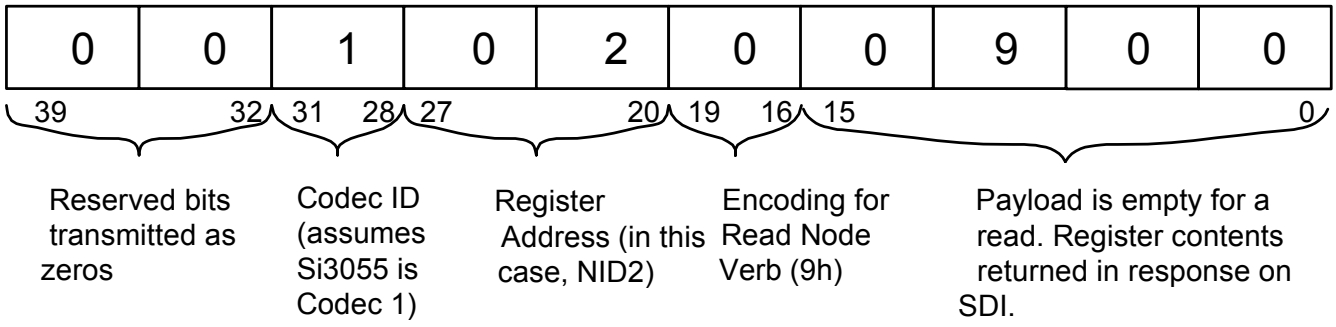


Figure 44. Si3054 Read Node Verb Encoding Example

8.11.1. Subordinate Node Count

The Subordinate Node Count parameter provides information to the bus driver about nodes associated with the Si3054. When the parameter verb is called with NID 0 (root node) as the starting node number, the response returns 0x00010001, indicating that only one function group exists in the Si3054. When the parameter verb is called with NID 1 (the modem function group), the response returns 0x00020026 indicating the number of subordinate nodes in the Si3054.

8.11.2. Node Read/Write

The read/write control verb enables direct access to the subordinate nodes within the Si3054. The verb ID is defined in Table 36. The read (9h) or write (1h) encoding is set in bits (19:16) of the command field (See Figure). The register value is sent in bits 15:0 of the command field or response field for a write or read, respectively. An example of the correct encoding to read an Si3054 register is presented in Figure 44.

8.11.3. Get Converter Format

The Converter Format control determines the format of the Si3054 data. This verb sets the link sample rate and the number of bits per sample (the Si3054 supports either 16 or 24 bit data). Refer to "8.8.Sample Rates," on page 46 for details regarding the selection of modem and link sample rates for the Si3054.

8.12. HD Audio Power States

Power management of the Si3054 can be accomplished with the either the power state verb or through direct manipulation of power control bits in NID 2. In order to ensure proper power control, only one of these methods should be utilized by the modem function driver (both should not be used concurrently). The four power states supported by the Si3054, along with a map of the NID 2 power control bits to the Power State verb PowerState field, are presented in Table 37. Bits [7:2] in the PowerState field are reserved (all zeros).

Table 37. Si3054 Power States

Power State [1:0]	Name	PRD (DAC)	PRC (ADC)	PRA (GPIO)	AZLNK	PDL	System Side	Line Side	W-on-R	Description
00	D0init (D0)	X	X	X	0	0	ON	ON	Enabled	Selected by Function Driver
01	D0uninit (D1)	1	1	1	0	1	ON	OFF	Disabled	POR and Link Reset power state, selected by Function Driver
10	D3hot (D2)	X	X	X	1	0	OFF	ON	Enabled	Ready for sleep mode, selected by Bus Driver
11	D3cold (D3)	1	1	1	1	1	OFF	OFF	Disabled	Ready for sleep mode, selected by Bus Driver

9. PnP EPROM Interface

The AC ’97 or HD Audio codec(s) on a Communication Networks Riser (CNR) card or Mobile Daughter Card (MDC) are attached to the system board chipset and enumerated as a PCI bus device. As such, the codec and CNR/MDC combination should present a unique PCI subsystem vendor ID (SVID) and subsystem ID (SID) to the system board chipset and BIOS for proper Windows Plug-and-Play (PnP) device driver identification and loading. To implement PnP, SVID and SID registers (four bytes total) are defined and loaded from an external serial EPROM.

The EPROM load sequence reads five data bytes immediately after a cold reset ($\overline{\text{RESET}}$ goes high) and also upon software command (EECS bit, Register 6Ah or NID 19). The first data byte is a header value of 97h. The next 4 bytes are loaded into the registers, SVID (Page 1, Register 62h) and SSID (Page 1, Register 64h). In AC ’97 mode, status is readable in the Register 6Ah EECS and EEOK bit. In HD Audio mode, status is readable by initiating the “Get Parameter” control verb.

The EPROM interface is overlaid on the GPIO_A and GPIO_B pins. GPIO_A drives the serial clock during data reception and drives low when finished. GPIO_A continues to drive low until configured as an output, at which time the serial clock driver is disabled until the next EPROM sequence. The GPIO_B pin is the bidirectional serial data input/output. When the EPROM hardware sequence is not executing, the pin can be used for alternate functions, including programming the EPROM via the AC ’97 slot12 GPIO_A and GPIO_B bits, or via the HD Audio GPIO bits.

To initiate a read sequence without a reset, software strobes the EECS bit high. The read sequence executes and sets the EEOK and EECS bit when the SVID and SID registers are loaded. Strobing EECS bit low during the sequence aborts the read, possibly altering the value of the SVID and SSID registers.

If the EPROM read sequence fails for any reason (e.g., if contention is found on the serial interface indicating the presence of some device other than the EPROM or if the header is invalid indicating the absence of the EPROM), the EEOK status bit will be low when EECS indicates completion of the sequence.

Table 38. AC‘97 and HD Audio Control Register Reference Table

Register or Node Name	HD Audio NID (decimal)	AC'97 Address (hex)	
Extended modem status and control	2	3Eh	Page 0
DAC/ADC rate	3	40h	Page 0
DAC/ADC level	4	46h	Page 0
GPIO pin configuration	5	4Ch	Page 0
GPIO pin polarity & type	6	4Eh	Page 0
GPIO pin sticky	7	50h	Page 0
GPIO pin wake up mask	8	52h	Page 0
GPIO pin Status	9	54h	Page 0
GPI	10	60h	Page 0
Misc. Modem AFE status & control	11	56h	Page 0
Chip ID and revision	12	5Ah	Page 0
Line side configuration 1	13	5Ch	Page 0
Line side status	14	5Eh	Page 0
DC termination	15	62h	Page 2
Line side configuration	16	64h	Page 2
Call progress attenuation	17	68h	Page 2
Spark Quenching control	18	6Eh	Page 2
Misc. feature controls	19	6Ah	Page 0
Ring validation control 1	20	6Ch	Page 0
Ring validation control 2	21	6Eh	Page 0
Reserved	22	6Ch	Page 2
Resistor calibration	32	68h	Page 5
Codec Class/Rev	n/a	60h	Page 1
PCI SVID	n/a	62h	Page 1

10. AC‘97 Mode Control Registers

Note: Any register not listed here is reserved and should not be written. Undefined/unimplemented registers return 0.

Table 39. Register Summary

Register	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
24h	Paging													PG3	PG2	PG1	PG0
3Ch	Extended Modem ID	ID1	ID0													LIN2	LIN1
3Eh	Extended Modem Status & Control					PRD	PRC	PRB	PRA					DAC	ADC	MREF	GPIO
40h	DAC/ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
46h	DAC/ADC Level	Mute				DAC3	DAC2	DAC1		Mute				ADC3	ADC2	ADC1	
4Ch	GPIO Pin Configuration	GC15	GC14	GC13	GC12	GC11	GC10	GC9	GC8	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0
4Eh	GPIO Pin Polarity & Type	GP15	GP14	GP13	GP12	GP11	GP10	GP9			GP6	GP5	GP4	GP3	GP2	GP1	GP0
50h	GPIO Pin Sticky	GS15	GS14	GS13		GS11		GS9			GS6	GS5	GS4	GS3		GS1	
52h	GPIO Pin Wake Up Mask	GW15	GW14	GW13		GW11		GW9			GW6	GW5	GW4	GW3		GW1	
54h	GPIO Pin Status	GI15	GI14	GI13	GI12	GI11	GI10	GI9	GI8	GI7	GI6	GI5	GI4	GI3	GI2	GI1	GI0
56h	Miscellaneous Modem AFE Status & Control				MLNK										L1B2	L1B1	L1B0
5Ah	Chip ID & Revision				SID	LSID3	LSID2	LSID1	LSID0	LREV3	LREV2	LREV1	LREV0	SREV3	SREV2	SREV1	SREV0
5Ch	Line Side Configuration 1	ARM1[1]	ARM0[1]	ATM1[1]	ATM0[1]	IIRE		RFWE	ACT2	OHS	BTE	ACT	DCT1[1]	DCT0[1]	RZ		RT
5Eh	Line Side Status	OPE	DODM	ROVM	BTDM	OPD	DOD	ROV	BTD	LCS0	FDT	LCS4	LCS3	LCS2	LCS1	RDTP	RDTN
62h	Line Side Configuration 2								DIAL[1]	FJM[1]	VOL1[1]	VOL0[1]					
64h	Line Side Configuration 3													OVL			
6Ah	Misc Feature Controls	PWME			RNGG	PWMM1	PWMM0	WDTEN								EECS	EEOK
6Ch	Ring Validation Control 1	RNGV	RDLY2	RDLY1	RDLY0	RCC2	RCC1	RCC0									
6Eh	Ring Validation Control 2	RMX5	RMX4	RMX3	RMX2	RMX1	RMX0	RTO3	RTO2	RTO1	RTO0	RAS5	RAS4	RAS3	RAS2	RAS1	RAS0
7Ch	Vendor ID	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0
7Eh	Vendor ID	T7	T6	T5	T4	T3	T2	T1	T0	PID2	PID1	PID0					

Note: All register bits are available when MAP = 0 and MAP = 1 except
1. Only available when MAP = 0
2. Only available when MAP = 1

Table 40. Extended Register Pages Summary

Register	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Page 1: PnP ID Registers 60h–64h																	
60h	Codec Class/ Rev					CL3	CL2	CL1	CL0	RV7	RV6	RV5	RV4	RV3	RV2	RV1	RV0
62h	PCI Subsystem Vendor ID	PVI15	PVI14	PVI13	PVI12	PVI11	PVI10	PVI9	PVI8	PVI7	PVI6	PVI5	PVI4	PVI3	PVI2	PVI1	PVI0
64h	PCI Subsystem ID	PI15	PI14	PI13	PI12	PI11	PI10	PI9	PI8	PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0
Page 2: Enhanced DAA Control Registers 60h–6Eh																	
60h	Register Map	MAP															
62h	DC Termination							DCV1[2]	DCV0[2]			MINI1[2]	MINI0[2]			ILIM[2]	DCR[2]
64h	Line-Side Configuration	CALZ	MCAL	CALD		FOH1	FOH0	OHS2						OVL			
66h	Reserved																
68h	Call Progress Attenuation	ARM7[2]	ARM6[2]	ARM5[2]	ARM4[2]	ARM3[2]	ARM2[2]	ARM1[2]	ARM0[2]	ATM7[2]	ATM6[2]	ATM5[2]	ATM4[2]	ATM3[2]	ATM2[2]	ATM1[2]	ATM0[2]
6Ah–6Ch	Reserved																
6Eh	Spark Quenching Control		SQ1		SQ0		RG1										
Page 3: Reserved Registers 60h–66h																	
60h–66h	Reserved																
Page 4: Reserved Registers 60h–68h																	
60h–68h	Reserved																
Page 5: Test Register 68h																	
68h	Resistor Calibration			RCALD													

Note: All register bits are available when MAP = 0 and MAP = 1 except
1. only available when MAP = 0
2. only available when MAP = 1

Register 24h. Paging

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name													PG3	PG2	PG1	PG0
Type													R/W	R/W	R/W	R/W

Reset settings = 0x0000

Bit	Name	Function
15:4	Reserved	Read returns zero.
3:0	PG[3:0]	**Register Page.** Changes the definition of registers 60h to 6Eh as follows: 000 = Standard AC97 registers. 001 = Plug-n-Play ID registers. 010 = Enhanced DAA control registers. 011 = Hybrid registers. 100 = Reserved. 101 = Calibration and test registers. 110 = Reserved. 111 = Reserved.

Register 3Ch. Extended Modem ID

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	ID1	ID0													LIN2	LIN1
Type	R	R													R	R

Reset settings = 0x4001

Bit	Name	Function
15:14	ID1:0	**Codec Configuration** These bits indicate the codec configuration: 00 = Primary 01 = Secondary device #2 10 = Secondary device #1 11 = Factory test For Si3054 Revision E and later devices, these bits are fixed to “01”.
13:2	Reserved	Read returns zero.
1:0	LIN2, LIN1	**Line configuration** These bits indicate the slot in the audio output frame used to transfer codec data: 01 = codec data transferred in slot 5. 10 = codec data transferred in slot 10. For Si3054 Revision E and later devices, these bits are fixed to “01”.

Register 3Eh. Extended Modem Status and Control

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name					PRD	PRC	PRB	PRA					DAC	ADC	MREF	GPIO
Type					R/W	R/W	R/W	R/W					R	R	R	R

Reset settings = 0xFF00

Bits 7–0 are read only, 1 indicates modem AFE subsystem readiness.

Bits 13–8 are read/write and control modem AFE subsystem powerdown.

Note: When bits 13–8 are all set to 1, the Si3018 is powered down.

Bit	Name	Function
15:12	Reserved	Read returns one.
11	PRD	PRD = 1 indicates Modem Line 1 DAC off.
10	PRC	PRC = 1 indicates Modem Line 1 ADC off.
9	PRB	Reserved for future use.
8	PRA	PRA = 1 indicates GPIO powerdown.
7:4	Reserved	Read returns one.
3	DAC	DAC = 1 indicates Modem DAC ready.
2	ADC	ADC = 1 indicates Modem ADC ready.
1	MREF	MREF = 1 indicates Modem V_{REF} is up to nominal level.
0	GPIO	GPIO = 1 indicates GPIO ready.

Register 40h. Line DAC/ADC Rate

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0x0000

Each DAC/ADC pair is governed by a read/write modem sample rate control register that contains a 16-bit unsigned value between 0 and 65535, representing the rate of operation in Hz. A number written over 3800h causes the sample rate to be 16000 Hz. For all rates, if the value written to the register is supported, that value is echoed back when read, otherwise the closest rate supported is returned.

When set to zero, the internal PLL is disabled. The PLL should be programmed before the line side (Si3018) is activated via clearing any PR bit in Register 3Eh. Furthermore, sleep mode is not supported when the PLL is disabled.

Sample Rate	D15–D0
7200	1C20
8000	1F40
8228.57 (57600/7)	2024
8400	20D0
9000	2328
9600	2580
10285.71 (72000/7)	282D
12000	2EE0
13714.28 (96000/7)	3592
16000	3E80

Register 46h. Line 1 DAC/ADC Level

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	Mute				DAC3	DAC2	DAC1		Mute				ADC3	ADC2	ADC1	
Type	R/W				R/W	R/W	R/W		R/W				R/W	R/W	R/W	

Reset setting for Line 1 device = 0x8080

This read/write register controls the modem AFE DAC and ADC levels. The default value after cold register reset for this register (0x8080) corresponds to 0 dB DAC attenuation with mute on and 0 dB ADC gain with mute on.

Bit	Name	Function
15	Mute	**Transmit Mute.** 0 = mute off. 1 = mute on.
14:12	Reserved	Read returns zero.
11:9	DAC[3:1]	**Analog Transmit Attenuation.** 000 = 0 db attenuation. 001 = 3 db attenuation. 010 = 6 db attenuation. 011 = 9 db attenuation. 1xx = 12 db attenuation.
8	Reserved	Read returns zero.
7	Mute	**Receive Mute.** 0 = mute off. 1 = mute on.
6:4	Reserved	Read returns zero.
3:1	ADC[3:1]	**Analog Receive Gain.** 000 = 0 db gain. 001 = 3 db gain. 010 = 6 db gain. 011 = 9 db gain. 1xx = 12 db gain.
0	Reserved	Read returns zero.

Register 4Ch. GPIO Pin Configuration

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	GC15	GC14	GC13	GC12	GC11	GC10	GC9	GC8	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset setting for Line 1 device = 0x00FF

The GPIO Pin Configuration register is read/write for configuring Slot 12 I/O. These pins are digital commands (virtual pins). This register specifies whether a GPIO pin is configured for input (1) or output (0). The digital controller sends the desired GPIO pin value over output slot 12 in the outgoing stream of the AC-link before configuring any of these bits for output.

Register 4Eh. GPIO Pin Polarity and Type

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	GP15	GP14	GP13	GP12	GP11	GP10	GP9			GP6	GP5	GP4	GP3	GP2	GP1	GP0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W			R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0xFFFF

The GPIO Pin Polarity/Type register is read/write for selecting the polarity and type for Slot 12 I/O. This register defines GPIO Input Polarity (0 = low, 1 = high active) when a GPIO pin is configured as an input. It defines GPIO output type (0 = CMOS, 1 = OPEN-DRAIN) when a GPIO pin is configured as an output. The default value after soft reset (0xFFFF) is all pins active high. Non-implemented GPIO pins always return 1s.

Note: Register 4Eh is not effected by a cold or warm reset. (This is to avoid corrupting Sticky bits.)

Register 50h. GPIO Pin Sticky

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	GS15	GS14	GS13		GS11		GS9			GS6	GS5	GS4	GS3		GS1	
Type	R/W	R/W	R/W		R/W		R/W			R/W	R/W	R/W	R/W		R/W	

Reset settings = 0x0000

The GPIO Pin Sticky is a read/write register. It defines the GPIO input type (0 = Non-Sticky, 1 = Sticky) when a GPIO pin (defined in slot 12 I/O) is configured as an input. Applies to Ring Detect, Delta Loop Current Sense, GPIO_A, and GPIO_B bits.

GPIO inputs configured as Sticky are cleared only by writing a 0 to the corresponding bit of the GPIO Pin Status Register 54h. The default value after cold register reset (0x0000) is all pins Non-Sticky. Unimplemented GPIO pins always return zeros. Sticky is defined as Edge sensitive; Non-Sticky is defined as Level sensitive.

Register 52h. GPIO Pin Wake Up Mask

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	GW15	GW14	GW13		GW11		GW9			GW6	GW5	GW4	GW3		GW1	
Type	R/W	R/W	R/W		R/W		R/W			R/W	R/W	R/W	R/W		R/W	

Reset settings = 0x0000

The GPIO Pin Wake-up is a read/write register that provides a mask for determining whether an input GPIO change will generate a wake-up or GPIO_INT (0 = No, 1 = Yes). When the AC-link is powered down, a wake-up event triggers the assertion of SDATA_IN. When AC-link is powered up, a wake-up event appears as GPIO_INT = 1 on bit 0 of input slot 12. Ring-detection wake-up can be enabled or disabled.

An AC-Link wake-up interrupt is defined as a 0 to 1 transition on SDATA_IN when the AC-link is powered down. GPIO bits that have been programmed as Inputs, Sticky, and Pin Wake-up, upon transition (either high-to-low or low-to-high) depending on pin polarity, cause an AC-Link wake-up event if the AC-Link was powered down.

The default value after cold register reset (0x0000) defaults to all 0s specifying no wake-up event. Applies to Ring Detect, Delta Loop Current Sense, GPIO_A, and GPIO_B bits. Non-implemented GPIO pins always return 0s.

Register 54h. GPIO Pin Status

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	GI15	GI14	GI13	GI12	GI11	GI10	GI9	GI8	GI7	GI6	GI5	GI4	GI3	GI2	GI1	GI0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0x

GPIO Status is a read/write register that reflects the state of all GPIO pins (inputs and outputs) on slot 12. The value of all GPIO pin inputs and outputs comes from each frame on slot 12, but is also available for reading as GPIO Pin Status via the standard slot 1 and 2 command address/data protocols. GPIO inputs configured as Sticky are cleared by writing a 0 to the corresponding bit of this register. (This should be the last event before setting the AC ’97 MLNK bit.)

GPIO bits that have been programmed as Inputs and Sticky, upon transition (high-to-low or low-to-high) cause the individual GI bit to go asserted 1 and remain asserted until a write of 0 to that bit. The only way to set the desired value of a GPIO output pin is to set the control bit in output slot 12.

If configured as an input, the default value after register reset is always the state of the GPIO pin.

Register 56h. Miscellaneous Modem AFE Status and Control

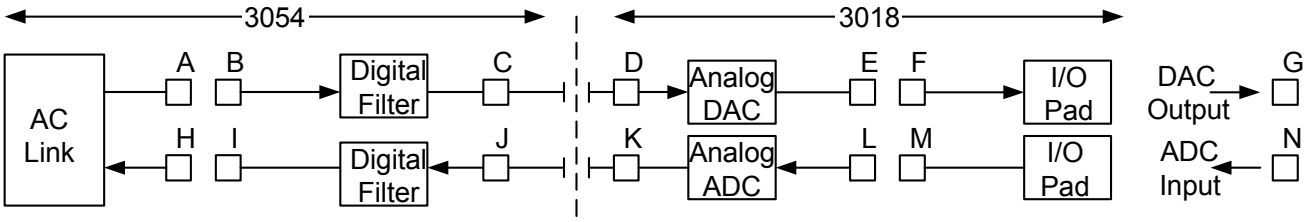
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name				MLNK										L1B2	L1B1	L1B0
Type				R/W										R/W	R/W	R/W

Reset settings = 0x0000

This read/write register defines the loopback modes available for the modem line ADCs/DACs.

The default value after cold register reset (0x000) is all loopbacks disabled.

Bit	Name	Function
15:13	Reserved	Read returns zero.
12	MLNK	Controls an MC'97's AC-link status. 1 sets the MC'97's AC-link to off (sleep), 0 sets the link on (active).
11:3	Reserved	Read returns zero.
2:0	L1B[2:0]	**Line 1 Loopback Modes.** 000 = Disabled (default). 001 = ADC Loopback (I→B). 010 = Local Analog Loopback (F→M). 011 = Digital DAC Loopback (C→J). 100 = Remote Analog Loopback (M→F). 101 = Capacitive Communications Link Loopback (D→K). 110 = External Analog Loopback (G→N). 111 = AC-Link Loopback (A→H).



Note: For all loopback modes except 011, line-side must be powered on and off-hook.

Figure 45. Loopback Points

Register 5Ah. Chip ID and Revision

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name				SID	LSID3	LSID2	LSID1	LSID0	LREV3	LREV2	LREV1	LREV0	SREV3	SREV2	SREV1	SREV0
Type				R	R	R	R	R	R	R	R	R	R	R	R	R

Reset settings = 0x0XXX

Bit	Name	Function
15:13	Reserved	Read returns zero.
12	SID	**System-Side ID.** 0 = Reserved 1 = Si3054 (dual mode device with serial bus autodetection)
11:8	LSID[3:0]	**Line-Side ID.** 0001 = Si3018 global. Other = Reserved.
7:4	LREV[3:0]	**Line-Side Revision.** Four-bit value indicating the revision of the line-side chip.
3:0	SREV[3:0]	**System-Side Revision.** Four-bit value indicating the revision of the system-side chip.

Note: Line side must be activated via PR bits before valid read

.

Register 5Ch. Line-Side Configuration 1

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	ARM1	ARM0	ATM1	ATM0	IIRE		RFWE	ACT2	OHS	BTE	ACT	DCT1	DCT0	RZ		RT
Type	R/W	R/W	R/W	R/W	R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		R/W

Reset settings = 0xF010

Bit	Name	Function
15:14	ARM[1:0]	**Analog (Call Progress) Receive Path Mute (MAP = 0 only).** 00 = 0 dB receive path attenuation for call progress AOUT pin only. 01 = –12 dB receive path attenuation for call progress AOUT pin only. 10 = Mutes receive path for call progress AOUT pin only. 11 = –6 dB receive path attenuation for call progress AOUT pin only.
13:12	ATM[1:0]	**Analog (Call Progress) Transmit Path Mute (MAP = 0 only).** 00 = –20 dB transmit path attenuation for call progress AOUT pin only. 01 = –30 dB transmit path attenuation for call progress AOUT pin only. 10 = Mutes transmit path for call progress AOUT pin only. 11 = –26 dB transmit path attenuation for call progress AOUT pin only.
11	IIRE	**IIR Filter Enable.** 0 = FIR filter selected. 1 = IIR filter selected.
10	Reserved	Read returns zero.
9	RFWE	**Ring Detector Full-Wave Rectifier Enable.** When RNGV is disabled, this bit controls the ring detector mode. When RNGV is enabled, this bit configures the RDT bit to either follow the ringing signal detected by the ring validation circuit, or to follow an unqualified ring detect one-shot signal initiated by a ring-threshold crossing and terminated by a fixed counter timeout of approximately 5 seconds. **RNGV** **RFWE** **RDT bit** 0 0 Half-Wave 0 1 Full-Wave 1 0 Validated Ring Envelope 1 1 Ring Threshold Crossing One-Shot
8	ACT2	**AC Termination Select 2.** Works with the ACT bit to select one of four ac terminations. **ACT2** **ACT** **AC Termination** 0 0 Real, 600 Ω 0 1 Global complex impedance 1 0 Global complex impedance, except New Zealand 1 1 New Zealand complex impedance The global complex impedance satisfies minimum return loss requirements in a country requiring a complex ac termination. The other complex impedances can be used for improved return loss performance.

Bit	Name	Function
7	OHS	**On-Hook Speed.** This bit, in combination with the OHS2 bit and the SQ[1:0] bits, sets the amount of time for the line-side device to go on-hook. The on-hook speeds specified are measured from the time the OH bit is cleared until loop current equals zero. **OHS** **OHS2** **SQ[1:0]** **Mean On-Hook Speed** 0 0 00 Less than 0.5 ms 0 1 00 3 ms ±10% (meets ETSI standard) 1 X 11 26 ms ±10% (meets Australia spark quenching spec)
6	BTE	**Billing Tone Detector Enable.** When set, the DAA can detect a billing tone signal on the line and maintain an off-hook state through the billing tone. If a billing tone is detected, the BTD bit is set to indicate the event. 0 = Billing tone detection disabled. The BDT bit is not functional. 1 = Billing tone detection enabled. The BDT is functional.
5	ACT	**AC Termination Select 1.** When the ACT2 bit is cleared, the ACT bit selects the following: 0 = Selects the real impedance (600 Ω). 1 = Selects the complex impedance.
4:3	DCT[1:0]	**DC Termination Select (MAP = 0 only).** 00 = Low voltage mode (Transmit level = –5 dBm). 01 = Japan mode. Lower voltage mode (Transmit level = –3 dBm). 10 = FCC mode. Standard voltage mode (Transmit level = –1 dBm). 11 = TBR21 mode. Current limiting mode (Transmit level = –1 dBm).
2	RZ	**Ringer Impedance.** 0 = Maximum (high) ringer impedance. 1 = Synthesize ringer impedance. See "6.14.Ringer Impedance and Threshold," on page 30.
1	Reserved	Read returns zero.
0	RT	**Ringer Threshold Select.** Satisfies country requirements on ring detection. Signals below the lower level do not generate a ring detection. Signals above the upper level are guaranteed to generate a ring detection. 0 = 13.5 to 16.5 V_{rms}. 1 = 19.35 to 23.65 V_{rms}.

Register 5Eh. Line-Side Status

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	OPE	DODM	ROVM	BTDM	OPD	DOD	ROV	BTD	LCS0	FDT	LCS4	LCS3	LCS2	LCS1	RDTP	RDTN
Type	R/W	R/W	R/W	R/W	R	R	R/W	R	R	R	R	R	R	R	R	R

Reset setting = 0x0000

Bit	Name	Function
15	OPE	**Overload Protect Enable.** 0 = Disable overload protection. 1 = Enable overload protection. The overload protection feature prevents damage to the DAA when going off-hook with excessive line current or voltage. When off-hook, if OPE is set and LCS = 11111, the dc termination is disabled (800 Ω presented to the line), the hookswitch current is reduced, and the OPD bit is set. The OPE bit should be written ~25 ms after going off-hook; it should be written to 0 to reset.
14	DODM	**Drop Out Detect Interrupt Mask.** 0 = A line supply dropout does not cause a DAA interrupt indication in Slot 12 GPIO 7/8. 1 = A line supply dropout causes a DAA interrupt indication in Slot 12 GPIO 7/8.
13	ROVM	**Receive Overload Interrupt Mask.** 0 = A receive overload does not cause a DAA interrupt indication in Slot 12 GPIO 7/8. 1 = A receive overload causes a DAA interrupt indication in Slot 12 GPIO 7/8.
12	BTDM	**Billing Tone Detect Interrupt Mask.** 0 = A billing tone does not cause a DAA interrupt indication in Slot 12 GPIO 7/8. 1 = A billing tone causes a DAA interrupt indication in Slot 12 GPIO 7/8.
11	OPD	**Overload Protect Detect.** This bit is used to indicate that the DAA has detected a loop current overload. The detector firing threshold depends on the setting of the ILIM bit. **OPD** **ILIM** **Overcurrent Threshold** **Overcurrent Status** 0 0 160 mA No overcurrent condition exists 0 1 60 mA No overcurrent condition exists 1 0 160 mA An overcurrent condition has been detected 1 1 60 mA An overcurrent condition has been detected
10	DOD	**Drop Out Detected.** 0 = Line-side power available. 1 = Line-side power unavailable; reads 1 when off-hook.
9	ROV	**Receive Overload.** Set when the receive input has an excessive input level (i.e., receive pin goes below ground). Cleared by writing a 0 to this location. 0 = Normal receive input level. 1 = Excessive receive input level.

Bit	Name	Function
8	BTD	**Billing Tone Detected.** Set if a billing tone is detected. Clear by clearing BTE. 0 = No billing tone detected. 1 = Billing tone detected.
7	LCS[0]	**Loop Current Sense.** Five-bit value returning the loop current in 3 mA/bit resolution when the DAA is in an off-hook state. 00000 = Indicates the loop current is less than required for normal operation. 00100 = Indicates minimum loop current for normal operation. 11111 = Indicates loop current is >127 mA.
6	FDT	**Frame Detect.** 0 = Indicates the communications link has not established frame lock. 1 = Indicates communications link frame lock is established.
5:2	LCS[3:0]	**Loop Current Sense.** Five-bit value returning the loop current in 3 mA/bit resolution when the DAA is in an off-hook state. 00000 = Indicates the loop current is less than required for normal operation. 00100 = Indicates minimum loop current for normal operation. 11111 = Indicates loop current is >127 mA.
1	RDTP	**Ring Detect Signal Positive.** 0 = No ring signal is occurring. 1 = A positive ring signal is occurring.
0	RDTN	**Ring Detect Signal Negative.** 0 = No ring signal is occurring. 1 = A negative ring signal is occurring.
Note: Line-side must be activated via PR bits before valid read/write.		

Register 62h. Line-Side Configuration 2

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name								DIAL	FJM	VOL1	VOL0					
Type								R/W	R/W	R/W	R/W					

Reset setting = 0x0000

Bit	Name	Function
15:9	Reserved	Read returns zero.
8	DIAL	**DTMF Dialing Mode. (Map = 0 only)** Set during DTMF dialing in TBR21 mode if LVCS[4:0] < 16 decimal. 0 = Normal operation. 1 = Increase headroom for DTMF dialing.
7	FJM	**Force Japan DC Termination Mode. (Map = 0 only)** 0 = Normal Gain. 1 = When DCT[1:0] is set to 10_b (FCC Mode), setting this bit forces Japan dc termination mode while allowing for a transmit level of –1 dBm.
6:5	VOL[1:0]	**Line Voltage Adjust. (Map = 0 only)** When set, this bit adjusts the TIP-RING line voltage. Lowering this voltage improves margin in low voltage countries. Raising this voltage may improve distortion performance. 00 = Normal operation. 01 = –0.125 V. 10 = 0.25 V. 11 = 0.125 V.
4:0	Reserved	Read returns zero.

Register 64h. Line-Side Configuration 3

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name													OVL			
Type	R															

Reset setting = 0x0000

Bit	Name	Function
15:8	Reserved	Read returns zero.
7	Reserved	Read may return zero or one.
6:4	Reserved	Read returns zero.
3	OVL	**Overload Detected.** This bit has the same function as ROV in Register 5E but clears itself after the overload has been removed. See “6.17.Billing Tone Protection and Receive Overload” on page 31. This bit is masked by the off-hook counter and is not affected by the BTE bit. 0 = Normal receive input level. 1 = Excessive receive input level.
2:0	Reserved	Test bits.

Register 6Ah. Miscellaneous Feature Controls

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	PWME			RNGG	PWMM1	PWMM0	WDTEN								EECS	EEOK
Type	R/W			R/W	R/W	R/W	R/W								R/W	R

Reset setting = 0x0000

Bit	Name	Function
15	PWME	**Pulse Width Modulation Enable.** 0 = Call progress PWM AOUT disabled. 1 = Call progress PWM AOUT enabled.
14:13	Reserved	Read returns zero.
12	RNGG	**GPIO Ring Select.** The ring detect signal is represented as a general purpose input and defined in conjunction with RNGV (70[14]) and RFWE (5C[9]), as follows: **RNGV / RNGG / RFWE / Ring Detect GPIO** 0 / 0 / 0 — The ring signal is qualified by passing the half-wave rectified comparator output through a fixed retriggerable one-shot counter. 0 / 0 / 1 — Full-wave rectified unfiltered output of comparators. 0 / 1 / 0 — Half-wave rectified unfiltered output of comparators. 0 / 1 / 1 — Full-wave rectified unfiltered output of comparators. 1 / 0 / x — Fully validated ring. 1 / 1 / 0 — Fully validate ring for wake-up only. After the AC-link is active, the ring signal is qualified by passing the half-wave rectified comparator output through a fixed retriggerable one-shot counter. 1 / 1 / 1 — Fully validate ring for wake-up only. After the AC-link is active, use full-wave rectified unfiltered output of comparators.
11:10	PWMM[1:0]	**Pulse Width Modulation Mode.** Selects the type of signal on the call progress AOUT pin. 00 = PWM output clocked at 16.384 MHz. A local density of 1s and 0s tracks the combined transmit and receive signal. 01 = Conventionally PWM output signal returns to 0 at 32 kHz intervals and rises at a time in the 32 kHz period proportional to the instantaneous amplitude. 10 = Balanced conventional PWM output signal has high and low portions of the modulated pulse centered on the 16 kHz sample clock. 11 = Reserved.
9	WDTEN	**Watchdog Timer Enable.** 0 = Watchdog timer disabled. 1 = Watchdog timer enabled. When set, this bit is cleared only by a hardware reset. The watchdog timer monitors DAA register writers. If a register write does not occur within a 4.096 second window, then the DAA is put into an on-hook state. Only a write of a DAA register restarts the timer.

Bit	Name	Function
8:2	Reserved	Read returns zero.
1	EECS	**EPROM Command Status.** To initiate a serial EPROM read, software strobes EECS high. Strobing the bit low aborts the EPROM read and clears the associated status. The read-back (status) value returns 1 during EPROM read progress and 1 upon completion of the task.
0	EEOK	**EPROM OK.** 0 = EPROM read aborted. 1 = EPROM read successful.

Register 6Ch. Ring Validation Control 1

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RNGV	RDLY2	RDLY1	RDLY0	RCC2	RCC1	RCC0									
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W									

Reset setting = 0x2A00

Bit	Name	Function
15	RNGV	**Ring Validation Enable.** 0 = Ring validation feature is disabled. 1 = Ring validation feature is enabled in normal operating mode and low-power mode.
14:12	RDLY[2:0]	**Ring Delay.** These bits set the amount of time between when a ring signal is validated and when a valid ring signal is indicated. 000 = 0 ms 001 = 256ms 010 = 512 ms . . . 111 = 1792 ms
11:9	RCC[2:0]	**Ring Confirmation Count.** Determine the time interval over which the ring signal must meet tolerances defined by RAS[5:0] and RMX[5:0] to be classified as a valid ring signal. 000 = 100 ms 001 = 150 ms 010 = 200 ms 011 = 256 ms 100 = 384 ms 101 = 512 ms 110 = 640 ms 111 = 1024 ms
8:0	Reserved	Read returns zero.

Register 6Eh. Ring Validation Control 2

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RMX5	RMX4	RMX3	RMX2	RMX1	RMX0	RTO3	RTO2	RTO1	RTO0	RAS5	RAS4	RAS3	RAS2	RAS1	RAS0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset setting = 0x5959

Bit	Name	Function
15:10	RMX[5:0]	**Ring Assertion Maximum Count.** These bits set the maximum ring frequency for a valid ring signal within a 10% margin of error. During ring qualification, a timer is loaded with the RAS[5:0] field upon a TIP/RING event and decrements at a regular rate. When a subsequent TIP/RING event occurs, the timer value is compared to the RMX[5:0] field, and, if it exceeds the value in RMX[5:0], the frequency of the ring is too high and the ring is invalidated. The difference between RAS[5:0] and RMX[5:0] identifies the minimum duration between TIP/RING events to qualify as a ring, in binary-coded increments of 2.0 ms (nominal). A TIP/RING event typically occurs twice per ring tone period. At 20 Hz, TIP/RING events would occur every 1/(2 x 20 Hz) = 25 ms. To calculate the correct RMX[5:0] value for a frequency range [f_min, f_max], the following equation should be used: $$RMX[5:0] \geq RAS[5:0] - \frac{1}{2 \times f\_max \times 2\ ms}, RMX \leq RAS$$ To compensate for error margin and ensure a sufficient ring detection window, it is recommended that the calculated value of RMX[5:0] be incremented by 1.
9:6	RTO[3:0]	**Ring Timeout.** Determine when ringing is finished after the most recent ring threshold crossing. 0000 = Invalid 0001 = 128 x 1 = 128 ms 0010 = 128 x 2 = 256 ms . . . 1111 = 128 x 15 = 1920 ms
5:0	RAS[5:0]	**Ring Assertion Time.** These bits set the minimum ring frequency for a valid ring signal. During ring qualification, a timer is loaded with the RAS[5:0] field upon a TIP/RING event and decrements at a regular rate. If a second or subsequent TIP/RING event occurs after the timer has timed out then the frequency of the ring is too low and the ring is invalidated. The difference between RAS[5:0] and RMX[5:0] identifies the minimum duration between TIP/RING events to qualify as a ring, in binary-coded increments of 2.0 ms (nominal). A TIP/RING event typically occurs twice per ring tone period. At 20 Hz, TIP/RING events would occur every 1/(2 x 20 Hz) = 25 ms. To calculate the correct RAS[5:0] value for a frequency range [f_min, f_max], the following equation should be used: $$RAS[5:0] \geq \frac{1}{2 \times f\_min \times 2\ ms}$$

Register 7Ch and 7Eh. Vendor ID

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0
T7	T6	T5	T4	T3	T2	T1	T0	PID2	PID1	PID0					

Reset settings F[7:0] = 53h

S[7:0] = 49h

T[7:0] = 4Ch

PID[2:0] = 010_b

Remaining Bits = Reserved

These registers are for specific vendor identification. The ID method is Microsoft's Plug and Play Vendor ID code with F7..0 being the first character of that ID, S7..0 being the second character, and T7..0 the third character. These three characters are ASCII encoded. Silicon Laboratories Vendor ID is "SIL" or "53h 49h 4Ch". The PID[2:0] field contains the Silicon Laboratories Part ID ("011_b"), indicating the system-side device is the Si3054. For the Si3024, PID[2:0] = 001_b.

11. AC‘97 Mode Extended Register Pages

11.1. Page 1: PnP ID Registers

Register 60h. Codec Class/Rev

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name					CL3	CL2	CL1	CL0	RV7	RV6	RV5	RV4	RV3	RV2	RV1	RV0
Type					R	R	R	R	R	R	R	R	R	R	R	R

Reset settings = 0xXXXX

Bit	Name	Function
15:12	Reserved	Read returns zero.
11:8	CL[3:0]	**Codec Compatibility Class.** EPROM configurable. 00 = Field not implemented (default).
7:0	RV[7:0]	**Codec Revision.** EPROM configurable. These bits specify a device specific revision identifier. This field should be viewed as a vendor-defined extension to the codec ID. 0000 0011 = Rev C (default).

Register 62h. PCI Subsystem Vendor ID

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	PVI15	PVI14	PVI13	PVI12	PVI11	PVI10	PVI9	PVI8	PVI7	PVI6	PVI5	PVI4	PVI3	PVI2	PVI1	PVI0
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Reset settings = 0xXXXX

Bit	Name	Function
15:0	PVI[15:0]	**PCI Subsystem Vendor ID.** EPROM or resistor ID configurable.

Register 64h. PCI Subsystem ID

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	PI15	PI14	PI13	PI12	PI11	PI10	PI9	PI8	PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Reset settings = 0xXXXX

Bit	Name	Function
15:0	PI[15:0]	**PCI Subsystem ID.** EPROM or resistor ID configurable.

11.2. Page 2: AC'97 Mode Enhanced DAA Control Registers

Register 60h. Register Map

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	MAP															
Type	R/W															

Reset settings = 0x0000

Bit	Name	Function
15	MAP	**Register Map.** 0 = Basic register set (Si3014 compatible) selected. 1 = Enhanced register set selected. **Note:** This bit should be set during initialization only.
14:0	Reserved	Read returns zero.

Register 62h. DC Termination

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name							DCV1	DCV0			MINI1	MINI0			ILIM	DCR
Type							R/W	R/W			R/W	R/W			R/W	R/W

Reset settings = 0x0000

Bit	Name	Function
15:10	Reserved	Read returns zero.
9:8	DCV[1:0]	**TIP/RING Voltage Adjust.** Adjust the voltage on the DCT pin of the line-side device, which affects the TIP/RING voltage on the line. Low voltage countries should use a lower TIP/RING voltage. Raising the TIP/RING voltage improves signal headroom. **DCV[1:0] DCT Pin Voltage** 00 3.1 V 01 3.2 V 10 3.35 V 11 3.5 V
7:6	Reserved	Read returns zero.
5:4	MINI[1:0]	**Minimum Operational Loop Current.** Adjusts the minimum loop current so the DAA can operate. Increasing the minimum operational loop current improves signal headroom at a lower TIP/RING voltage. **MINI[1:0] Min Loop Current** 00 10 mA 01 12 mA 10 14 mA 10 16 mA
3:2	Reserved	Read returns zero.
1	ILIM	**Current Limiting Enable.** 0 = Current limiting mode disabled. 1 = Current limiting mode enabled. Limits loop current to a maximum of 60 mA per the TBR21 standard.
0	DCR	**DC Impedance Selection.** 0 = 50 Ω dc termination is selected. Use this mode for all standard applications. 1 = 800 Ω dc termination is selected.
Note: Function available when MAP = 1.		

Register 64h. Line-Side Configuration

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	CALZ	MCAL	CALD		FOH1	FOH0	OHS2						OVL			
Type	R/W	R/W	R/W		R/W	R/W							R/W			

Reset settings = 0x0400

Bit	Name	Function
15	CALZ	**Clear Calibration.** 0 = Normal operation. 1 = Clear calibration data. This bit must be written back to 0 after being set.
14	MCAL	**Manual Calibration.** 0 = No calibration. 1 = Initiate calibration.
13	CALD	**Auto-Calibration Disable.** 0 = Enable auto-calibration. 1 = Disable auto-calibration.
12	Reserved	Read returns zero.
11:10	FOH[1:0]	**Fast Off-Hook Selection.** Determines the length of the off-hook counter. 00 = 512 ms 01 = 128 ms (default) 10 = 64 ms 11 = 8 ms
9	OHS2	**On-hook Speed 2.** This bit, in combination with the OHS bit and the SQ[1:0] bits, sets the amount of time for the line-side device to go on-hook. The on-hook speeds specified are measured from the time the OH bit is cleared until loop current equals zero. **OHS** **OHS2** **SQ[1:0]** **Mean On-Hook Speed** 0 0 00 Less than 0.5 ms 0 1 00 3 ms ±10% (meets ETSI standard) 1 X 11 26 ms ±10% (meets Australia spark quenching spec)
8:4	Reserved	Read returns zero.
3	OVL	**Overload Detected.** This bit has the same function as the ROV bit but clears itself after the overload is removed. See “Billing Tone Detection” section. This bit is only masked by the off-hook counter only and is not affected by the BTE bit. 0 = Normal receive input level. 1 = Excessive receive input level.
2:0	Reserved	Read returns zero.

Register 66h. Reserved

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name																
Type																

Reset settings = 0x0000

Bit	Name	Function
15:0	Reserved	Read returns zero.

Register 68h. Call Progress Attenuation

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	ARM7	ARM6	ARM5	ARM4	ARM3	ARM2	ARM1	ARM0	ATM7	ATM6	ATM5	ATM4	ATM3	ATM2	ATM1	ATM0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0x0000

Bit	Name	Function
15:8	ARM[7:0]	**AOUT Receive Path Attenuation.** When decremented from the default setting, these bits linearly attenuate the AOUT receive path signal used for call progress monitoring. Setting the bits to 0s mutes the AOUT receive path. Attenuation = ARM[7:0]/64 0111_1111 = +6 dB (gain) 0100_0000 = 0 dB 0010_0000 = –6 dB (attenuation) 0001_0000 = –12 dB . . . 0000_0000 = Mute
7:0	ATM[7:0]	**AOUT Transmit Path Attenuation.** When decremented from the default setting, these bits linearly attenuate the AOUT transmit path signal used for call progress monitoring. Setting the bits to 0s mutes the AOUT transmit path. Attenuation = ATM[7:0]/64 0111_1111 = +6 dB (gain) 0100_0000 = 0 dB 0010_0000 = –6 dB (attenuation) 0001_0000 = –12 dB . . . 0000_0000 = Mute
Note: Function available when MAP = 1.		

Register 6Ah-6Ch. Reserved

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name																
Type																

Reset settings = 0xXXXX

Bit	Name	Function
15:0	Reserved	Read returns zero or one.

Register 6Eh. Spark Quenching Control

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name		SQ1		SQ0		RG1										
Type		R/W		R/W		R/W										

Reset settings = 0x0000

Bit	Name	Function
15	Reserved	Read returns zero or one.
14	SQ1	**Spark Quenching.** This bit, in combination with the OHS bit and the OHS2 bit, sets the amount of time for the line-side device to go on-hook. The on-hook speeds specified are measured from the time the OH bit is cleared until loop current equals zero. **OHS OHS2 SQ[1:0] Mean On-Hook Speed** 0 0 00 Less than 0.5 ms 0 1 00 3 ms±10% (meets ETSI standard) 1 X 11 26 ms ±10% (meets Australia spark quenching spec)
13	Reserved	Read returns zero or one.
12	SQ0	**Spark Quenching.** This bit, in combination with the OHS bit and the OHS2 bit, sets the amount of time for the line-side device to go on-hook. The on-hook speeds specified are measured from the time the OH bit is cleared until loop current equals zero. **OHS OHS2 SQ[1:0] Mean On-Hook Speed** 0 0 00 Less than 0.5 ms 0 1 00 3 ms±10% (meets ETSI standard) 1 X 11 26 ms ±10% (meets Australia spark quenching spec)
11	Reserved	Read returns zero or one.
10	RG1	**Receive Gain 1 (Si3018 Revision E or later).** This bit enables receive path gain adjustment. 0 = No gain applied to hybrid, full scale RX on line = 0 dBm. 1 = 1 dB of gain applied to hybrid, full scale RX on line = –1 dBm.
9:0	Reserved	Read returns zero or one.

11.3. Page 3: AC‘97 Mode Reserved Registers

Register 60h-66h. Reserved

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name																
Type																

Reset settings = 0xXXXX

Bit	Name	Function
15:0	Reserved	Read returns zero or one.

11.4. Page 4: AC'97 Mode Reserved Registers

Registers 60h–68h. Reserved

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name																
Type																

Reset settings = 0xXXXX

Bit	Name	Function
15:0	Reserved	Read returns zero or one.

11.5. Page 5: AC'97 Mode Test Registers

Register 68h. Resistor Calibration

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name			RCALD													
Type			R/W													

Reset settings = 0x0000

Bit	Name	Function
15:14	Reserved	Read returns zero.
13	RCALD	**Resistor Calibration Disable.** 0 = Internal resistor calibration enabled. 1 = Internal resistor calibration disabled.
12:0	Reserved	Read returns zero.

12. HD Audio Mode Control Registers

Note: Any register not listed here is reserved and should not be written. Undefined/unimplemented registers return 0.

Table 41. Register Summary

NID	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
2	Extended Modem Status & Control	1	1	1	1	PRD	PRC	PRB	PRA	AZLNK	PDL			DAC	ADC	MREF	GPIO
3	DAC/ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
4	DAC/ADC Level	DTAG[3:0]				DAC3	DAC2	DAC1	TXM	ATAG[3:0]				ADC3	ADC2	ADC1	RXM
5	GPIO Config							GCO1	GCO0	GCI7	GCI6	GCI5	GCI4	GCI3	GCI2	GCI1	GCI0
6	GPIO Polarity & Type	1	1	1	1	1	1	1	1	GP7	GP6	GP5	1	1	GP2	1	1
7	GPIO Sticky									GSI7	GSI6	GSI5	GSI4	GSI3	GSI2	GSI1	GSI0
8	GPIO Wake Up Mask									GWI7	GWI6	GWI5	GWI4	GWI3	GWI2	GWI1	GWI0
9	GPIO Pin Status				GPO4			GPO1	GPO0	GPI7	GPI6	GPI5	GPI4	GPI3	GPI2	GPI1	GPI0
10	GPIO Control													GPOBD	BPOAD	GOHM	GOH
11	Miscellaneous Modem AFE Status & Control														LB[2:0]		
12	Chip ID & Revision				SID	LSID3	LSID2	LSID1	LSID0	LREV3	LREV2	LREV1	LREV 0	SREV3	SREV2	SREV1	SREV 0
13	Line Side Configuration 1					IIRE		RFWE	ACT2	OHS	BTE	ACT			RZ		RT
14	Line Side Status	OPE	DODM	ROVM	BTDM	OPD	DOD	ROV	BTD	LCS0	FDT	LCS4	LCS3	LCS2	LCS1	RDTP	RDTN
15	DC Termination							DCV1	DCV0			MINI1	MINI0			ILIM	DCR
16	Line-Side Configuration	CALZ	MCAL	CALD		FOH1	FOH0	OHS2						OVL			
17	Call Progress Attenuation	ARM7	ARM6	ARM5	ARM4	ARM3	ARM2	ARM1	ARM0	ATM7	ATM6	ATM5	ATM4	ATM3	ATM2	ATM1	ATM0
18	Spark Quenching Control		SQ1		SQ0		RG1										
19	Misc Feature Controls	PWME			RNGG	PWMM1	PWMM 0	WDTE N								EECS	EEOK
20	Ring Validation Control 1	RNGV	RDLY2	RDLY1	RDLY0	RCC2	RCC1	RCC0									
21	Ring Validation Control 2	RMX5	RMX4	RMX3	RMX2	RMX1	RMX0	RTO3	RTO2	RTO1	RTO0	RAS5	RAS4	RAS3	RAS2	RAS1	RAS0
22–31	Reserved																
32	Register Calibration			RCALD													
33–39	Reserved																

NID 2. Extended Modem Status and Control

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	1	1	1	1	PRD	PRC	PRB	PRA	AZLNK	PDL			DAC	ADC	MREF	GPIO
Type	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W			R	R	R	R

Reset settings = 0xFF40

Bits 5–0 are read only, 1 indicates modem AFE subsystem readiness.

Bits 11–6 are read/write and control modem AFE subsystem powerdown.

Note: When bits 13–8 are all set to 1, the Si3018 is powered down.

Bit	Name	Function
15:12	Reserved	Read returns one.
11	PRD	PRD = 1 indicates Modem DAC off.
10	PRC	PRC = 1 indicates Modem ADC off.
9	PRB	
8	PRA	PRA = 1 indicates GPIO powerdown.
7	AZLNK	AZLNK = 1 sets ready-to-sleep mode.
6	PDL	PDL = 1 sets line-side off (no WOR).
5:4	Reserved	Read returns zero.
3	DAC	DAC = 1 indicates Modem DAC ready.
2	ADC	ADC = 1 indicates Modem ADC ready.
1	MREF	MREF = 1 indicates Modem V_{REF} is up to nominal level.
0	GPIO	GPIO = 1 indicates GPIO ready.

NID 3. Line DAC/ADC Rate

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0x0000

Each DAC/ADC pair is governed by a read/write modem sample rate control register that contains a 16-bit unsigned value between 0 and 65535, representing the rate of operation in Hz. A number written over 3800h causes the sample rate to be 16000 Hz. For all rates, if the value written to the register is supported, that value is echoed back when read; otherwise, the closest rate supported is returned.

Sample rates for Line 1 and Line 2	
Sample Rate	**D15–D0**
7200	1C20
8000	1F40
8228.57 (57600/7)	2024
8400	20D0
9000	2328
9600	2580
10285.71 (72000/7)	282D
12000	2EE0
13714.28 (96000/7)	3592
16000	3E80

NID 4. DAC/ADC Tag and Level

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	DTAG[3:0]				DAC3	DAC2	DAC1	TXM	ATAG[3:0]				ADC3	ADC2	ADC1	RXM
Type	R/W				R/W	R/W	R/W	R/W	R/W				R/W	R/W	R/W	R/W

Reset settings = 0xF1F1

This read/write register controls the modem AFE DAC and ADC levels. The default value after cold register reset for this register (0xF1F1) corresponds to 0 dB DAC attenuation with mute on and 0 dB ADC gain with mute on. The DAC and ADC stream tags should be programmed to the correct IO for the associated HD Audio stream.

Bit	Name	Function
15:12	DTAG[3:0]	**DAC Stream Tag.**
11:9	DAC[3:1]	**Analog Transmit Attenuation.** 000 = 0 db attenuation. 001 = 3 db attenuation. 010 = 6 db attenuation. 011 = 9 db attenuation. 1xx = 12 db attenuation.
8	TXM	**Transmit Mute.** 0 = mute off. 1 = mute on.
7:4	ATAG[3:0]	**ADC Stream Tag.**
3:1	ADC[3:1]	**Analog Receive Gain.** 000 = 0 db gain. 001 = 3 db gain. 010 = 6 db gain. 011 = 9 db gain. 1xx = 12 db gain.
0	RXM	**Receive Mute.** 0 = mute off. 1 = mute on.

NID 5. GPIO Configuration

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name							GC01	GC00	GCI7	GCI6	GCI5	GCI4	GCI3	GCI2	GCI1	GCI0
Type							R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset setting = 0x1FFF

These pins are digital commands (virtual pins). This register specifies whether a GPIO is configured as an input or output (for GCI6 or GCI7) or enabled or disabled (for all other GCI/GCO).

Bit	Name	Function
15:10	Reserved	Read returns zero.
9	GCO1	**CID GPO Configuration.** 0 = output enabled. 1 = disabled.
8	GCO0	**OH GPO Configuration.** 0 = output enabled. 1 = disabled.
7	GCI7	**GPIO_A Configuration.** 0 = output enabled. 1 = input enabled.
6	GCI6	**GPIO_B Configuration.** 0 = output enabled. 1 = input enabled.
5	GCI5	**DAA_INT GPI Enable.** 0 = disabled. 1 = input enabled.
4	GCI4	**OPD GPI Enable.** 0 = disabled. 1 = input enabled.
3	GCI3	**DLCS GPI Enable.** 0 = disabled. 1 = input enabled.
2	GCI2	**RDT GPI Enable.** 0 = disabled. 1 = input enabled.
1	GCI1	**FDT GPI Enable.** 0 = disabled. 1 = input enabled.
0	GCI0	**GPIO_INT Enable.** 0 = disabled. 1 = input enabled.

NID 6. GPIO Polarity and Type

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	1	1		1	1	1	1	1	GP7	GP6	GP5	1	1	GP2	1	1
Type	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R	R/W	R	R

Reset settings = 0xFFFF

This register defines GPIO Input Polarity (0 = low, 1 = high active) when a GPIO pin is configured as an input. For the physical GPIO pins on the Si3054, this register defines GPIO output type (0 = CMOS, 1 = OPEN-DRAIN) when the pin is configured as an output. The default value after soft reset (0xFFFF) is all pins active high. Non-implemented GPIO pins always return 1s.

Note: NID 6 is not effected by a cold or warm reset. (This is to avoid corrupting Sticky bits that are intended to report wake events after the PC resumes from a suspended state.)

Bit	Name	Function
15:14	Reserved	Read returns one.
13	Reserved	Read returns zero or one.
12:8	Reserved	Read returns one.
7	GP7	**GPIO_A Polarity or Type.** If GPIO_A is an input, this bit defines GPIO polarity: 0 = active low. 1 = active high. If GPIO_A is an output, this bit defines GPIO type: 0 = CMOS. 1 = OPEN-DRAIN.
6	GP6	**GPIO_B Polarity or Type.** If GPIO_B is an input, this bit defines GPIO polarity: 0 = active low. 1 = active high. If GPIO_B is an output, this bit defines GPIO type: 0 = CMOS. 1 = OPEN-DRAIN.
5	GP5	**DAA_INT GPI Polarity.** 0 = low. 1 = active high.
4:3	Reserved	Read returns one.
2	GP2	**RDT GPI Polarity.** 0 = disabled. 1 = input enabled.
1:0	Reserved	Read returns one.

NID 7. GPIO Sticky

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name									GSI7	GSI6	GSI5	GSI4	GSI3	GSI2	GSI1	GSI0
Type									R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

Reset settings = 0x0000

The GPIO Sticky is a read/write register that defines the GPIO input type (0 = non-sticky, 1 = sticky) when a GPIO is configured as an input.

GPIO inputs configured as sticky are cleared only by writing a 0 to the corresponding bit of the GPIO Status Register. The default value after cold register reset (0x0000) is all pins non-sticky. Unimplemented GPIO always returns zeros. Sticky is defined as edge sensitive; Non-sticky is defined as level sensitive.

Bit	Name	Function
15:8	Reserved	Read returns zero.
7	GSI7	**GPIO_A Sticky (when configured as an input).** 0 = non-sticky. 1 = sticky.
6	GSI6	**GPIO_B Sticky (when configured as an input).** 0 = non-sticky. 1 = sticky.
5	GSI5	**DAA_INT GPI Sticky.** 0 = non-sticky. 1 = sticky.
4	GSI4	**OPD GPI Sticky.** 0 = non-sticky. 1 = sticky.
3	GSI3	**DLCS GPI Sticky.** 0 = non-sticky. 1 = sticky.
2	GSI2	**RDT GPI Sticky.** 0 = non-sticky. 1 = sticky.
1	GSI1	**FDT GPI Sticky.** 0 = non-sticky. 1 = sticky.
0	GSI0	**GPIO_INT GPI Sticky.** This GPI is automatically configured as sticky if any of GPIs 7:1 are sticky.

NID 8. GPIO Wake Up Mask

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name									GWI7	GWI6	GWI5	GWI4	GWI3	GWI2	GWI1	GWI0
Type									R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0x0000

The GPIO Wake-up is a read/write register that provides a mask for determining whether an input GPIO change generates a wake-up or GPIO_INT (0 = No, 1 = Yes). When the HD Audio bus is powered down, a wake-up event triggers an unsolicited response. When AC-link is powered up, a wake-up event appears as GPIO_INT = 1. Ring-detection wake-up can be enabled or disabled.

GPIO bits that have been programmed as Inputs, Sticky, and Pin Wake-up trigger an unsolicited response on the HD Audio link upon transition (either high-to-low or low-to-high depending on pin polarity).

The default value after cold register reset (0x0000) defaults to all 0s specifying no wake-up event. Applies to Ring Detect, Delta Loop Current Sense, GPIO_A, and GPIO_B bits. Non-implemented GPIO pins always return 0s.

Bit	Name	Function
15:8	Reserved	Read returns zero.
7	GWI7	**GPIO_A Wake-up Mask.** 0 = GPIO change does not generate a wake-up GPIO_INT. 1 = GPIO change generates a wake-up/GPIO_INT.
6	GWI6	**GPIO_B Sticky Wake-up Mask.** 0 = GPIO change does not generate a wake-up/ GPIO_INT. 1 = GPIO change generates a wake-up/GPIO_INT.
5	GWI5	**DAA_INT GPI Wake-up Mask.** 0 = GPIchangedoesnotgenerateawake-up/GPIO_INT. 1 = GPI change generates a wake-up/GPIO_INT.
4	GWI4	**OPD GPI Wake-up Mask.** 0 = GPIchangedoesnotgenerateawake-up/GPIO_INT. 1 = GPI change generates a wake-up/GPIO_INT.
3	GWI3	**DLCS GPI Wake-up Mask.** 0 = GPIchangedoesnotgenerateawake-up/GPIO_INT. 1 = GPI change generates a wake-up/GPIO_INT.
2	GWI2	**RDT GPI Wake-up Mask.** 0 = GPIchangedoesnotgenerateawake-up/GPIO_INT. 1 = GPI change generates a wake-up/GPIO_INT.
1	GWI1	**FDT GPI Wake-up Mask.** 0 = GPIchangedoesnotgenerateawake-up/GPIO_INT. 1 = GPI change generates a wake-up/GPIO_INT.
0	GWI0	**GPIO_INT GPI Wake-up Mask.** 0 = GPIchangedoesnotgenerateawake-up/GPIO_INT. 1 = GPI change generates a wake-up/GPIO_INT.

NID 9. GPIO Pin Status

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name				GPO4			GPO1	GPO0	GPI7	GPI6	GPI5	GPI4	GPI3	GPI2	GPI1	GPI0
Type	R						R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0x0000

GPIO Status is a read/write register that reflects the state of all GPIO pins (inputs and outputs). GPIO inputs configured as Sticky are cleared by writing a 0 to the corresponding bit of this register. GPI bits that have been programmed as Sticky, upon transition (high-to-low or low-to-high), causes the individual GPI bit to assert as a 1 and remain asserted until a write of 0 to that bit. If configured as an input, the default value after register reset is always the state of the GPIO pin.

Bit	Name	Function
15:13	Reserved	Read returns zero.
12	GPO4	**OPE Status.**
11:10	Reserved	Read returns zero.
9	GPO1	**CID Status.**
8	GPO0	**OH Status.**
7	GPI7	**GPIO_A Status.**
6	GPI6	**GPIO_B Status.**
5	GPI5	**DAA_INT GPIO Status.** This GPIO is asserted to 1 if any DAA interrupts in NID 14 are enabled and asserted to 1. These interrupts include DOD, ROV, and BTD.
4	GPI4	**OPD GPIO Status.** This GPIO is asserted to 1if the OPD bit in NID 14 is asserted to 1.
3	GPI3	**DLCS GPIO Status.** This GPIO is asserted to 1if the LCS bits in NID 14 change value.
2	GPI2	**RDT GPIO Status.** This GPIO is asserted to 1if the ring detect bits in NID 14 are asserted to 1.
1	GPI1	**FDT GPIO Status.** This GPIO is asserted to 1if the FDT bit in NID 14 is asserted to 1.
0	GPI0	**GPIO_INT Status.** This GPIO is asserted to 1 if any of GPIOs [7:1] are asserted to 1.

NID 10. GPIO Control

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name													GPOBD	GPOAD	CID	OH
Type													R/W	R/W	R/W	R/W

Reset settings = 0x0000

Bit	Name	Function
15:4	Reserved	Read returns zero.
3	GPOBD	
2	GPOAD	
1	CID	Caller ID 0 = Caller ID data reception disabled. 1 = Caller ID data reception enabled.
0	OH	Off Hook. 0 = Line-side device on-hook. 1 = Cause the line-side device to go off-hook

NID 11. Miscellaneous Modem AFE Status and Control

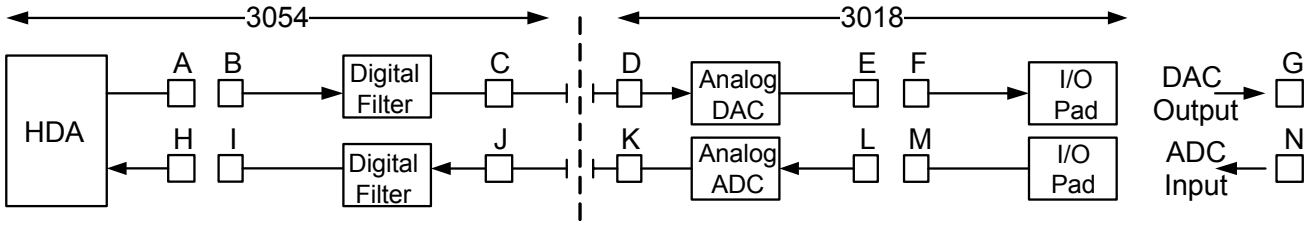
Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name														LB2	LB1	LB0
Type														R/W	R/W	R/W

Reset settings = 0x0000

This read/write register defines the loopback modes available for the modem line ADCs/DACs.

The default value after cold register reset (0x000) is all loopbacks disabled.

Bit	Name	Function
15:3	Reserved	Read returns zero.
2:0	LB[2:0]	**Loopback Modes.** 000 = Disabled (default). 001 = ADC Loopback (I→B). 010 = Local Analog Loopback (F→M). 011 = Digital DAC Loopback (C→J). 100 = Remote Analog Loopback (M→F). 101 = Capacitive Communications Link Loopback (D→K). 110 = External Analog Loopback (G→N). 111 = High Definition Audio Loopback (A→H).



Note: For all loopback modes except 011, line-side must be powered on and off-hook.

Figure 46. Loopback Points

NID 12. Chip ID and Revision

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name				SID	LSID3	LSID2	LSID1	LSID0	LREV3	LREV2	LREV1	LREV0	SREV3	SREV2	SREV1	SREV0
Type				R	R	R	R	R	R	R	R	R	R	R	R	R

Reset settings = 0x1007

Bit	Name	Function
15:13	Reserved	Read returns zero.
12	SID	**System-Side ID.** 0 = Reserved 1 = Si3054 (dual-mode device with serial bus autodetection).
11:8	LSID[3:0]	**Line-Side ID.** 0001 = Si3018 global. Other = Reserved.
7:4	LREV[3:0]	**Line-Side Revision.** Four-bit value indicating the revision of the line-side chip.
3:0	SREV[3:0]	**System-Side Revision.** Four-bit value indicating the revision of the system-side chip.

Note: Line side must be activated via PDL bits before valid read

NID 13. Line-Side Configuration 1

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name					IIRE		RFWE	ACT2	OHS	BTE	ACT			RZ		RT
Type					R/W		R/W	R/W	R/W	R/W	R/W			R/W		R/W

Reset settings = 0x0000

Bit	Name	Function
15:12	Reserved	Read returns zero.
11	IIRE	**IIR Filter Enable.** 0 = FIR filter selected. 1 = IIR filter selected.
10	Reserved	Read returns zero.
9	RFWE	**Ring Detector Full-Wave Rectifier Enable.** When RNGV is disabled, this bit controls the ring detector mode. When RNGV is enabled, this bit configures the RDT bit to either follow the ringing signal detected by the ring validation circuit, or to follow an unqualified ring detect one-shot signal initiated by a ring-threshold crossing and terminated by a fixed counter timeout of approximately 5 seconds. **RNGV** **RFWE** **RDT bit** 0 0 Half-Wave 0 1 Full-Wave 1 0 Validated Ring Envelope 1 1 Ring Threshold Crossing One-Shot
8	ACT2	**AC Termination Select 2.** Works with the ACT bit to select one of four ac terminations. **ACT2** **ACT** **AC Termination** 0 0 Real, 600 Ω 0 1 Global complex impedance 1 0 Global complex impedance, except New Zealand 1 1 New Zealand complex impedance The global complex impedance satisfies minimum return loss requirements in a country requiring a complex ac termination. The other complex impedances can be used for improved return loss performance.
7	OHS	**On-Hook Speed.** This bit, in combination with the OHS2 bit and the SQ[1:0] bits, sets the amount of time for the line-side device to go on-hook. The on-hook speeds specified are measured from the time the OH bit is cleared until loop current equals zero. **OHS** **OHS2** **SQ[1:0]** **Mean On-Hook Speed** 0 0 00 Less than 0.5 ms 0 1 00 3 ms ±10% (meets ETSI standard) 1 X 11 26 ms ±10% (meets Australia spark quenching spec)

Bit	Name	Function
6	BTE	**Billing Tone Detector Enable.** When set, the DAA can detect a billing tone signal on the line and maintain an off-hook state through the billing tone. If a billing tone is detected, the BTD bit is set to indicate the event. Writing this bit to zero clears the BTD bit. 0 = Billing tone detection disabled. The BDT bit is not functional. 1 = Billing tone detection enabled. The BDT is functional.
5	ACT	**AC Termination Select 1.** When the ACT2 bit is cleared, the ACT bit selects the following: 0 = Selects the real impedance (600 Ω). 1 = Selects the complex impedance.
4:3	Reserved	Read returns zero.
2	RZ	**Ringer Impedance.** 0 = Maximum (high) ringer impedance. 1 = Synthesize ringer impedance. See "6.14.Ringer Impedance and Threshold," on page 30. **Note:** The RZ bit should be cleared during pulse dialing and set after going back on hook.
0	RT	**Ringer Threshold Select.** Satisfies country requirements on ring detection. Signals below the lower level do not generate a ring detection. Signals above the upper level are guaranteed to generate a ring detection. 0 = 13.5 to 16.5 V_{rms}. 1 = 19.35 to 23.65 V_{rms}.
1	Reserved	Read returns zero.

NID 14. Line-Side Status

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	OPE	DODM	ROVM	BTDM	OPD	DOD	ROV	BTD	LCS0	FDT	LCS4	LCS3	LCS2	LCS1	RDTP	RDTN
Type	R/W	R/W	R/W	R/W	R	R	R/W	R	R	R	R	R	R	R	R	R

Reset setting = 0x0000

Bit	Name	Function
15	OPE	**Overload Protect Enable.** 0 = Disabled. 1 = Enabled. The overload protection feature can be used to prevent damage to the DAA when off-hook when excessive line current or voltage is present. When off-hook, if OPE is set and LCS = 11111, the dc termination is disabled (800 Ω presented to the line), the hookswitch current is reduced, and the OPD bit is set. The OPE bit should be written ~25 ms after going off-hook; it should be written to 0 to reset. The OPE bit should always be cleared before going off-hook.
14	DODM	**Drop Out Detect Interrupt Mask.** 0 = A line-side power collapse does not cause a DAA interrupt indication in GPI5. 1 = A line-side power collapse causes a DAA interrupt indication in GPI5.
13	ROVM	**Receive Overload Interrupt Mask.** 0 = A receive overload does not cause a DAA interrupt indication in GPI5. 1 = A receive overload causes a DAA interrupt indication in GPI5.
12	BTDM	**Billing Tone Detect Interrupt Mask.** 0 = A billing tone does not cause a DAA interrupt indication in GPI5. 1 = A billing tone causes a DAA interrupt indication in GPI5.
11	OPD	**Overload Protect Detect.** This bit is used to indicate that the DAA has detected a loop current overload. The detector firing threshold depends on the setting of the ILIM bit. **OPD / ILIM / Overcurrent Threshold / Overcurrent Status** 0 / 0 / 160 mA / No overcurrent condition exists 0 / 1 / 60 mA / No overcurrent condition exists 1 / 0 / 160 mA / An overcurrent condition has been detected 1 / 1 / 60 mA / An overcurrent condition has been detected
10	DOD	**Recal/Dropout Detect.** When the line-side device is off-hook, it is powered from the line itself. This bit reads 1 when loop current is not flowing. For example, if this line-derived power supply collapses, such as when the line is disconnected, this bit is set to 1. Additionally, when on-hook, and the line-side device is enabled, this bit is set to 1. 0 = Normal operation. 1 = Line supply dropout detected when off-hook.

Bit	Name	Function
9	ROV	**Receive Overload.** This bit is set when the receive input has an excessive input level (i.e., receive pin goes below ground). Writing a 0 to this location clears this bit. 0 = Normal receive input level. 1 = Excessive receive input level.
8	BTD	**Billing Tone Detected.** Set if a billing tone is detected. Clear by clearing BTE. 0 = No billing tone detected. 1 = Billing tone detected.
7	LCS[4:0]	**Loop Current Sense.** Five-bit value returning the loop current in 3 mA/bit resolution when the DAA is in an off-hook state. 00000 = Indicates the loop current is less than required for normal operation. 00100 = Indicates minimum loop current for normal operation. 11111 = Indicates loop current is >127 mA, and a current overload may exist.
6	FDT	**Frame Detect.** 0 = Indicates communications link has not established frame lock. 1 = Indicates communications link frame lock is established.
5:2	LCS[4:0]	**Loop Current Sense.** Five-bit value returning the loop current in 3 mA/bit resolution when the DAA is in an off-hook state. 00000 = Indicates the loop current is less than required for normal operation. 00100 = Indicates minimum loop current for normal operation. 11111 = Indicates loop current is >127 mA, and a current overload may exist.
1	RDTP	**Ring Detect Signal Positive.** 0 = No positive ring signal is occurring. 1 = A positive ring signal is occurring.
0	RDTN	**Ring Detect Signal Negative.** 0 = No negative ring signal is occurring. 1 = A negative ring signal is occurring.
Note: Line-side must be activated via PR bits before valid read/write.		

NID 15. DC Termination

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name							DCV1	DCV0			MINI1	MINI0			ILIM	DCR
Type							R/W	R/W			R/W	R/W			R/W	R/W

Reset settings = 0x6000

Bit	Name	Function
15:10	Reserved	Read returns zero or one.
9:8	DCV[1:0]	**TIP/RING Voltage Adjust.** Adjust the voltage on the DCT pin of the line-side device, which affects the TIP/RING voltage on the line. Low voltage countries should use a lower TIP/RING voltage. Raising the TIP/RING voltage improves signal headroom. **DCV[1:0] DCT Pin Voltage** 00 3.1 V 01 3.2 V 10 3.35 V 11 3.5 V
7:6	Reserved	Read returns zero or one.
5:4	MINI[1:0]	**Minimum Operational Loop Current.** Adjusts the minimum loop current so the DAA can operate. Increasing the minimum operational loop current improves signal headroom at a lower TIP/RING voltage. **MINI[1:0] Min Loop Current** 00 10 mA 01 12 mA 10 14 mA 10 16 mA
3:2	Reserved	Read returns zero or one.
1	ILIM	**Current Limiting Enable.** 0 = Current limiting mode disabled. 1 = Current limiting mode enabled. Limits loop current to a maximum of 60 mA per the TBR21 standard.
0	DCR	**DC Impedance Selection.** 0 = 50 Ω dc termination is selected. Use this mode for all standard applications. 1 = 800 Ω dc termination is selected.

NID 16. Line-Side Configuration

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	CALZ	MCAL	CALD		FOH1	FOH0	OHS2						OVL			
Type	R/W	R/W	R/W		R/W	R/W	R/W						R/W			

Reset settings = 0x0400

Bit	Name	Function
15	CALZ	**Clear Calibration.** 0 = Normal operation. 1 = Clear calibration data. This bit must be written back to 0 after being set.
14	MCAL	**Manual ADC Calibration.** 0 = No calibration. 1 = Initiate manual ADC calibration.
13	CALD	**ADC Auto-Calibration Disable.** 0 = Enable auto-calibration. 1 = Disable auto-calibration.
12	Reserved	Read returns zero.
11:10	FOH[1:0]	**Fast Off-Hook Selection.** Determines the length of the off-hook counter. 00 = 512 ms 01 = 128 ms (default) 10 = 64 ms 11 = 8 ms
9	OHS2	**On-hook Speed 2.** This bit, in combination with the OHS bit and the SQ[1:0] bits, sets the amount of time for the line-side device to go on-hook. The on-hook speeds specified are measured from the time the OH bit is cleared until loop current equals zero. **OHS** **OHS2** **SQ[1:0]** **Mean On-Hook Speed** 0 0 00 Less than 0.5 ms 0 1 00 3 ms ±10% (meets ETSI standard) 1 X 11 26 ms ±10% (meets Australia spark quenching spec)
8:4	Reserved	Read returns zero.
3	OVL	**Overload Detected.** This bit has the same function as the ROV bit but clears itself after the overload is removed. See “Billing Tone Detection” section. This bit is only masked by the off-hook counter only and is not affected by the BTE bit. 0 = Normal receive input level. 1 = Excessive receive input level.
2:0	Reserved	Read returns zero.

NID 17. Call Progress Attenuation

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	ARM7	ARM6	ARM5	ARM4	ARM3	ARM2	ARM1	ARM0	ATM7	ATM6	ATM5	ATM4	ATM3	ATM2	ATM1	ATM0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 0x0000

Bit	Name	Function
15:8	ARM[7:0]	**AOUT Receive Path Attenuation.** When decremented from the default setting, these bits linearly attenuate the AOUT receive path signal used for call progress monitoring. Setting the bits to 0s mutes the AOUT receive path. Attenuation = ARM[7:0]/64 0111_1111 = +6 dB (gain) 0100_0000 = 0 dB 0010_0000 = –6 dB (attenuation) 0001_0000 = –12 dB . . . 0000_0000 = Mute
7:0	ATM[7:0]	**AOUT Transmit Path Attenuation.** When decremented from the default setting, these bits linearly attenuate the AOUT transmit path signal used for call progress monitoring. Setting the bits to 0s mutes the AOUT transmit path. Attenuation = ATM[7:0]/64 0111_1111 = +6 dB (gain) 0100_0000 = 0 dB 0010_0000 = –6 dB (attenuation) 0001_0000 = –12 dB . . . 0000_0000 = Mute

NID 18. Spark Quenching Control

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name		SQ1		SQ0		RG1										
Type		R/W		R/W		R/W										

Reset settings = 0x0000

Bit	Name	Function
15	Reserved	Read returns zero or one.
14	SQ1	**Spark Quenching.** This bit, in combination with the OHS bit and the OHS2 bit, sets the amount of time for the line-side device to go on-hook. The on-hook speeds specified are measured from the time the OH bit is cleared until loop current equals zero. **OHS** **OHS2** **SQ[1:0]** **Mean On-Hook Speed** 0 0 00 Less than 0.5 ms 0 1 00 3 ms±10% (meets ETSI standard) 1 X 11 26 ms ±10% (meets Australia spark quenching spec)
13	Reserved	Read returns zero.
12	SQ0	**Spark Quenching.** This bit, in combination with the OHS bit and the OHS2 bit, sets the amount of time for the line-side device to go on-hook. The on-hook speeds specified are measured from the time the OH bit is cleared until loop current equals zero. **OHS** **OHS2** **SQ[1:0]** **Mean On-Hook Speed** 0 0 00 Less than 0.5 ms 0 1 00 3 ms±10% (meets ETSI standard) 1 X 11 26 ms ±10% (meets Australia spark quenching spec)
11	Reserved	Read returns zero.
10	RG1	**Receive Gain 1 (Si3018 Revision E or later).** This bit enables receive path gain adjustment. 0 = No gain applied to hybrid, full scale RX on line = 0 dBm. 1 = 1 dB of gain applied to hybrid, full scale RX on line = –1 dBm.
9:0	Reserved	Read returns zero.

NID 19. Miscellaneous Feature Controls

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	PWME			RNGG	PWMM1	PWMM0	WDTEN								EECS	EEOK
Type	R/W			R/W	R/W	R/W	R/W								R/W	R

Reset setting = 0x0000

Bit	Name	Function
15	PWME	**Pulse Width Modulation Enable.** 0 = Pulse width modulation mode disabled (AOUT). 1 = Enable pulse width modulation mode for the call progress analog output (AOUT). This mode sums the transmit and receive audio paths and presents this as a CMOS digital-level output of PWM data. The circuit in Figure 21 on page 21 should be used.
14:13	Reserved	Read returns zero.
12	RNGG	**GPIO Ring Select.** The ring detect signal is represented as a general purpose input and defined in conjunction with RNGV (NID20, bit 5) and RFWE (NID13, bit 9), as follows: **RNGV / RNGG / RFWE / Ring Detect GPIO** 0 / 0 / 0 — The ring signal is qualified by passing the half-wave rectified comparator output through a fixed retriggerable one-shot counter. 0 / 0 / 1 — Full-wave rectified unfiltered output of comparators. 0 / 1 / 0 — Half-wave rectified unfiltered output of comparators. 0 / 1 / 1 — Full-wave rectified unfiltered output of comparators. 1 / 0 / x — Fully validated ring. 1 / 1 / 0 — Fully validate ring for wake-up only. After the AC-link is active, the ring signal is qualified by passing the half-wave rectified comparator output through a fixed retriggerable one-shot counter. 1 / 1 / 1 — Fully validate ring for wake-up only. After the AC-link is active, use full-wave rectified unfiltered output of comparators.
11:10	PWMM[1:0]	**Pulse Width Modulation Mode.** Selects the type of signal on the call progress AOUT pin. 00 = PWM output clocked at 16.384 MHz. A local density of 1s and 0s tracks the combined transmit and receive signals. 10 = Conventional PWM output signal returns to logic 0 at regular 32 kHz intervals and rises at a time in the 32 kHz period proportional to its instantaneous amplitude. 01 = Balanced conventional PWM output signal has high and low portions of the modulated pulse centered on the 16 kHz sample clock. 11 = Reserved.

Bit	Name	Function
9	WDTEN	**Watchdog Timer Enable.** 0 = Watchdog timer disabled. 1 = Watchdog timer enabled. When set, this bit is cleared only by a hardware reset. The watchdog timer monitors DAA register access. If a register write does not occur within a 4.096 second window, then the DAA is put into an on-hook state. A read or write of a DAA register restarts the timer. If the watchdog timer times out, the OH bit is cleared placing the DAA into an off-hook state. Setting the OH bit places the DAA back into an off-hook state.
8:2	Reserved	Read returns zero.
1	EECS	**EPROM Command Status.** To initiate a serial EPROM read, software strobes EECS high. Strobing the bit low aborts the EPROM read and clears the associated status. The read-back (status) value returns 1 during EPROM read progress and 1 upon completion of the task.
0	EEOK	**EPROM OK.** 0 = EPROM read aborted. 1 = EPROM read successful.

NID 20. Ring Validation Control 1

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RNGV	RDLY2	RDLY1	RDLY0	RCC2	RCC1	RCC0									
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W									

Reset setting = 0x2A00

Bit	Name	Function
15	RNGV	**Ring Validation Enable.** 0 = Ring validation feature is disabled. 1 = Ring validation feature is enabled in normal operating mode and low-power mode.
14:12	RDLY[2:0]	**Ring Delay.** These bits set the amount of time between when a ring signal is validated and when a valid ring signal is indicated. 000 = 0 ms 001 = 256ms 010 = 512 ms . . . 111 = 1792 ms
11:9	RCC[2:0]	**Ring Confirmation Count.** Determine the time interval over which the ring signal must meet tolerances defined by RAS[5:0] and RMX[5:0] to be classified as a valid ring signal. 000 = 100 ms 001 = 150 ms 010 = 200 ms 011 = 256 ms 100 = 384 ms 101 = 512 ms 110 = 640 ms 111 = 1024 ms
8:0	Reserved	Read returns zero.

NID 21. Ring Validation Control 2

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RMX5	RMX4	RMX3	RMX2	RMX1	RMX0	RTO3	RTO2	RTO1	RTO0	RAS5	RAS4	RAS3	RAS2	RAS1	RAS0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset setting = 0x5959

Bit	Name	Function
15:10	RMX[5:0]	**Ring Assertion Maximum Count.** These bits set the maximum ring frequency for a valid ring signal within a 10% margin of error. During ring qualification, a timer is loaded with the RAS[5:0] field upon a TIP/RING event and decrements at a regular rate. When a subsequent TIP/RING event occurs, the timer value is compared to the RMX[5:0] field, and, if it exceeds the value in RMX[5:0], the frequency of the ring is too high and the ring is invalidated. The difference between RAS[5:0] and RMX[5:0] identifies the minimum duration between TIP/RING events to qualify as a ring, in binary-coded increments of 2.0 ms (nominal). A TIP/RING event typically occurs twice per ring tone period. At 20 Hz, TIP/RING events would occur every 1/(2 x 20 Hz) = 25 ms. To calculate the correct RMX[5:0] value for a frequency range [f_min, f_max], the following equation should be used: $$RMX[5:0] \geq RAS[5:0] - \frac{1}{2 \times f\_max \times 2\ ms}, RMX \leq RAS$$ To compensate for error margin and ensure a sufficient ring detection window, it is recommended that the calculated value of RMX[5:0] be incremented by 1.
9:6	RTO[3:0]	**Ring Timeout.** This bit sets when a ring signal is determined to be over after the most recent ring threshold crossing. 0000 = Invalid (do not use this setting) 0001 = 128 x 1 = 128 ms 0010 = 128 x 2 = 256 ms . . . 1111 = 128 x 15 = 1920 ms
5:0	RAS[5:0]	**Ring Assertion Time.** These bits set the minimum ring frequency for a valid ring signal. During ring qualification, a timer is loaded with the RAS[5:0] field upon a TIP/RING event and decrements at a regular rate. If a second or subsequent TIP/RING event occurs after the timer has timed out then the frequency of the ring is too low and the ring is invalidated. The difference between RAS[5:0] and RMX[5:0] identifies the minimum duration between TIP/RING events to qualify as a ring, in binary-coded increments of 2.0 ms (nominal). A TIP/RING event typically occurs twice per ring tone period. At 20 Hz, TIP/RING events would occur every 1/(2 x 20 Hz) = 25 ms. To calculate the correct RAS[5:0] value for a frequency range [f_min, f_max], the following equation should be used: $$RAS[5:0] \geq \frac{1}{2 \times f\_min \times 2\ ms}$$

NIDs 22–31. Reserved

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name																
Type																

Reset settings = 0xXXXX

Bit	Name	Function
15:0	Reserved	Read returns zero or one.

NID 32. Resistor Calibration

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name			RCALD													
Type	R/W															

Reset settings = 0x0807

Bit	Name	Function
15:14	Reserved	Read returns zero.
13	RCALD	**Resistor Calibration Disable.** 0 = Internal resistor calibration enabled. 1 = Internal resistor calibration disabled.
12:0	Reserved	Read returns zero.

NIDs 33–39. Reserved

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name																
Type																

Reset settings = 0xXXXX

Bit	Name	Function
15:0	Reserved	Read returns zero or one.

APPENDIX—UL1950 3RD EDITION

Designs using the Si3054 pass all overcurrent and overvoltage tests for UL1950 3rd Edition compliance with a couple of considerations.

Figure 47 shows the designs that can pass the UL1950 overvoltage tests, as well as electromagnetic emissions. The top schematic of Figure 47 shows the configuration in which the ferrite beads (FB1, FB2) are on the unprotected side of the sidactor (RV1). For this configuration, the current rating of the ferrite beads needs to be 6 A. However, the higher current ferrite beads are less effective in reducing electromagnetic emissions.

The bottom schematic of Figure 47 shows the configuration in which the ferrite beads (FB1, FB2) are on the protected side of the sidactor (RV1). For this design, the ferrite beads can be rated at 200 mA.

In a cost optimized design, it is important to remember that compliance to UL1950 does not always require overvoltage tests. It is best to plan ahead and know which overvoltage tests apply to your system. System-level elements in the construction, such as fire enclosure and spacing requirements, need to be considered during the design stages. Consult with your Professional testing agency during the design of the product to determine which tests apply to your system.

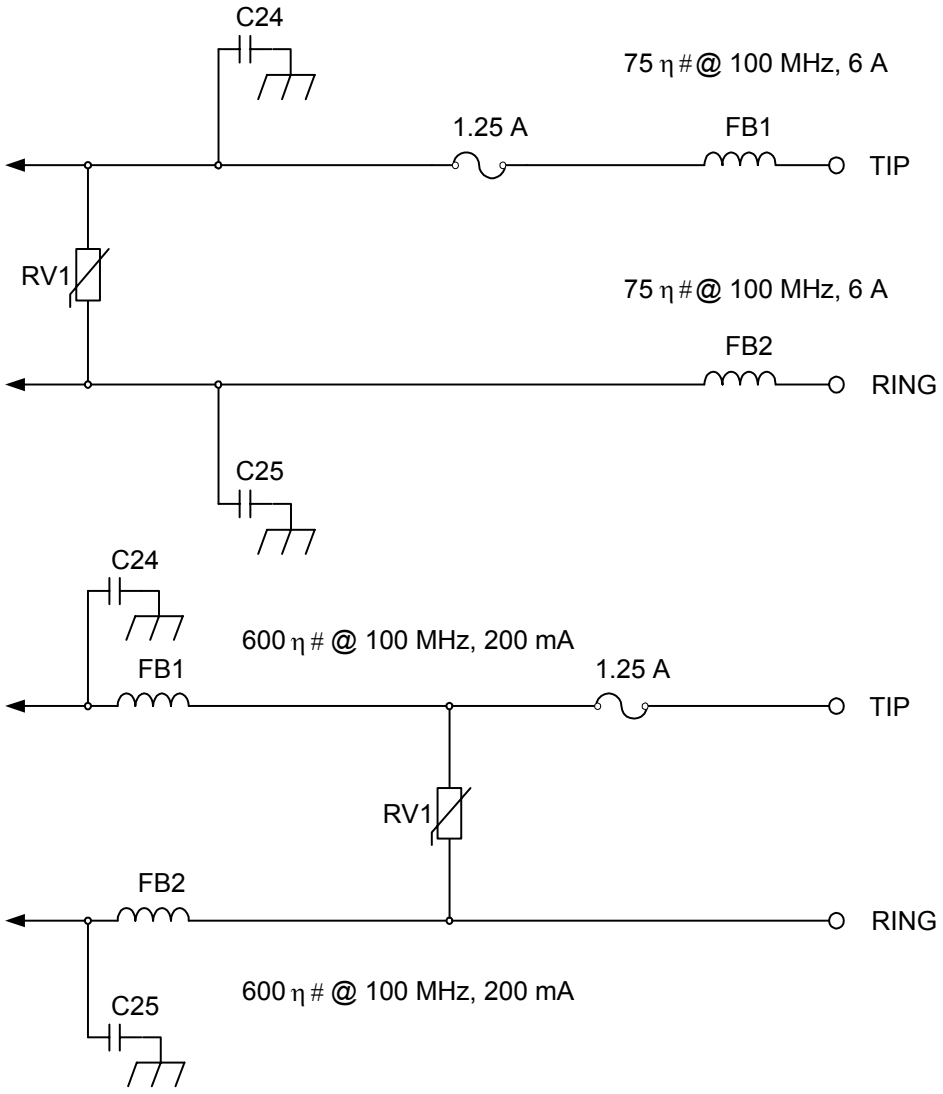


Figure 47. Circuits that Pass all UL1950 Overvoltage Tests

13. Pin Descriptions: Si3054 (Revision E and later)

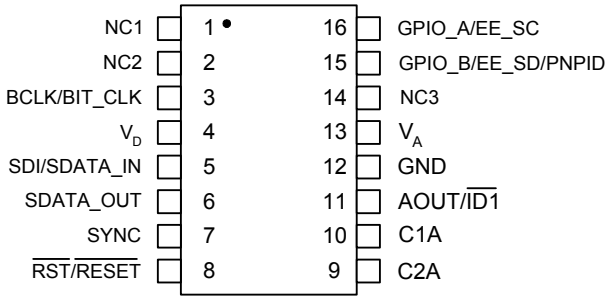


Table 42. Si3054 Pin Descriptions

Pin #	Pin Name	Description
1	NC1	**No Connect.**
2	NC2	**No Connect.**
3	BCLK/BIT_CLK	**Serial Port Clock.** Clock signal generated by a primary codec (AC '97 mode BIT_CLK) or the clock signal generated by the HD Audio controller (BCLK). The clock signal controls the serial data in SDI/SDATA_IN and latches the data on SDO/SDATA_OUT. Controls the serial data on SDATA_IN and latches the data on SDATA_OUT. Output when configured as an AC'97 primary device. Input when configured as a secondary AC'97 device or an HD Audio device.
4	VD	**Digital Power Supply.** Provides the 3.3V digital supply voltage to the Si3054.
5	SDI/SDATA_IN	**Serial Data In.** Serial communication and status data that is provided by the Si3054 to the digital controller.
6	SDO/SDATA_OUT	**Serial Data Out.** Serial communication and control data that is generated by the digital controller and presented as an input to the Si3054.
7	SYNC	**Frame Sync Input.** Data framing signal that is used to indicate the start and stop of a communication data frame.
8	$\overline{\text{RST}}$/$\overline{\text{RESET}}$	**Reset Input.** An active low input that is used to reset all control registers to a defined, initialized state. Also used to bring the Si3054 out of sleep mode.
9	C2A	**Isolation Capacitor 2A Input/Output.** Differential isolation for communication with the DAA line-side device.

Table 42. Si3054 Pin Descriptions

10	C1A	**Isolation Capacitor 1A Input/Output.** Differential isolation for communication with the DAA line-side device.
11	AOUT	**Analog Speaker Output.** Provides an analog output or PWM signal for driving a call progress speaker.
12	GND	**Ground.** Connects to the system digital ground.
13	V_A	**Voltage Regulator.** Connects to an external capacitor to provide bypassing for an internal power supply.
14	NC3	**No Connect.**
15	GPIO_B/EE_SD/PNPID	**General Purpose I/O B.** Programmable via registers 4Ch–54h (AC ‘97 mode), or NIDs 5–10 (HD Audio mode). **EPROM Serial Data.** I/O interface to external serial EPROM. **PnP ID Select Input.** Resistor selection for Plug-n-Play (PnP) identification.
16	GPIO_A/EE_SC	**General Purpose I/O A.** Programmable via registers 4Ch–54h (AC ‘97 mode), or NIDs 5–10 (HD Audio mode). **EPROM Serial Clock.** Output to external serial EPROM.

14. Pin Descriptions: Si3018

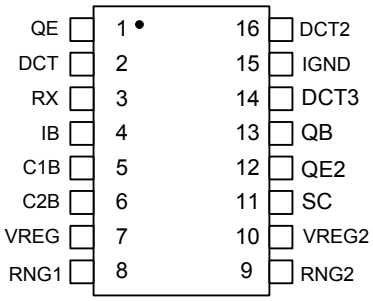


Table 43. Si3018 Pin Descriptions

Pin #	Pin Name	Description
1	QE	**Transistor Emitter.** Connects to the emitter of Q3.
2	DCT	**DC Termination.** Provides dc termination to the telephone network.
3	RX	**Receive Input.** Serves as the receive side input from the telephone network.
4	IB	**Internal Bias 1.** Provides internal bias.
5	C1B	**Isolation Capacitor 1B.** Connects to one side of isolation capacitor C1 and communicates with the Si3054.
6	C2B	**Isolation Capacitor 2B.** Connects to one side of isolation capacitor C2 and communicates with the Si3054.
7	VREG	**Voltage Regulator.** Connects to an external capacitor to provide bypassing for an internal power supply.
8	RNG1	**Ring 1.** Connects through a capacitor to the RING lead of the telephone line. Provides the ring and caller ID signals to the Si3054.
9	RNG2	**Ring 2.** Connects through a capacitor to the TIP lead of the telephone line. Provides the ring and caller ID signals to the Si3054.
10	VREG2	**Voltage Regulator 2.** Connects to an external capacitor to provide bypassing for an internal power supply.
11	SC	**Circuit Enable.** Enables transistor network.
12	QE2	**Transistor Emitter 2.** Connects to the emitter of Q4.
13	QB	**Transistor Base.** Connects to the base of transistor Q3. Used to go on- and off-hook.
14	DCT3	**DC Termination 3.** Provides the dc termination to the telephone network.
15	IGND	**Isolated Ground.** Connects to ground on the line-side interface.
16	DCT2	**DC Termination 2.** Provides dc termination to the telephone network.

15. Ordering Guide[1,2]

Region	Interface	System-Side		Line-Side		Temperature
		Part #	Package	Part #	Package	
Global	PCI	Si3052-KQ	TQFP	Si3018-KS or Si3018-X-FS	SOIC	0 to 70 °C
Global	AC-Link	Si3054-KS or Si3054-D-KS (Revision D)	SOIC	Si3018-KS or Si3018-X-FS	SOIC	0 to 70 °C
Global	Dual Mode AC-Link/HD Audio	Si3054-X-FS (Revision E or later)	SOIC	Si3018-KS or Si3018-X-FS	SOIC	0 to 70 °C

Notes:

1. Many of the above devices are available in lead-free packages. For lead-free parts, the “K” in the part number suffix is replaced with an “F”.
2. An “X” in the ordering part number is a placeholder for the actual device revision. The die revision may not always be included in the ordering part number. Refer to the following Product Identification section for more information on part numbering conventions.

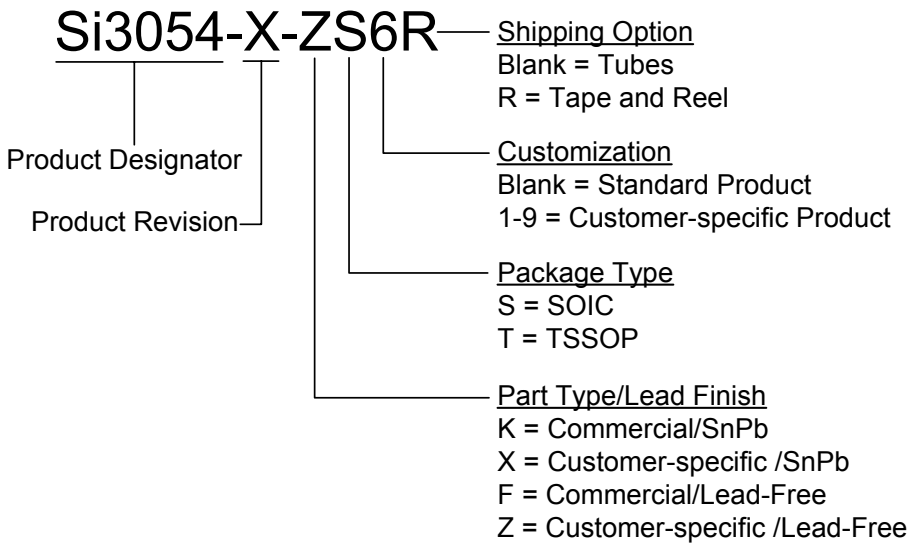
16. Product Selection and Identification Guide

Device	Finished Goods Part Number	Description	Marking
Si3054	Si3054-X-FS	Commercial part, lead-free version	FG Part #
Si3054	Si3054-X-ZS4	Customer-specific bond option, lead-free version	Custom
Si3054	Si3054-X-ZS5	Customer-specific bond option, lead-free version	Custom
Si3054	Si3054-X-ZS6	Customer-specific bond option, lead-free version	Custom
Si3054	Si3054-X-ZS9	Customer-specific bond option, lead-free version	Custom

17. Product Identification

The product identification number is a finished goods part number or is specified by a finished goods part number, such as a special customer part number.

Example:



18. Package Outline: 16-Pin SOIC

Figure 48 illustrates the package details for the Si3054 and Si3018. Table 44 lists the values for the dimensions shown in the illustration.

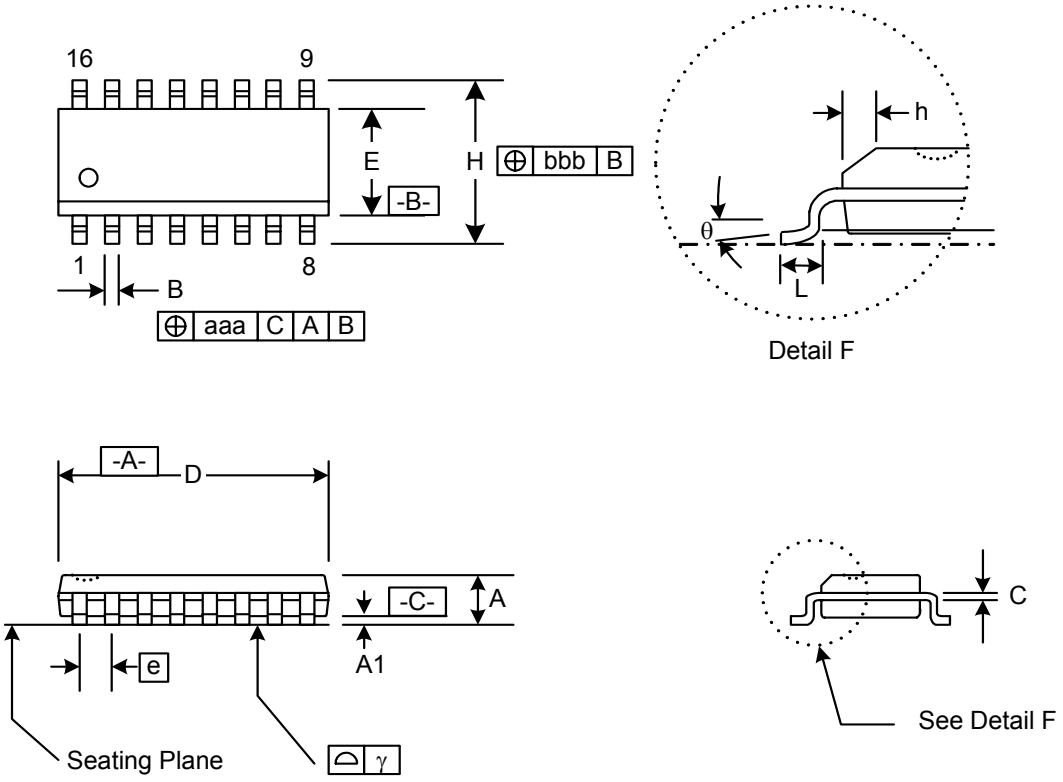


Figure 48. 16-pin Small Outline Integrated Circuit (SOIC) Package

Table 44. Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	1.35	1.75
A1	.10	.25
B	.33	.51
C	.19	.25
D	9.80	10.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	.25	.50
L	.40	1.27
γ	0.10	
θ	0º	8º
aaa	0.25	
bbb	0.25	

19. Package Outline: 16-Pin TSSOP

Figure 49 illustrates the package details for the Si3018. Table 45 lists the values for the dimensions shown in the illustration.

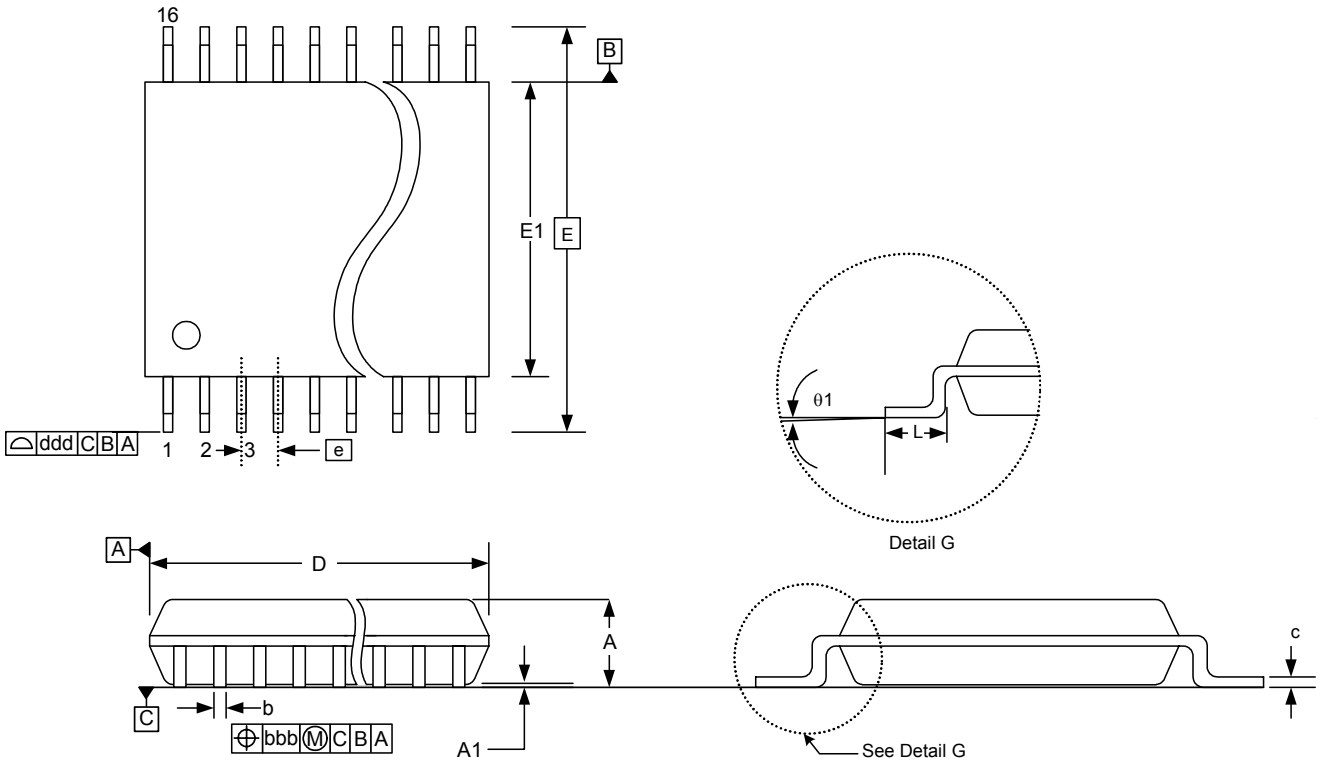


Figure 49. 16-Pin Thin Small Shrink Outline Package (TSSOP)

Table 45. Package Diagram Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	—	—	1.20
A1	0.05	—	0.15
b	0.19	—	0.30
c	0.09	—	0.20
D	4.90	5.00	5.10
e	0.65 BSC		
E	6.40 BSC		
E1	4.30	4.40	4.50
L	0.45	0.60	0.75
θ1	0°	—	8°
bbb	0.10		
ddd	0.20		

Document Change List

Revision 0.89 to Revision 0.9

- The following bits have been added, but are only supported with Si3018 Revision E or later line-side devices.
  - RG1 (Receive Gain 1)
- Updated Tables 3, 5, 8, 12, and 38.
- Updated Figures 11–20.
- Updated “6.7.Off-Hook” functional description.
- Updated “6.9.DC Termination” functional description.
- Updated “6.10.AC Termination” functional description.
- Updated “6.16.Pulse Dialing and Spark Quenching” functional description.
- Updated “6.18.Billing Tone Filter (Optional)” functional description.
- Updated “6.28.Revision Identification” functional description.
- Updated “16.Product Selection and Identification Guide”
- Updated package diagrams.

Revision 0.9 to Revision 0.91

- Updated Register 6E on page page 81
- Updated Figure 29 on page 37.
- Updated Table 5 on page 8.
- Updated Table 8 on page 9.
- Updated Table 10 on page 10.
- Updated Table 12 on page 11.
- Updated Table 14 on page 13.
- Updated Table 19 on page 22.
- Updated Table 35 on page 50.
- Updated Table 40 on page 55.
- Updated Table 41 on page 84.
- Updated Register 3Ch on page 57.
- Updated Register 6Ah on page 71.
- Updated NID 6 “GPIO Polarity and Type” on page 89.
- Updated NID 9 “GPIO Pin Status” on page 92.
- Updated NID 10 “GPIO Control” on page 93.
- Updated NID 12 “Chip ID and Revision” on page 95.
- Updated NID 15 “DC Termination” on page 100.
- Updated NID 18 “Spark Quenching Control” on page 103.
- Updated NID 19 “Miscellaneous Feature Controls” on page 104.
- Updated NID 32 “Register Calibration” on page 108.

Revision 0.91 to Revision 1.0

- Updated Figure 21 on page 21.
- Updated Figure 28 on page 34.
- Updated Table 18 on page 21.
- Updated Table 19 on page 22.
  - Changed recommended country settings for Australia, Bahrain, Bulgaria, China, Croatia, Cyprus, Czech Republic, Egypt, Hungary, Israel, Japan, Jordan, Kazakhstan, Latvia, Lebanon, Malaysia, Malta, Morocco, Nigeria, Oman, Pakistan, Philippines, Poland, Romania, Russia, Slovakia, Slovenia, South Africa, South Korea, Taiwan, Thailand, United Kingdom.
- Updated Table 38 on page 53.
- Updated Table 44 on page 115.
- Changed location of R61 bit in Table 39 and Register 6E description for AC’97 mode.
- Changed location of R61 bit in Table 41 and NID18 register description.
- Updated NID13 register description.
- Updated “Ordering Guide” on page 113.
- Updated “Bill of Materials” on page 18.
  - Changed recommended case size of FB1, FB2.
- Updated "18.Package Outline: 16-Pin SOIC," on page 115.

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