

Si4170DY

RoHS

COMPLIANT

Vishay Siliconix

## N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	$\mathbf{R}_{DS(on)}$ (Ω) $\mathbf{I}_{D}$ (A) <sup>a</sup>		Q <sub>g</sub> (Typ.)	
30	0.0035 at V <sub>GS</sub> = 10 V	30	29 nC	
	0.0045 at $V_{GS}$ = 4.5 V	27	29110	

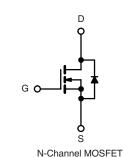
#### **FEATURES**

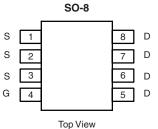
- Halogen-free •
- TrenchFET<sup>®</sup> Power MOSFET
- 100 % R<sub>g</sub> Tested
- 100 % Avalanche Tested ٠

#### **APPLICATIONS**

Notebook PC Core

- Low Side Switch





Ordering Information: Si4170DY-T1-GE3 (Lead (Pb)-free and Halogen-free)

Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V <sub>DS</sub>	30	V	
Gate-Source Voltage		V <sub>GS</sub>	± 20		
Continuous Drain Current (T <sub>J</sub> = 150 °C)	$T_{C} = 25 °C$ $T_{C} = 70 °C$ $T_{A} = 25 °C$ $T_{A} = 70 °C$	I <sub>D</sub>	30 22.8 21.8 <sup>b, c</sup> 17.3 <sup>b, c</sup>	A	
Pulsed Drain Current		I <sub>DM</sub>	70		
Continuous Source-Drain Diode Current	$T_{C} = 25 \text{ °C}$ $T_{A} = 25 \text{ °C}$	I <sub>S</sub>	5.4 2.7 <sup>b, c</sup>		
Single Pulse Avalanche Current         L = 0.1 mH           Single Pulse Avalanche Energy         L = 0.1 mH		I <sub>AS</sub>	40		
		E <sub>AS</sub>	80	mJ	
Maximum Power Dissipation $ \frac{T_{C}}{T_{C}} = \frac{T_{C}}{T_{A}} = \frac$		P <sub>D</sub>	6 3.3 3.0 <sup>b, c</sup> 1.9 <sup>b, c</sup>	w	
Operating Junction and Storage Temperature Ra	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b, d</sup>	t ≤ 10 s	R <sub>thJA</sub>	33	42	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R <sub>thJF</sub>	16	21	0/11

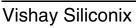
Notes:

a. Based on T<sub>C</sub> = 25 °C.

b. Surface Mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. Maximum under Steady State conditions is 85 °C/W.





Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = 250 \mu\text{A}$	30			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	l <sub>D</sub> = 250 μA		33		mV/°C	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	i <sub>D</sub> = 250 μA		- 6.4			
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = 250 \ \mu A$			2.6	V	
Gate-Source Leakage	I <sub>GSS</sub>				± 100	nA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$			1		
		$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			10	μΑ	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	30			Α	
Drain-Source On-State Resistance <sup>a</sup>		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A		0.0029	0.0035	Ω	
	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A		0.0036	0.0045		
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 15 A		90		S	
Dynamic <sup>b</sup>	1 1			1			
Input Capacitance	C <sub>iss</sub>			4355		pF	
Output Capacitance	C <sub>oss</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz		595			
Reverse Transfer Capacitance	C <sub>rss</sub>			256			
Total Gate Charge		$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 20 \text{ A}$		65	100	nC	
	Qg			29	45		
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS}$ = 15 V, $V_{GS}$ = 4.5 V, $I_{D}$ = 20 A		11.5			
Gate-Drain Charge	Q <sub>gd</sub>			7.5			
Gate Resistance	Rg	f = 1 MHz	0.2	0.55	1.1	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			15	30		
Rise Time	t <sub>r</sub>	$V_{DD}$ = 15 V, $R_L$ = 1.5 $\Omega$		10	20		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 10 \text{ A}, \text{ V}_{\text{GEN}} = 10 \text{ V}, \text{ R}_{\text{g}} = 1 \Omega$		35	65		
Fall Time	t <sub>f</sub>			8	16		
Turn-On Delay Time	t <sub>d(on)</sub>			36	65	ns	
Rise Time	t <sub>r</sub>	$V_{DD}$ = 15 V, $R_L$ = 1.5 $\Omega$		17	30	-	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 10 \text{ A}, \text{ V}_{\text{GEN}} = 4.5 \text{ V}, \text{ R}_{\text{g}} = 1 \Omega$		45	80		
Fall Time	t <sub>f</sub>			20	40		
Drain-Source Body Diode Characteris	tics						
Continuous Source-Drain Diode Current	۱ <sub>S</sub>	T <sub>C</sub> = 25 °C			40	^	
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>			1	70	A	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 3 A		0.74	1.1	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			34	65	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			29	55	nC	
Reverse Recovery Fall Time	t <sub>a</sub>	$I_F = 10 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, \text{ T}_J = 25 ^\circ\text{C}$		17		ns	
Reverse Recovery Rise Time	t <sub>b</sub>			17			

Notes:

a. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %.

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



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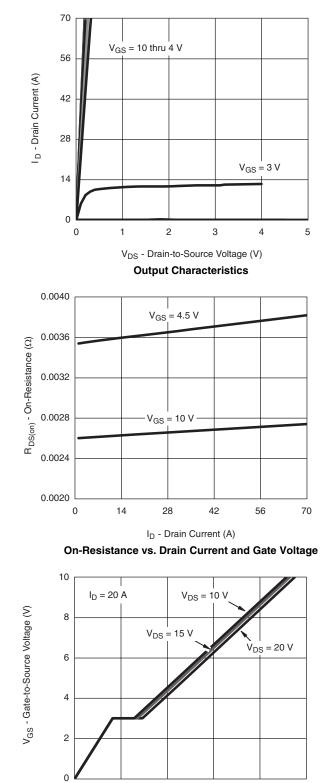
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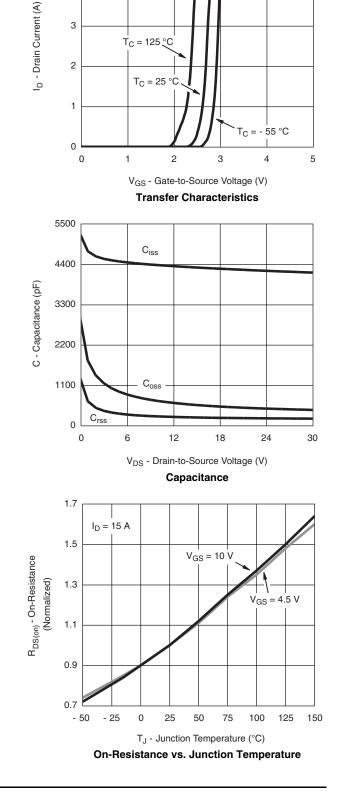


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#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





0

14

28

Qg - Total Gate Charge (nC)

Gate Charge

42

56

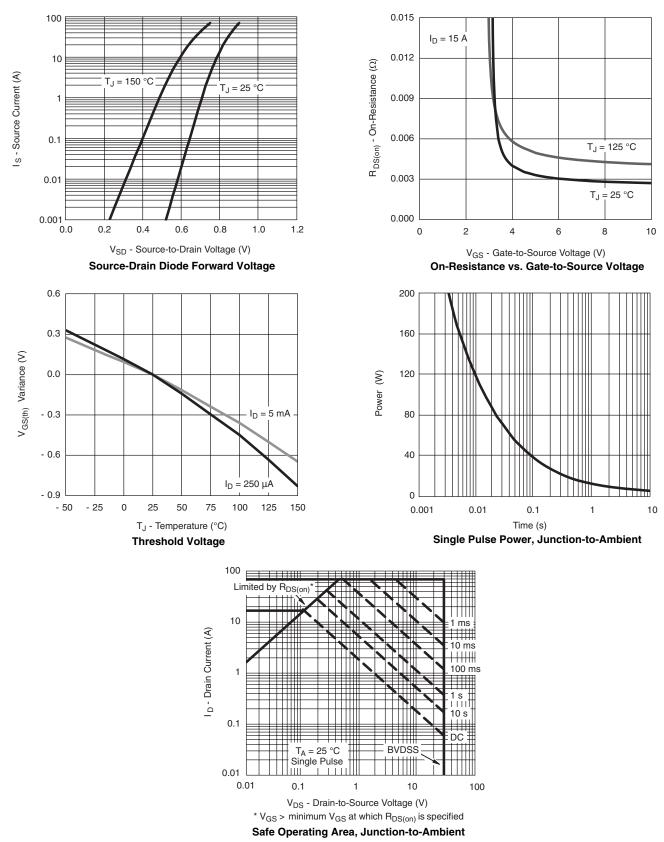
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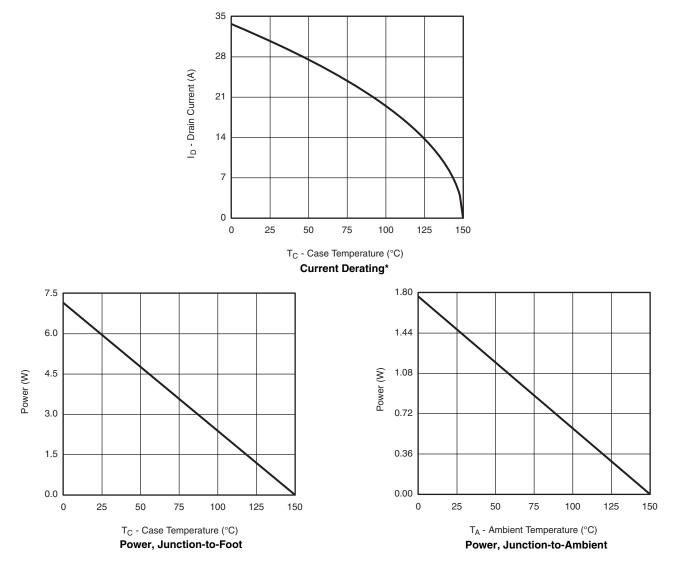
#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





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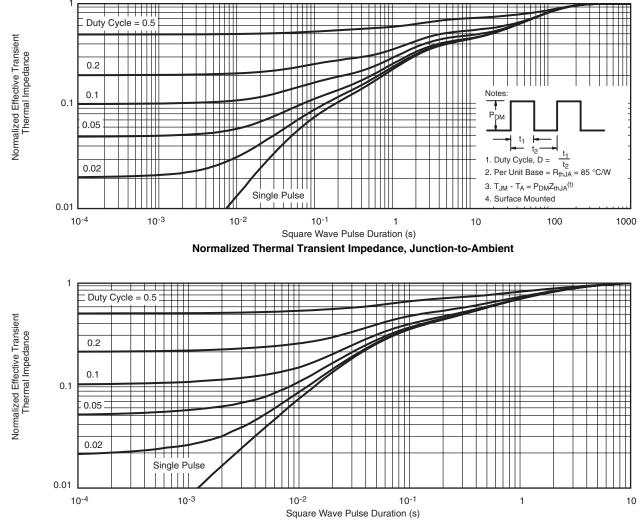
\* The power dissipation  $P_D$  is based on  $T_{J(max)}$  = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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# VISHAY.

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#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Foot

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