Si4701-A

Broadcast FM Radio Tuner for Portable Applications

Features

- Worldwide FM band support (76–108 MHz)
- Digital low-IF receiver
- Frequency synthesizer with integrated VCO
- Seek tuning
- Automatic frequency control (AFC)
- Automatic gain control (AGC)
- Excellent overload immunity
- Signal strength measurement
- Programmable de-emphasis (50/75 µs)
- Adaptive noise suppression
- Volume control
- Line-level analog output
- 32.768 kHz reference clock
- 2-wire and 3-wire control interface
- 2.7 to 5.5 V supply voltage
- Integrated LDO regulator allows direct connection to battery
- 4x4 mm 24-pin QFN package
  - Lead-free/RoHS compliant
- RDS/RBDS Processor

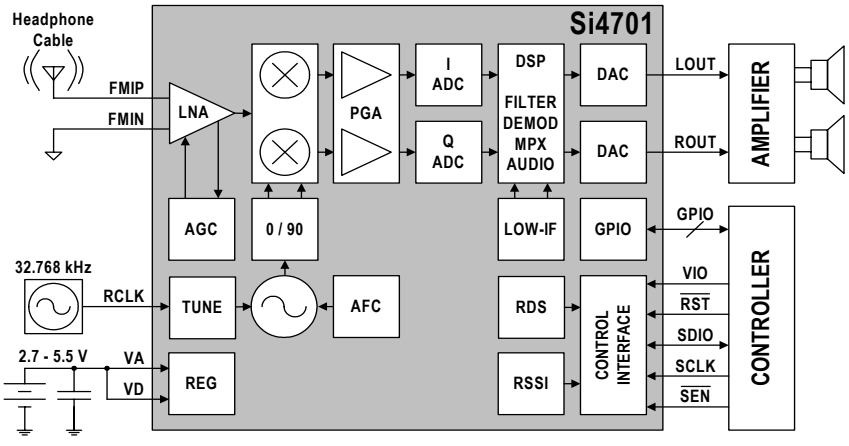
Applications

- Cellular handsets
- MP3 players
- Portable radios
- USB FM radio
- PDAs
- Notebook PCs

Description

The Si4701 integrates the complete tuner function from antenna input to stereo audio output for FM broadcast radio reception.

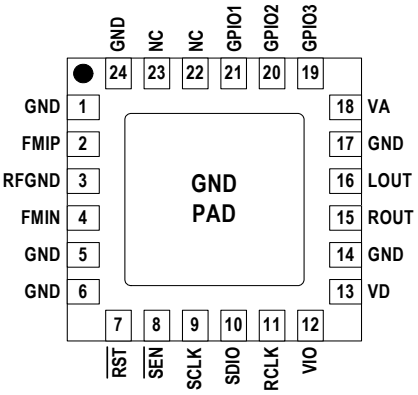
Functional Block Diagram



Ordering Information:
See page 26.

Pin Assignments (Top View)

Si4701-GM



Patents pending

Notes:

1. FM Receiver performance is subject to adherence to antenna design guidelines in “AN231: Headphone and Antenna Interface.” Failure to use these guidelines will negatively affect the performance of the Si4701, particularly in weak signal and noisy environments. Silicon Laboratories will evaluate schematics and layouts for qualified customers.
2. Place Si4701 as close as possible to antenna jack and keep FMIP trace as short as possible.

TABLE OF CONTENTS

Section **Page**

1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Supply Voltage	VD		2.7	—	5.5	V
Analog Supply Voltage	VA		2.7	—	5.5	V
Interface Supply Voltage	VIO		1.5	—	3.6	V
Ambient Temperature	T_A		–20	25	85	°C

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at VD = VA = 3.3 V and 25 °C unless otherwise stated. Parameters are tested in production unless otherwise stated.

Table 2. Absolute Maximum Ratings[1,2]

Parameter	Symbol	Value	Unit
Digital Supply Voltage	VD	–0.5 to 5.8	V
Analog Supply Voltage	VA	–0.5 to 5.8	V
Interface Supply Voltage	VIO	–0.5 to 3.9	V
Input Current[3]	I_{IN}	±10	mA
Input Voltage[3]	V_{IN}	–0.3 to (VIO + 0.3)	V
Operating Temperature	T_{OP}	–40 to 95	°C
Storage Temperature	T_{STG}	–55 to 150	°C
RF Input Level[4]		0.4	V_{pK}

Notes:
1. Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure beyond recommended operating conditions for extended periods may affect device reliability.
2. The Si4701 device is a high-performance RF integrated circuit with an ESD rating of < 2 kV. Handling and assembly of this device should only be done at ESD-protected workstations.
3. For input pins SCLK, SEN, SDIO, RST, RCLK, GPIO1, GPIO2, and GPIO3.
4. At RF input pins.

Table 3. DC Characteristics[1]

(VD = VA = 2.7 to 5.5 V, VIO = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Analog Supply Current[2]	I_A	ENABLE = 1	—	12.9	14.5	mA
Analog Supply Current[2,3,8]	I_A	ENABLE = 1 Low RSSI level	—	14	16.5	mA
Analog Powerdown Current[2,4,5]	I_{PDA}	ENABLE = 0	—	1.5	5	µA
Digital Supply Current[2]	I_D	ENABLE = 1	—	5.3	7.5	mA
Digital Supply Current[2,3,8,9]	I_D	ENABLE = 1 Low RSSI level	—	4.4	6.5	mA
Digital Powerdown Current[2,4,5]	I_{PDD}	ENABLE = 0	—	1.0	6	µA
Interface Supply Current[2]	I_{IO}	ENABLE = 1	—	400	600	µA
Interface Powerdown Current[4,5]	I_{IO}	SCLK, RCLK inactive ENABLE = 0	—	0.5	2	µA
High Level Input Voltage[6]	V_{IH}		0.7 x VIO	—	VIO + 0.3	V
Low Level Input Voltage[6]	V_{IL}		–0.3	—	0.3 x VIO	V
High Level Input Current[6]	I_{IH}	V_{IN} = VIO = 3.6 V	–10	—	10	µA
Low Level Input Current[6]	I_{IL}	V_{IN} = 0 V, VIO = 3.6 V	–10	—	10	µA
High Level Output Voltage[7]	V_{OH}	I_{OUT} = 500 µA	0.8 x VIO	—	—	V
Low Level Output Voltage[7]	V_{OL}	I_{OUT} = –500 µA	—	—	0.2 x VIO	V

Notes:

1. This table applies to Si4701 Firmware Revision 14.
2. Refer to 6. "Register Descriptions" on page 19 for ENABLE bit description.
3. The LNA is automatically switched to higher current mode for optimum sensitivity in weak signal conditions.
4. Specifications are guaranteed by characterization.
5. Refer to Section 4.8. "Reset, Powerup, and Powerdown" on page 16.
6. For input pins SCLK, SEN, SDIO, RST, RCLK, GPIO1, GPIO2, and GPIO3.
7. For output pins SDIO, GPIO1, GPIO2, and GPIO3.
8. Analog and digital supply currents are simultaneously adjusted based on RSSI level.
9. Stereo and RDS functionality are disabled at low RSSI levels.

Table 4. Reset Timing Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
$\overline{SEN}$, SDIO Input to $\overline{RST}$ ↑ Setup	t_{SRST}		30	—	—	ns
$\overline{SEN}$, SDIO Input to $\overline{RST}$ ↑ Hold	t_{HRST}		30	—	—	ns

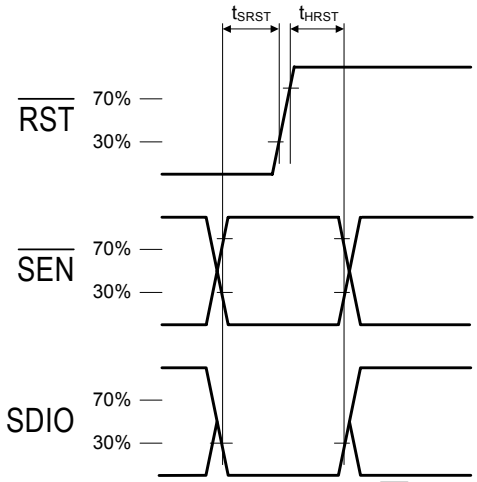


Figure 1. Reset Timing Parameters

Table 5. 3-Wire Control Interface Characteristics
(VD = VA = 2.7 to 5.5 V, VIO = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{CLK}		0	—	2.5	MHz
SCLK High Time	t_{HIGH}		25	—	—	ns
SCLK Low Time	t_{LOW}		25	—	—	ns
SDIO Input, $\overline{SEN}$ to SCLK ↑ Setup	t_S		20	—	—	ns
SDIO Input to SCLK ↑ Hold	t_{HSDIO}		10	—	—	ns
$\overline{SEN}$ Input to SCLK ↓ Hold	t_{HSEN}		10	—	—	ns
SCLK ↑ to SDIO Output Valid	t_{CDV}	Read	2	—	25	ns
SCLK ↑ to SDIO Output High Z	t_{CDZ}	Read	2	—	25	ns

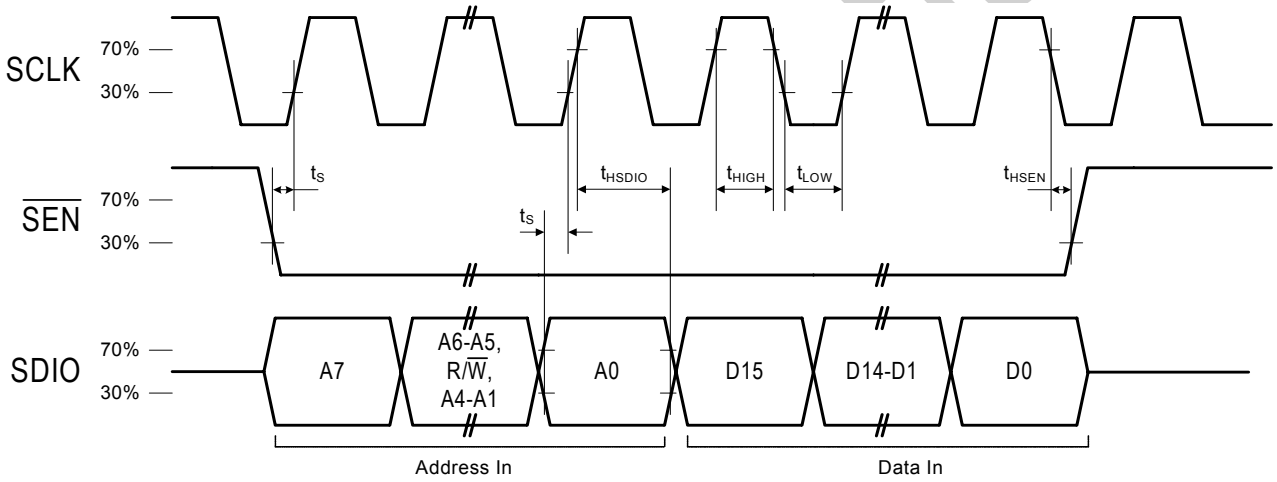


Figure 2. 3-Wire Control Interface Write Timing Parameters

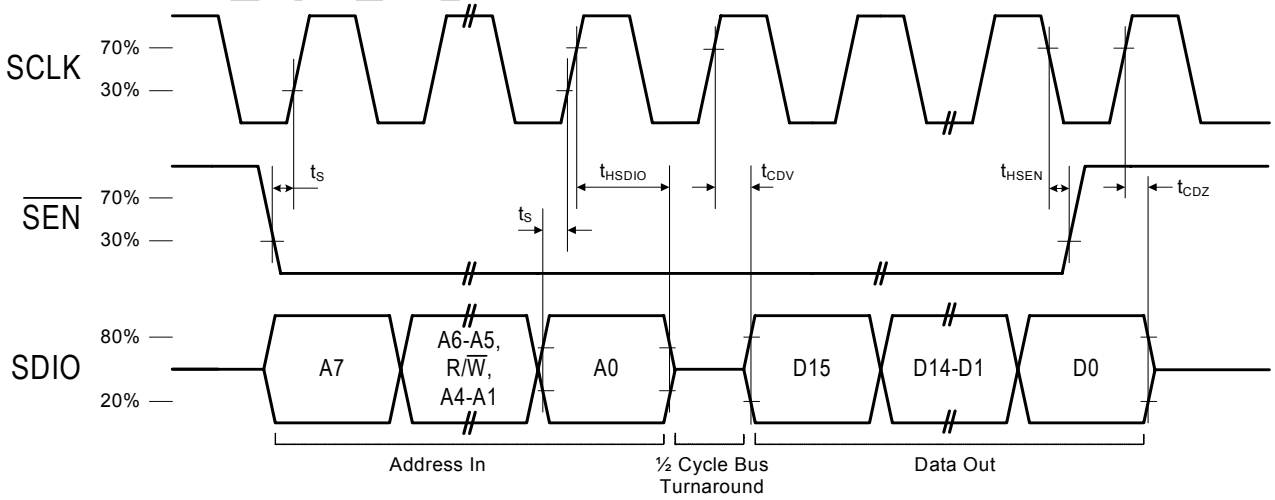


Figure 3. 3-Wire Control Interface Read Timing Parameters

Table 6. 2-Wire Control Interface Characteristics[1]
(VD = VA = 2.7 to 5.5 V, VIO = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK Frequency	f_{SCL}		0	—	400	kHz
SCLK Low Time	t_{LOW}		1.3	—	—	µs
SCLK High Time	t_{HIGH}		0.6	—	—	µs
SCLK Input to SDIO ↓ Setup (START)	$t_{SU:STA}$		0.6	—	—	µs
SCLK Input to SDIO ↓ Hold (START)	$t_{HD:STA}$		0.6	—	—	µs
SDIO Input to SCLK ↑ Setup	$t_{SU:DAT}$		100	—	—	ns
SDIO Input to SCLK ↓ Hold[2]	$t_{HD:DAT}$		0	—	900	ns
SCLK input to SDIO ↑ Setup (STOP)	$t_{SU:STO}$		0.6	—	—	µs
STOP to START Time	t_{BUF}		1.3	—	—	µs
SDIO Output Fall Time	$t_{f:OUT}$		20 + 01.C_b	—	250	ns
SDIO Input, SCLK Rise/Fall Time	$t_{f:IN}$ $t_{r:IN}$		20 + 01.C_b	—	300	ns
SCLK, SDIO Capacitive Loading	C_b		—	—	50	pF
Input Filter Pulse Suppression	t_{SP}		—	—	50	ns

Notes:
1. When VIO = 0 V, SCLK and SDIO are low impedance.
2. As a transmitter, the Si4701 delays SDIO by a minimum of 300 ns from the V_{IH} threshold of SCLK to comply with the 0 ns $t_{HD:DAT}$ specification.

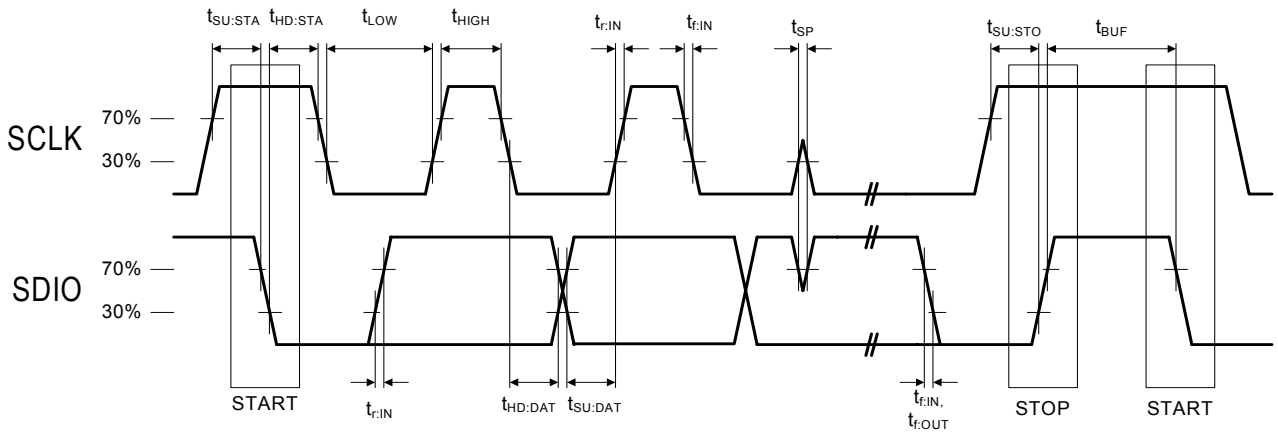


Figure 4. 2-Wire Control Interface Read and Write Timing Parameters

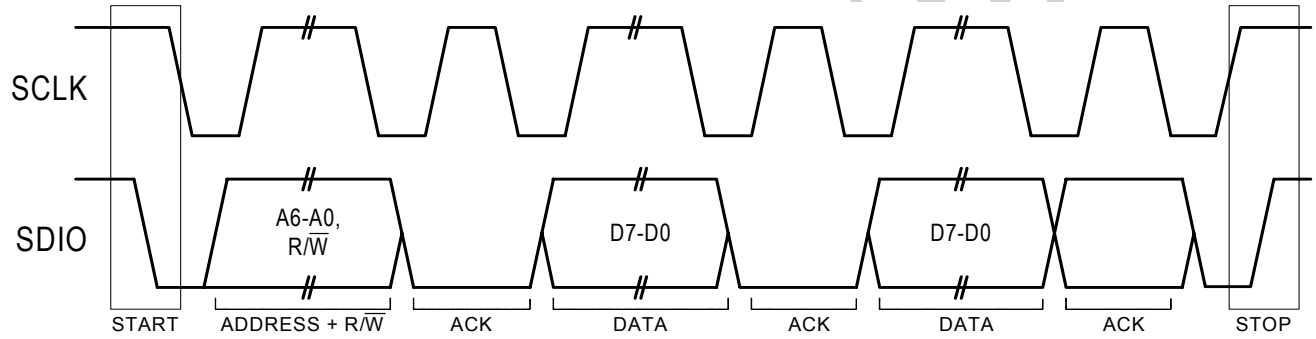


Figure 5. 2-Wire Control Interface Read and Write Timing Diagram

Table 7. FM Receiver Characteristics[1,2,3]

(VD = VA = 2.7 to 5.5 V, VIO = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Frequency	f_{RF}		76	—	108	MHz
Sensitivity[4,5,6]		(S+N)/N = 26 dB	—	2.5	3.6	µV EMF
RDS Sensitivity		Δf = 2 kHz, RDS BLER < 5%	—	15	—	µV EMF
LNA Input Resistance[7,12]			3	4	5	kΩ
LNA Input Capacitance[7,12]			4	5	6	pF
Input IP3[8,12]			105	108	—	dBµV EMF
AM Suppression[4,5,7,12]		m = 0.3	40	55	—	dB
Adjacent Channel Selectivity		±200 kHz	35	50	—	dB
Alternate Channel Selectivity		±400 kHz	60	70	—	dB
Spurious Response Rejection[12]		In-band	35	—	—	dB
RCLK Frequency			—	32.768	—	kHz
RCLK Frequency Tolerance[13]		SPACE[1:0] = 00 or 01	–200	—	200	ppm
		SPACE[1:0] = 10	–50	—	50	
Audio Output Voltage[4,5,7]			72	80	90	mV_{RMS}
Audio Output L/R Imbalance[4,7,9]			—	—	1	dB
Audio Band Limits[4,7,12]		±1.5 dB	30	—	15k	Hz
Audio Stereo Separation[4,7,9]			25	—	—	dB
Audio S/N[4,5,6,7,12]			58	63	—	dB
Audio THD[4,7,9]			—	0.1	0.5	%
De-emphasis Time Constant[10]		DE = 0	70	75	80	µs
		DE = 1	45	50	54	µs

Notes:

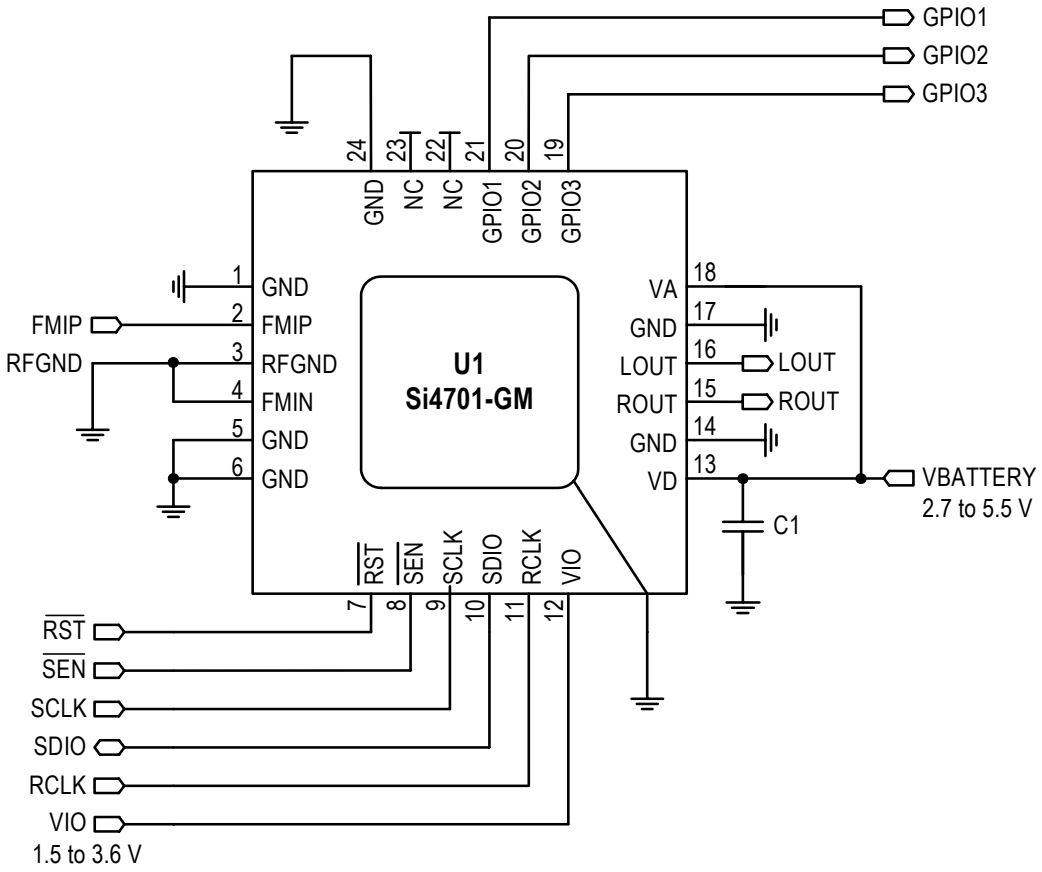
1. Additional testing information is available in Application Note AN234. Volume = maximum for all tests.
2. This table applies to Si4701 Firmware Revision 14.
3. FM Receiver performance specifications are subject to adherence to antenna design guidelines in AN231: Headphone and Antenna Interface. Failure to use these guidelines will negatively affect the performance of the Si4701, particularly in weak signal and noisy environments. Silicon Laboratories will evaluate schematics and layouts for qualified customers.
4. F_{MOD} = 1 kHz, 75 µs de-emphasis, MONO = 1, and L = R unless noted otherwise.
5. Δf = 22.5 kHz.
6. B_{AF} = 300 Hz to 15 kHz, A-weighted.
7. Measured at V_{EMF} = 1 mV, f_{RF} = 76 to 108 MHz.
8. $|f_2 – f_1| > 1$ MHz, $f_0 = 2 \times f_1 – f_2$. AGC is disabled by setting AGCD = 1. Refer to "6. Register Descriptions" on page 19.
9. Δf = 75 kHz.
10. The de-emphasis time constant is selected with the DE bit. Refer to "6. Register Descriptions" on page 19.
11. At LOUT and ROUT pins.
12. Guaranteed by characterization.
13. The channel spacing is selected with the SPACE[1:0] bits. Refer to "6. Register Descriptions" on page 19. Seek tuning is not recommended for 50 kHz channel spacing.

Table 7. FM Receiver Characteristics[1,2,3] (Continued)
(VD = VA = 2.7 to 5.5 V, VIO = 1.5 to 3.6 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Audio Common Mode Voltage[11]			0.7	0.8	0.9	V
Audio Output Load Resistance[11,12]	R_L	Single-ended	10	—	—	kΩ
Audio Output Load Capacitance[11,12]	C_L	Single-ended	—	—	50	pF
Seek Time			—	—	60	ms/channel
Powerup Time		From powerdown	—	—	110	ms

Notes:
1. Additional testing information is available in Application Note AN234. Volume = maximum for all tests.
2. This table applies to Si4701 Firmware Revision 14.
3. FM Receiver performance specifications are subject to adherence to antenna design guidelines in AN231: Headphone and Antenna Interface. Failure to use these guidelines will negatively affect the performance of the Si4701, particularly in weak signal and noisy environments. Silicon Laboratories will evaluate schematics and layouts for qualified customers.
4. F_{MOD} = 1 kHz, 75 µs de-emphasis, MONO = 1, and L = R unless noted otherwise.
5. Δf = 22.5 kHz.
6. B_{AF} = 300 Hz to 15 kHz, A-weighted.
7. Measured at V_{EMF} = 1 mV, f_{RF} = 76 to 108 MHz.
8. $|f_2 – f_1| > 1$ MHz, $f_0 = 2 \times f_1 – f_2$. AGC is disabled by setting AGCD = 1. Refer to "6. Register Descriptions" on page 19.
9. Δf = 75 kHz.
10. The de-emphasis time constant is selected with the DE bit. Refer to "6. Register Descriptions" on page 19.
11. At LOUT and ROUT pins.
12. Guaranteed by characterization.
13. The channel spacing is selected with the SPACE[1:0] bits. Refer to "6. Register Descriptions" on page 19. Seek tuning is not recommended for 50 kHz channel spacing.

2. Typical Application Schematic



Notes:

1. Place C1 close to VD pin.
2. All grounds connect directly to GND plane on PCB.
3. Pins 22 and 23 are no connects, leave floating.
4. FM Receiver performance is subject to adherence to antenna design guidelines in “AN231: Headphone and Antenna Interface.” Failure to use these guidelines will negatively affect the performance of the Si4701, particularly in weak signal and noisy environments. Silicon Laboratories will evaluate schematics and layouts for qualified customers.
5. Pin 2 connects to the antenna interface, refer to “AN231: Headphone and Antenna Interface.”
6. RFGND should be locally isolated from GND, refer to “AN231: Headphone and Antenna Interface.”
7. Place Si4701 as close as possible to antenna jack and keep FMIP trace as short as possible.

3. Bill of Materials

Component(s)	Value/Description	Supplier(s)
C1	Supply bypass capacitor, 22 nF, ±20%, Z5U/X7R	Murata
U1	Si4701 FM Radio Tuner	Silicon Laboratories

4. Functional Description

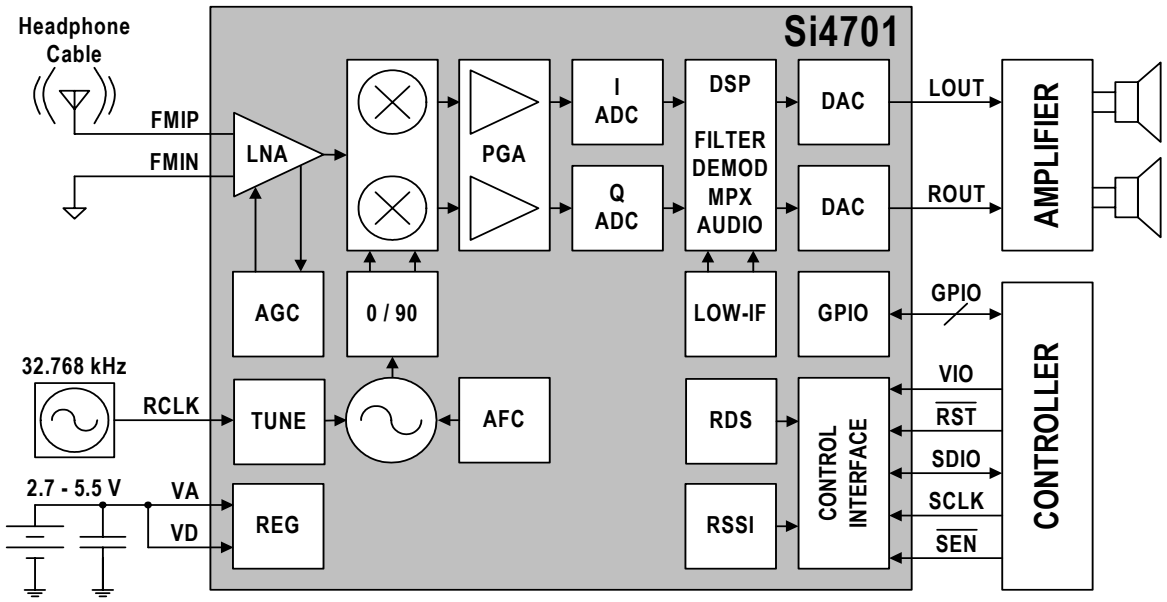


Figure 6. Si4701 FM Receiver Block Diagram

4.1. Overview

The Si4701 is the industry's first FM radio tuner IC to leverage digital integration and 100% CMOS process technology, resulting in a completely integrated solution that requires only one external supply bypass capacitor and less than 20 mm^2 of board space. Offering unmatched integration, the Si4701 allows FM radio reception to be added to a variety of portable devices where board space, performance, low power consumption, and ease of use are essential.

Leveraging Silicon Laboratories' proven Aero® digital low intermediate frequency (low-IF) receiver architecture and frequency synthesizer technology, the Si4701 delivers superior RF performance and interference rejection. Digital signal processing is utilized to provide optimum sound quality with varying reception conditions.

The high integration and complete system production test simplifies design-in, increases quality, and improves manufacturability. The Si4701 uses a streamlined programming model, which further reduces product development time. Power management is also simplified with an integrated regulator allowing direct connection to a 2.7 to 5.5 V battery.

The Si4701 incorporates a digital processor for the European Radio Data System (RDS) and the North American Radio Broadcast Data System (RBDS) including all required symbol decoding, block synchronization, error detection, and error correction functions. Using this feature, the Si4701 enables broadcast data such as station identification and song name to be displayed to the user.

4.2. FM Receiver

The receiver uses a digital low-IF architecture which allows for the elimination of external components and factory adjustments. The receive (RX) section integrates a low noise amplifier (LNA) supporting the worldwide FM broadcast band (76 to 108 MHz). An automatic gain control (AGC) circuit controls the gain of the LNA to optimize sensitivity and rejection of strong interferers. For testing purposes, the AGC can be disabled with the AGCD bit. Refer to Section 6. "Register Descriptions" on page 19 for additional programming and configuration information.

The Si4701 antenna design is not conventional. Adherence to the design guidelines in "AN231: Headphone and Antenna Interface" will result in excellent system performance. Failure to use these guidelines will negatively affect the performance of the Si4701, particularly in weak signal and noisy environments. Silicon Laboratories will evaluate schematics and layouts for qualified customers.

An image-reject mixer downconverts the RF signal to low-IF. The quadrature mixer output is amplified, filtered, and digitized with high resolution analog-to-digital converters (ADCs). This advanced architecture allows the use of digital signal processing (DSP) to

perform channel selection, FM demodulation, and stereo audio processing to achieve superior performance compared to traditional analog architectures.

4.3. Stereo Audio Processing

The output of the FM demodulator is a stereo multiplexed (MPX) signal. The MPX standard was developed in 1961, and is used worldwide. Today's MPX signal format consists of Left + Right (L+R) audio, Left – Right (L–R) audio, a 19 kHz pilot tone, and RDS/RBDS data as shown in Figure 7 below.

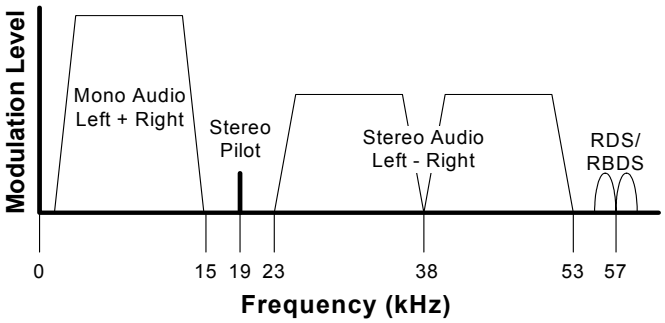


Figure 7. MPX Signal Spectrum

The Si4701's integrated stereo decoder automatically decodes the MPX signal using DSP techniques. The 0 to 15 kHz (L+R) signal is the mono output of the FM tuner. Stereo is generated from the (L+R), (L-R), and a 19 kHz pilot tone. The pilot tone is used as a reference to recover the (L-R) signal. Output left and right channels are obtained by adding and subtracting the (L+R) and (L-R) signals, respectively. The Si4701 uses frequency information from the 19 kHz stereo pilot to recover the 57 kHz RDS/RBDS signal.

Adaptive noise suppression is employed to gradually combine the stereo left and right audio channels to a mono (L+R) audio signal as the signal quality degrades to maintain optimum sound fidelity under varying reception conditions. Stereo/mono status can be monitored with the ST register bit and mono operation can be forced with the MONO register bit.

Pre-emphasis and de-emphasis is a technique used by FM broadcasters to improve the signal-to-noise ratio of FM receivers by reducing the effects of high frequency interference and noise. When the FM signal is transmitted, a pre-emphasis filter is applied to accentuate the high audio frequencies. All FM receivers incorporate a de-emphasis filter which attenuates high frequencies to restore a flat frequency response. Two time constants are used in various regions. The de-emphasis time constant is programmable to 50 or 75 µs with the DE bit.

High-fidelity stereo digital-to-analog converters (DACs) drive analog audio signals onto the LOUT and ROUT pins. The audio output may be muted with the DMUTE bit. Volume can be adjusted digitally with the VOLUME[3:0] bits.

The soft mute feature attenuates audio output by up to 24 dB to minimize audible noise in very weak signal conditions.

4.4. Tuning

The frequency synthesizer uses Silicon Laboratories' proven technology including a completely integrated VCO. The frequency synthesizer generates the quadrature local oscillator signal used to downconvert the RF input to a low intermediate frequency. The VCO frequency is locked to the reference clock and adjusted with an automatic frequency control (AFC) servo loop during reception.

The tuning frequency is defined as:

$$\text{Freq (MHz)} = \text{Spacing (kHz)} \times \text{Channel} + \text{Bottom of Band (MHz)}$$

Channel spacing of 50, 100 or 200 KHz is selected with bits SPACE[1:0]. The channel is selected with bits CHAN[9:0]. The bottom of the band is set to 76 MHz or 87.5 MHz with the bits BAND[1:0]. The tuning operation begins by setting the TUNE bit. After tuning completes, the Seek/Tune Complete (STC) bit will be set and the RSSI level is available by reading bits RSSI[7:0]. The TUNE bit must be set low after the STC bit is set high in order to complete the tune operation and clear the STC bit.

Seek tuning searches up or down for a channel with an RSSI greater than or equal to the Seek Threshold set with the SEEKTH[7:0] bits. Two seek modes are available. When the Seek Mode (SKMODE) bit is low and a seek is initiated, the device seeks through the band, wraps from one band edge to the other, and continues seeking. If the seek operation was unable to find a channel, the Seek Failure/Band Limit (SF/BL) bit will be set high and the device will return to the channel selected before the seek operation began. When the SKMODE bit is high and a seek is initiated, the device seeks through the band until the band limit is reached and the SF/BL bit will be set high. A seek operation is initiated by setting the SEEK and SEEKUP bits. After the seek operation completes, the STC bit will be set, and the RSSI level and channel are available by reading bits RSSI[7:0] and bits READCHAN[9:0]. During a seek operation READCHAN[9:0] is also updated and may be read to determine seek progress. The STC bit will be set after the seek operation completes. The channel is valid if the seek operation completes and the SF/BL bit is set low. At other times, such as before a seek operation or after a seek completes and the SF/BL bit is

set high, the channel is valid if the AFC Rail (AFCRL) bit is set low and the value of RSSI[7:0] is greater than or equal to SEEKTH[7:0]. The SEEK bit must be set low after the STC bit is set high in order to complete the seek operation and clear the STC and SF/BL bits. The seek operation may be aborted by setting the SEEK bit low at any time.

The device can be configured to generate an interrupt on GPIO2 when a tune or seek operation completes. Setting the Seek/Tune Complete (STCIEN) bit and GPIO2[1:0] = 01 will configure GPIO2 for a 5 ms low interrupt when the STC bit is set by the device.

Seek tuning is not recommended for 50 kHz channel spacing.

4.5. Reference Clock

The Si4701 accepts a 32.768 kHz reference clock to the RCLK pin. The reference clock is required whenever the ENABLE bit is set high. Refer to Table 3, “DC Characteristics[1],” on page 5 for switching voltage levels and Table 7, “FM Receiver Characteristics[1,2,3],” on page 10 for frequency tolerance information.

4.6. Control Interface

Two-wire slave-transceiver and three-wire interfaces are provided for the controller IC to read and write the control registers. Three-wire mode is selected during initialization if SEN is held low on a the rising edge of RST, and two-wire mode is selected if SEN is held high on the rising edge of RST. Registers may be written and read when the VIO supply is applied regardless of the state of the VD or VA supplies. RCLK is not required for proper register operation.

4.6.1. 3-Wire Control Interface

For three-wire operation, a transfer begins when the SEN pin is set low on a rising SCLK edge. The control word is latched internally on rising SCLK edges and is nine bits in length, comprised of a four bit chip address A7:A4 = 0110b, a read/write bit (write = 0 and read = 1), and a four bit register address, A3:A0. The ordering of the control word is A7:A5, R/W, A4:A0. Refer to Section 5. "Register Summary" on page 18 for a list of all registers and their addresses.

For write operations, the serial control word is followed by a 16-bit data word and is latched internally on rising SCLK edges.

For read operations, a bus turn-around of half a cycle is followed by a 16-bit data word shifted out on rising SCLK edges. The transfer ends on the rising SCLK edge after SEN is set high. Note that 26 SCLK cycles are required for a transfer, however, SCLK may run continuously.

For details on timing specifications and diagrams, refer to Table 5, “3-Wire Control Interface Characteristics,” on page 7, Figure 2, “3-Wire Control Interface Write Timing Parameters,” on page 7, and Figure 3, “3-Wire Control Interface Read Timing Parameters,” on page 7.

4.6.2. 2-wire Control Interface

For two-wire operation, a transfer begins with the START condition. The control word is latched internally on rising SCLK edges and is eight bits in length, comprised of a seven bit device address equal to 0010000b and a read/write bit (write = 0 and read = 1). The device acknowledges the address by setting SDIO low on the next falling SCLK edge.

For write operations, the device acknowledge is followed by an eight bit data word latched internally on rising edges of SCLK. The device always acknowledges the data by setting SDIO low on the next falling SCLK edge. Any number of data bytes may be written and register addresses are incremented by an internal address counter, starting with the upper byte of register 02h, followed by the lower byte of register 02h, and wrap back to 00h at the end of the register file.

For read operations, the device acknowledge is followed by an eight bit data word shifted out on falling SCLK edges. The controller IC returns an acknowledge if additional data will be transferred. Any number of data bytes can be read and register addresses are incremented by an internal address counter, starting at the upper byte of register 0Ah, followed by the lower byte of register 0Ah, and wrap back to 00h at the end of the register file. The transfer ends with the STOP conditions regardless of the state of the acknowledge.

For details on timing specifications and diagrams, refer to Table 6, “2-Wire Control Interface Characteristics[1],” on page 8, Figure 4, “2-Wire Control Interface Read and Write Timing Parameters,” on page 9 and Figure 5, “2-Wire Control Interface Read and Write Timing Diagram,” on page 9.

4.7. GPIO Outputs

The general purpose I/O (GPIO) functionality may be programmed with bits GPIO1[1:0], GPIO2[1:0], and GPIO3[1:0]. GPIO pins can be configured to output a constant low or high, or to high-Z. Setting STCIEN = 1 and GPIO2 = 01 will generate a 5 ms low pulse on GPIO2 when the STC bit is set. Setting RDSIEN = 1 and GPIO2 = 01 will generate a 5 ms low pulse on GPIO2 when the RDSR bit is set. STCIEN and RDSIEN bits may be set simultaneously. GPIO3 may be configured to provide a stereo/mono indication by setting GPIO3[1:0] = 01. Constant low, high or high-Z functionality is available regardless of the state of VA and VD supplies or the ENABLE and DISABLE bits.

4.8. Reset, Powerup, and Powerdown

Setting the $\overline{\text{RST}}$ pin low will disable analog and digital circuitry, reset the registers to their default settings, and disable the bus. Setting the $\overline{\text{RST}}$ pin high will bring the device out of reset. Setting $\overline{\text{SEN}}$ high on the rising edge of $\overline{\text{RST}}$ will select 2-wire operation and setting $\overline{\text{SEN}}$ low will select 3-wire operation. SDIO must always be set low on the rising edge of $\overline{\text{RST}}$. Refer to Table 4, “Reset Timing Characteristics,” on page 6 and Figure 1, “Reset Timing Parameters,” on page 6.

Setting the ENABLE bit high and the DISABLE bit low will powerup the device. A powerdown mode is available to reduce power consumption when the part is idle. Setting the ENABLE bit high and the DISABLE bit high will disable analog and digital circuitry while maintaining register configuration and keeping the bus active. Note that the device automatically sets the ENABLE bit low after the internal powerdown sequence completes. Setting the ENABLE bit low directly will cause the device to partially powerdown and should be avoided. Setting the ENABLE bit high and the DISABLE bit low will bring the device out of powerdown mode and resume normal operation. Refer to Table 3 on page 5 for current consumption specifications during powerdown.

4.9. Initialization Sequence

Refer to Figure 8, “Initialization Sequence,” on page 17.

To initialize the device:

1. Supply VA and VD.
2. Supply VIO while keeping the $\overline{\text{RST}}$ pin low. Note that steps 1 and 2 may be reversed. Power supplies may be sequenced in any order.
3. Provide RCLK.
4. Set the $\overline{\text{RST}}$ pin high. Setting $\overline{\text{SEN}}$ high on the rising edge of $\overline{\text{RST}}$ will select 2-wire operation and setting $\overline{\text{SEN}}$ low will select 3-wire operation. SDIO must always be set low on the rising edge of $\overline{\text{RST}}$. The device registers may now be read and written. Note that steps 3 and 4 may be reversed.
5. Set the ENABLE bit high and the DISABLE bit low to powerup the device.

To power down the device:

1. Set the ENABLE bit high and the DISABLE bit high to place the device in powerdown mode. Note that all register states are maintained so long as VIO is supplied and the $\overline{\text{RST}}$ pin is high.
2. Remove VA and VD supplies as needed.

To power up the device (after power down):

1. Note that VIO is still supplied in this scenario. If VIO is not supplied, refer to device initialization procedure above.
2. Supply VA and VD.
3. Set the ENABLE bit high and the DISABLE bit low to powerup the device.

4.10. Programming Guide

Refer to "AN230: Si4700/01 Programming Guide" for control interface programming information.

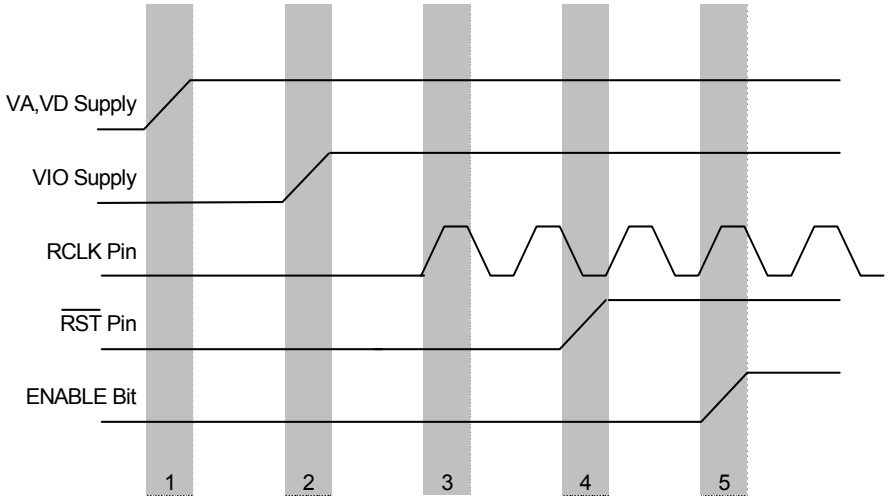


Figure 8. Initialization Sequence

4.11. RDS/RBDS Processor and Functionality

The Si4701 implements an RDS/RBDS* processor for symbol decoding, block synchronization, error detection, and error correction. RDS functionality is enabled by setting the RDS bit. Setting the RDS Interrupt Enable (RDSIEN) bit and GPIO2[1:0] = 01 will configure GPIO2 for a 5 ms low interrupt when the device sets the RDS Ready (RDSR) bit.

The Si4701 offers two RDS modes, a Standard mode and Verbose mode. The primary difference is increased visibility to RDS block error levels and synchronization status in RDS Verbose mode.

When the RDSM bit is high, the device is in RDS Verbose mode. The device sets the RDSR bit for a minimum of 40 ms when RDS is synchronized and RDS group data has been received by the device. The RDSR bit is set regardless of RDS block error levels in the data group. Verbose mode sets RDSR high every 1.1875 ms. If the device loses RDS synchronization (RDSS = 0), RDS data decode and data capture are not possible, and RDSR will not be set until RDS synchronization is reestablished (RDSS = 1), and an RDS data group has been received.

***Note:** RDS/RBDS is referred to only as RDS throughout the remainder of this document.

RDS Verbose mode reports RDS decoder synchronization status in RDSS, and detailed bit errors in the information word for each RDS block in BLERA, BLERB, BLERC, and BLERD. The range of reportable block errors is 0, 1–2, 3–5, or 6+. More than six errors indicates that the corresponding block information word contains six or more non-correctable errors, or that the block checkword contains errors.

When the RDSM bit is low, the device is in Standard RDS mode (default). The device will set the RDSR bit when an RDS data group has been received. RDS block errors are reported in RDSE, as in previous Beta firmware releases 10, 11, 12. RDSE is the concatenation of RDSS and BLERA in RDS Verbose mode. RDSE reports error visibility at the group level as 0 (no block errors) to 4 (all blocks have errors). If RDSE is non-zero, the data in RDSA, RDSB, RDSC, and RDSD is invalid and should be discarded. RDS Standard mode is intended to save processing overhead in the host application processor.

In both RDS Standard and RDS Verbose modes, received RDS data is available by reading registers RDSA, RDSB, RDSC, and RDSD.

When RDS is enabled, the Si4701-A14-GM can exhibit high RDS data block error rates in the limited FM frequency ranges of 95.5 to 97.0 MHz and 101.7 to 107.5 MHz. The probability of occurrence of this issue when a frequency in the above listed is selected is estimated at 10%. This issue has been isolated to a specific instruction sequence and is resolved in the Si4701-B15-GM, which is available starting in April 2006.

Refer to "AN243: Using RDS/RBDS with the Si4701" for additional information.

5. Register Summary

Reg[1]	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00h	DEVICEID	PN[3:0]				MFGID[11:0]											
01h	CHIPID	REV[5:0]						DEV	FIRMWARE[8:0]								
02h	POWERCFG	DSMUTE	DMUTE	MONO	0	RDSM	SKMODE	SEEKUP	SEEK	0	DISABLE	0	0	0	0	0	ENABLE
03h	CHANNEL	TUNE	0	0	0	0	0	CHAN[9:0]									
04h	SYSCONFIG1	RDSIEN	STCIEN	0	RDS	DE	AGCD	0	0	0	0	GPIO3[1:0]		GPIO2[1:0]		GPIO1[1:0]	
05h	SYSCONFIG2	SEEKTH[7:0]								BAND[1:0]		SPACE[1:0]		VOLUME[3:0]			
06h	SYSCONFIG3																
07h	TEST1																
08h	TEST2																
09h	BOOTCONFIG																
0Ah	STATUSRSSI	RDSR	STC	SF/BL	AFCRL	RDSS[2,3]	BLERA[1:0][2,3]		ST	RSSI[7:0]							
0Bh	READCHAN	BLERB[1:0][2]		BLERC[1:0][2]		BLERD[1:0][2]		READCHAN[9:0]									
0Ch	RDSA	RDSA[15:0]															
0Dh	RDSB	RDSB[15:0]															
0Eh	RDSC	RDSC[15:0]															
0Fh	RDSD	RDSD[15:0]															

Notes:

1. Any register not listed is reserved and should not be written. Writing to reserved registers may result in unpredictable behavior.
2. Available in RDS Verbose mode only.
3. In RDS Standard mode, RDSS and BLERA function as RDSE providing RDS data group-level error information.

6. Register Descriptions

Reg	Bits	Name	Type	Description
00h	15:12	PN[3:0]	R	**Part Number.** 0x01 = Si4701
00h	11:0	MFGID[11:0]	R	**Manufacturer ID.** 0x242
01h	15:10	REV[5:0]	R	**Chip Version.** 0x01 = Rev A (current)
01h	9	DEV	R	**Device.** 0 before powerup (ENABLE = 0). 1 after powerup (ENABLE = 1), enables Si4701 functionality.
01h	8:0	FIRMWARE[8:0]	R	**Firmware Version.** 0 before powerup (ENABLE = 0). Firmware version after powerup (ENABLE = 1).
02h	15	DSMUTE	R/W	**Softmute Disable.** 0 = Softmute enable (default). 1 = Softmute disable.
02h	14	DMUTE	R/W	**Mute Disable.** 0 = Mute enable (default). 1 = Mute disable.
02h	13	MONO	R/W	**Mono Select.** 0 = Stereo (default). 1 = Force mono.
02h	11	RDSM	R/W	**RDS Mode.** 0 = Standard (default). 1 = Verbose. Refer to “4.11. RDS/RBDS Processor and Functionality”.
02h	10	SKMODE	R/W	**Seek Mode.** 0 = Wrap at the upper or lower band limit and continue seeking (default). 1 = Stop seeking at the upper or lower band limit.
02h	9	SEEKUP	R/W	**Seek Up.** 0 = Seek down (default). 1 = Seek up.

Reg	Bits	Name	Type	Description
02h	8	SEEK	R/W	**Seek.** 0 = Disable (default). 1 = Enable. **Notes:** **1.** Seek begins at the current channel, and goes in the direction specified with the SEEKUP bit. Seek ends when a channel is found with RSSI level equal or greater than SEEKTH[7:0], the entire band has been searched (SKMODE = 0), or the upper or lower band limit has been reached (SKMODE = 1). **2.** The STC bit is set high when the seek operation completes and the SF/BL bit is set high if the seek operation was unable to find a channel with an RSSI greater than or equal to SEEKTH[7:0]. The STC and SF/BL bits must be set low by setting the SEEK bit low before the next seek or tune may begin. **3.** Seek operation is not recommended for 50 kHz channel spacing. **4.** A seek operation may be aborted by setting SEEK = 0.
02h	6	DISABLE	R/W	**Powerup Disable.** Refer to “4.8. Reset, Powerup, and Powerdown”.
02h	0	ENABLE	R/W	**Powerup Enable.** Refer to “4.8. Reset, Powerup, and Powerdown”.
03h	15	TUNE	R/W	**Tune.** 0 = Disable (default). 1 = Enable. The tune operation begins when the TUNE bit is set high. The STC bit is set high when the tune operation completes. The STC bit must be set low by setting the TUNE bit low before the next tune or seek may begin.
03h	9:0	CHAN[9:0]	R/W	**Channel Select.** BAND = 00 Freq (MHz) = Spacing (kHz) x Channel + 87.5 MHz BAND = 01, BAND = 10 Freq (MHz) = Spacing (kHz) x Channel + 76 MHz READCHAN[9:0] is updated during a seek operation and the final channel is updated after a seek operation completes (STC = 1). Spacing and channel are set with the SPACE[1:0] and CHAN[9:0] bits.
04h	15	RDSIEN	R/W	**RDS Interrupt Enable.** 0 = Disable Interrupt (default). 1 = Enable Interrupt. Setting RDSIEN = 1 and GPIO2[1:0] = 01 will generate a 5 ms low pulse on GPIO2 when the RDSR bit is set.
04h	14	STCIEN	R/W	**Seek/Tune Complete Interrupt Enable.** 0 = Disable Interrupt (default). 1 = Enable Interrupt. Setting STCIEN = 1 and GPIO2[1:0] = 01 will generate a 5 ms low pulse on GPIO2 when the STC bit is set.

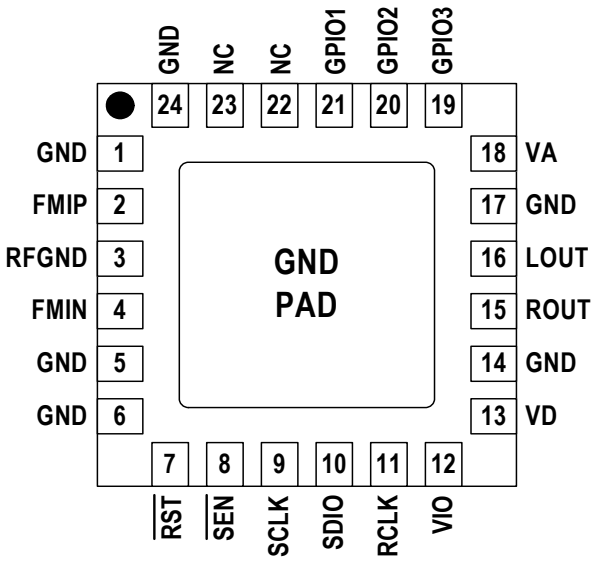
Reg	Bits	Name	Type	Description
04h	12	RDS	R/W	**RDS Enable.** 0 = Disable (default). 1 = Enable.
04h	11	DE	R/W	**De-emphasis.** 0 = 75 µs. Used in USA (default). 1 = 50 µs. Used in Europe, Australia, Japan.
04h	10	AGCD	R/W	**AGC Disable.** 0 = AGC enable (default). 1 = AGC disable.
04h	5:4	GPIO3[1:0]	R/W	**General Purpose I/O 3.** 00 = High impedance (default) 01 = Mono/Stereo indicator (ST) 10 = Low 11 = High
04h	3:2	GPIO2[1:0]	R/W	**General Purpose I/O 2.** 00 = High impedance (default) 01 = STC/RDS interrupt 10 = Low 11 = High Setting STCIEN = 1 will generate a 5 ms low pulse on GPIO2 when the STC bit is set. Setting RDSIEN = 1 will generate a 5 ms low pulse on GPIO2 when the RDSR bit is set.
04h	1:0	GPIO1[1:0]	R/W	**General Purpose I/O 1.** 00 = High impedance (default) 01 = Reserved 10 = Low 11 = High **Note:** GPIO1 should only be set to 11 = High if VIO < 2.4 V when the chip is enabled with ENABLE = 1.
05h	15:8	SEEKTH[7:0]	R/W	**Seek Threshold.** 0x00 = min RSSI (default) 0xFF = max RSSI RSSI scale is logarithmic. Settings of 19 for distant stations and 32 for local stations are recommended.
05h	7:6	BAND[1:0]	R/W	**Band Select.** 00 = 87.5–108 MHz (US/Europe, Default) 01 = 76–108 MHz (Japan wide band) 10 = 76–90 MHz (Japan) 11 = Reserved
05h	5:4	SPACE[1:0]	R/W	**Channel Spacing.** 00 = 200 kHz (USA, Australia) (default) 01 = 100 kHz (Europe, Japan) 10 = 50 kHz

Reg	Bits	Name	Type	Description
05h	3:0	VOLUME[3:0]	R/W	**Volume.** 0000 = min (default) 1111 = max Volume scale is logarithmic.
0Ah	15	RDSR	R	**RDS Ready.** 0 = No RDS group ready (default). 1 = New RDS group ready. Refer to “4.11. RDS/RBDS Processor and Functionality”.
0Ah	14	STC	R	**Seek/Tune Complete.** 0 = Not complete (default). 1 = Complete. The seek/tune complete flag is set when the seek or tune operation completes. Setting the SEEK or TUNE bit low will clear STC.
0Ah	13	SF/BL	R	**Seek Fail/Band Limit.** 0 = Seek successful. 1 = Seek failure/Band limit reached. The SF/BL flag is set high when SKMODE = 0 and the seek operation fails to find a channel with an RSSI level greater than SEEKTH[7:0]. The SF/BL flag is set high when SKMODE = 1 and the upper or lower band limit has been reached. The SEEK bit must be set low to clear SF/BL.
0A	12	AFCRL	R	**AFC Rail.** 0 = AFC not railed. 1 = AFC railed, indicating an invalid channel. AFCRL is updated after a tune or seek operation, during normal operation, and indicates an invalid channel.
0Ah	11	RDSS	R	**RDS Synchronized.** 0 = RDS decoder not synchronized (default). 1 = RDS decoder synchronized. Available only in RDS Verbose mode (RDSM = 1). Refer to “4.11. RDS/RBDS Processor and Functionality”.
0Ah	10:9	BLERA	R	**RDS Block A Errors.** 00 = 0 errors requiring correction. 01 = 1–2 errors requiring correction. 10 = 3–5 errors requiring correction. 11 = 6+ errors, correction not possible. Available only in RDS Verbose mode (RDSM = 1). Refer to “4.11. RDS/RBDS Processor and Functionality”.

Reg	Bits	Name	Type	Description
0Ah	11:9	RDSE[2:0]	R	**RDS Error.** Indicates the number of blocks containing errors in the current group contained in registers RDSA, RDSB, RDSC, and RDSD. 000 = 0 errors detected. 001 = errors detected in 1 block. 010 = errors detected in 2 blocks. 011 = errors detected in 3 blocks. 100 = errors detected in 4 blocks. Available only in RDS Standard mode (RDSM = 0). Refer to “4.11. RDS/RBDS Processor and Functionality”.
0Ah	8	ST	R	**Stereo Indicator.** 0 = Mono 1 = Stereo Stereo indication is also available on GPIO3 by setting GPIO3[1:0] = 01.
0Ah	7:0	RSSI[7:0]	R	**Received Signal Strength Indicator.** 0x00 = minimum signal strength. 0xFF = maximum signal strength. RSSI scale is logarithmic in dB.
0Bh	15:14	BLERB	R	**RDS Block B Errors.** 00 = 0 errors requiring correction. 01 = 1–2 errors requiring correction. 10 = 3–5 errors requiring correction. 11 = 6+ errors, correction not possible. Available only in RDS Standard mode (RDSM = 0). Refer to “4.11. RDS/RBDS Processor and Functionality”.
0Bh	13:12	BLERC	R	**RDS Block C Errors.** 00 = 0 errors requiring correction. 01 = 1–2 errors requiring correction. 10 = 3–5 errors requiring correction. 11 = 6+ errors, correction not possible. Available only in RDS Standard mode (RDSM = 0). Refer to “4.11. RDS/RBDS Processor and Functionality”.
0Bh	11:10	BLERD	R	**RDS Block D Errors.** 00 = 0 errors requiring correction. 01 = 1–2 errors requiring correction. 10 = 3–5 errors requiring correction. 11 = 6+ errors, correction not possible. Available only in RDS Standard mode (RDSM = 0). Refer to “4.11. RDS/RBDS Processor and Functionality”.

Reg	Bits	Name	Type	Description
0Bh	9:0	READCHAN[9:0]	R	**Read Channel.** BAND = 00 Freq (MHz) = Spacing (kHz) x Channel + 87.5 MHz BAND = 01, BAND = 10 Freq (MHz) = Spacing (kHz) x Channel + 76 MHz READCHAN[9:0] is updated during a seek operation and the final channel is updated after a seek operation completes (STC = 1). Spacing and channel are set with the SPACE[1:0] and CHAN[9:0] bits.
0Ch	15:0	RDSA	R	**RDS Block A Data.**
0Dh	15:0	RDSB	R	**RDS Block B Data.**
0Eh	15:0	RDSC	R	**RDS Block C Data.**
0Fh	15:0	RDSD	R	**RDS Block D Data.**

7. Pin Descriptions: Si4701-GM



Top View

Pin Number(s)	Name	Description
1, 5, 6, 14, 17, 24, GND PAD	GND	Ground. Connect to ground plane on PCB.
2, 4	FMIP, FMIN	FM RF inputs. For single-ended input, FMIN should be connected to RFGND.
3	RFGND	RF ground. Connect to ground plane on PCB.
7	$\overline{\text{RST}}$	Device reset (active low) input.
8	$\overline{\text{SEN}}$	Serial enable input (active low).
9	SCLK	Serial clock input.
10	SDIO	Serial data input/output.
11	RCLK	External reference oscillator input.
12	VIO	I/O supply voltage.
13	VD	Digital supply voltage. May be connected directly to battery.
15	ROUT	Right audio output.
16	LOUT	Left audio output.
18	VA	Analog supply voltage. May be connected directly to battery.
19–21	GPIO3, GPIO2, GPIO1	General purpose input/output.
22, 23	NC	No Connect. Leave floating.

8. Ordering Guide

Part Number*	Description	Package Type	Operating Temperature
Si4701-A14-GM	Portable Broadcast Radio Tuner FM Stereo Firmware Revision 14	QFN Lead-free	–20 to 85 °C
***Note:** Add an “(R)” at the end of the device part number to denote tape and reel option; 2500 quantity per reel.			

9. Package Outline: Si4701-GM

Figure 9 illustrates the package details for the Si4701-A14-GM. Table 8 lists the values for the dimensions shown in the illustration.

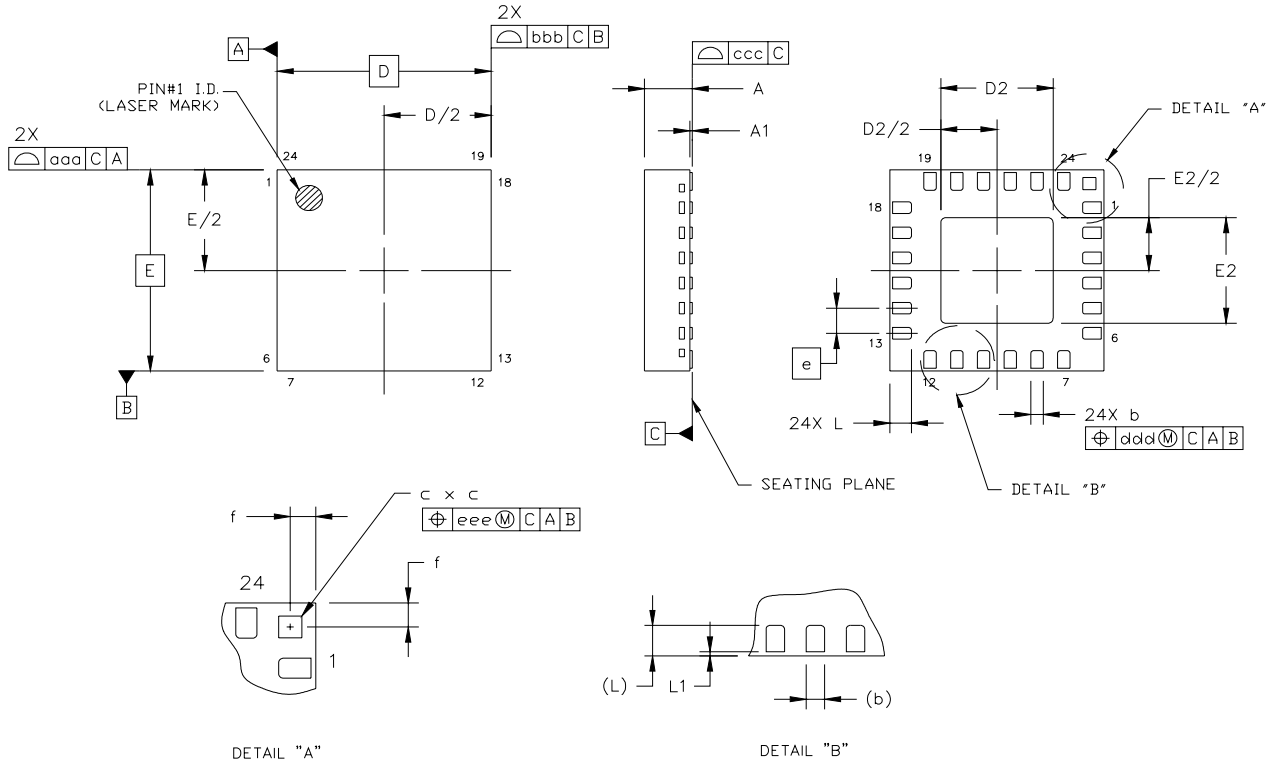


Figure 9. 24-Pin Quad Flat No-Lead (QFN)

Table 8. Package Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
c	0.19	0.24	0.29
D		4.00 BSC	
D2	2.00	2.10	2.20
e		0.50 BSC	
f		0.27 BSC	
E		4.00 BSC	

Symbol	Millimeters		
	Min	Nom	Max
E2	2.00	2.10	2.20
L	0.30	0.40	0.50
L1	0.03	0.05	0.08
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10

Notes:

1. All dimensions are shown in millimeters unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JECEC Solid State Outline MO-220, Variation VGGD-8.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.
5. Lead-free/RoHS compliant.

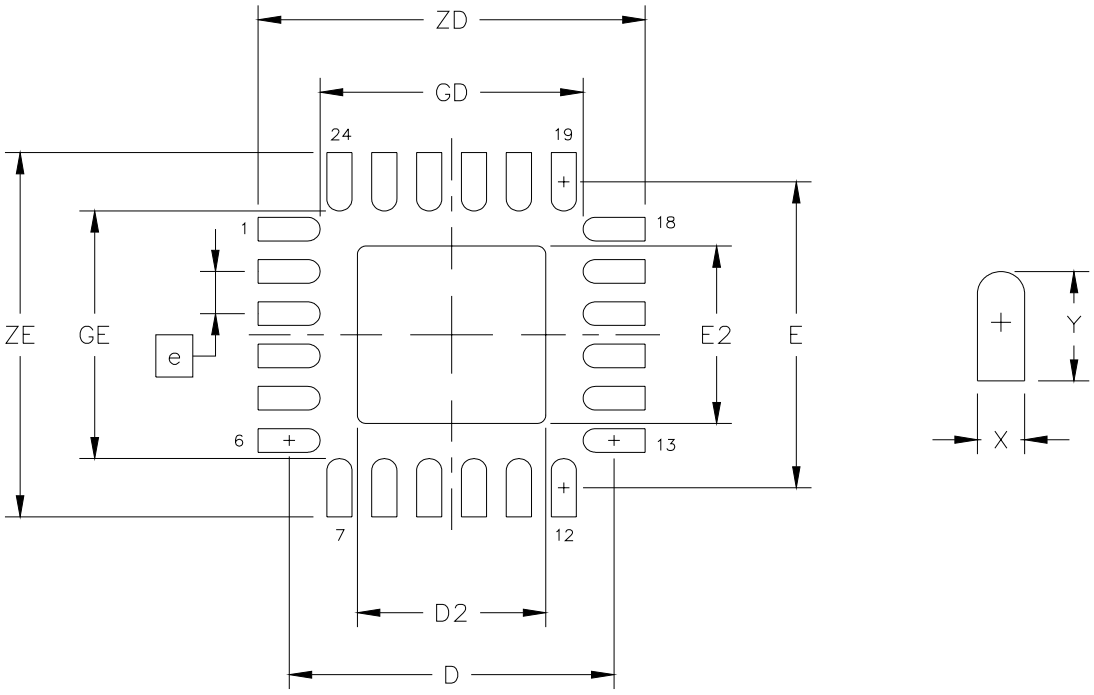


Figure 10. PCB Land Pattern

Table 9. Dimensions for PCB Land Pattern

Dimension	Min	Max
e	0.50 BSC.	
E	3.62 REF.	
D	3.62 REF.	
E2	2.00	2.20
D2	2.00	2.20
GE	2.93	—
GD	2.93	—
X	—	0.28
Y	0.69 REF.	
ZE	—	4.31
ZD	—	4.31

10. Additional Reference Resources

- AN230: Si4700/01 Programming Guide
- AN231: Si4700/01 Headphone and Antenna Interface
- AN232: Si4700/01 EVB User's Guide
- AN234: Si4700/01 EVB Test Procedure
- AN235: Si4700/01 EVB Quick Start Guide
- AN243: Using RDS/RBDS with the SI4701
- Si4700/01 Customer Support Site: http://www.mysilabs.com
  This site contains all application notes, evaluation board schematics and layouts, and evaluation software. NDA is required for access. To request access, register at http://www.mysilabs.com and send user's first and last name, company name, NDA reference number, and mysilabs user name to fminfo@silabs.com. Silicon Labs recommends an all lower case user name.

DOCUMENT CHANGE LIST

Revision 0.85 to Revision 0.86

- Updated Table 7 "FM Receiver Characteristics" on page 10.
  - Changed powerup time from 85 to 110 ms.
- Clarified and updated Section 4.11. "RDS/RBDS Processor and Functionality" on page 17.
- Updated 5. "Register Summary" on page 18.
  - Added footnote clarifying differences in RDS Verbose and Standard Mode bits.
- Updated 6. "Register Descriptions" on page 19.
  - Added note clarifying RDS Verbose and Standard Mode differences.
  - Added RDSE explanations.

Revision 0.86 to Revision 1.0

- Updated 4.11. "RDS/RBDS Processor and Functionality" on page 17 to include high RDS block error rate in Si4701-A14-GM. Issue is resolved in Si4701-B15-GM.
- Updated 5. "Register Summary" on page 18 for RDS block B, C, and D Errors to include "Available only in RDS standard mode (RDSM = 0)."
- Updated 10. "Additional Reference Resources" on page 29 to ask customers to provide user's first and last name, company name, and NDA reference number for access to the customer support site.

Revision 1.0 to Revision 1.1

- Added Notes 1 and 2 to page 1, with caution sign.
- Added Note 7 to page 12.

NOTES:

CONTACT INFORMATION

Silicon Laboratories Inc.

4635 Boston Lane
Austin, Texas 78735
Tel:1+ (512) 416-8500
Fax:1+ (512) 416-9669
Toll Free:1+ (877) 444-3032

Email: FMinfo@silabs.com
Internet: www.silabs.com