Si5322

Pin-Programmable Precision Clock Multiplier

Features

- Not recommended for new designs. For alternatives, see the Si533x family of products.
- Selectable output frequencies ranging from 19.44 to 1050 MHz
- Low jitter clock outputs with jitter generation as low as 0.6 ps_{RMS} (50 kHz–80 MHz)
- Integrated loop filter with selectable loop bandwidth (150 kHz to 1.3 MHz)
- Dual clock inputs with manual or automatically controlled switching
- Dual clock outputs with selectable signal format: LVPECL, LVDS, CML, CMOS
- Support for ITU G.709 FEC ratios (255/238, 255/237, 255/236)
- LOS alarm output
- Pin-programmable settings
- On-chip voltage regulator for 1.8 V ±5%, 2.5 or 3.3 V ±10% operation
- Small size: 6 x 6 mm 36-lead QFN
- Pb-free, RoHS compliant

Applications

- SONET/SDH OC-48/STM-16 and OC-192/STM-64 line cards
- GbE/10GbE, 1/2/4/8/10GFC line cards
- ITU G.709 line cards
- Optical modules
- Test and measurement

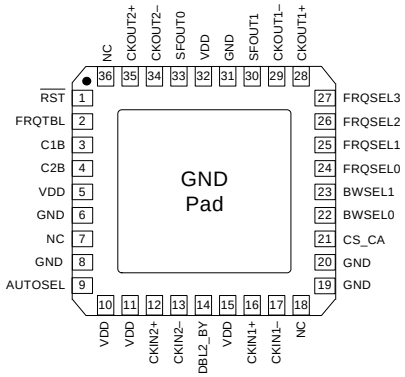
Description

The Si5322 is a low jitter, precision clock multiplier for high-speed communication systems, including SONET OC-48/OC-192, Ethernet, and Fibre Channel. The Si5322 accepts dual clock inputs ranging from 19.44 to 707 MHz and generates two equal frequency-multiplied clock outputs ranging from 19.44 to 1050 MHz. The input clock frequency and clock multiplication ratio are selectable from a table of popular SONET, Ethernet, and Fibre Channel rates. The Si5322 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides any-frequency synthesis in a highly-integrated PLL solution that eliminates the need for external VCXO and loop filter components. The DSPLL loop bandwidth is digitally programmable, providing jitter performance optimization at the application level. Operating from a single 1.8, 2.5, or 3.3 V supply, the Si5322 is ideal for providing clock multiplication in high performance timing applications.

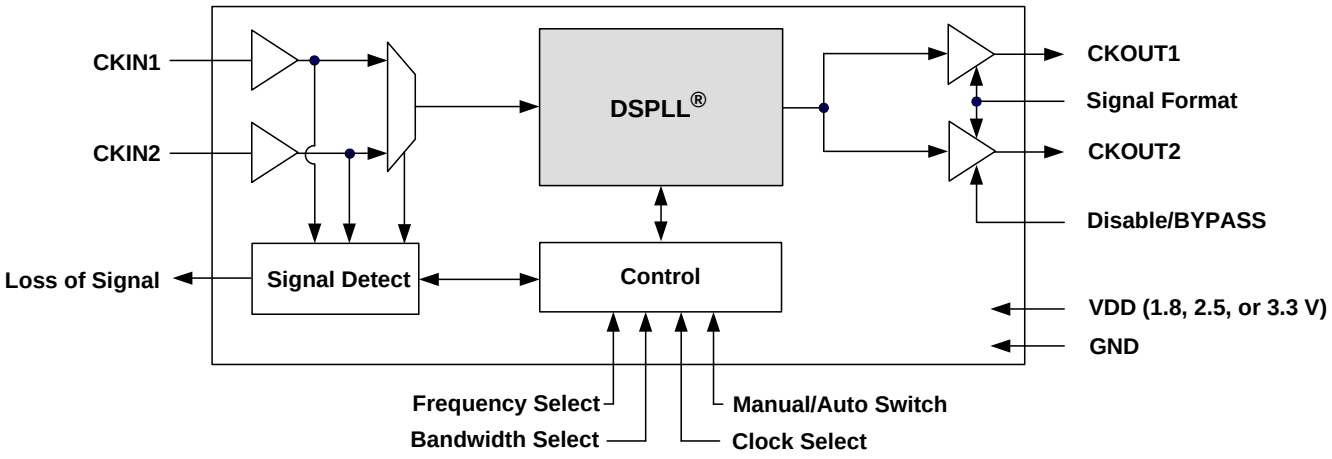
Ordering Information:

See page 18.

Pin Assignments



Functional Block Diagram



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1. Electrical Specifications

Table 1. Recommended Operating Conditions

(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Temperature Range	T_A		–40	25	85	ºC
Supply Voltage	V_{DD}	3.3 V nominal	2.97	3.3	3.63	V
		2.5 V nominal	2.25	2.5	2.75	V
		1.8 V nominal	1.71	1.8	1.89	V

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

Table 2. DC Characteristics

(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current (Supply current is independent of V_{DD})	I_{DD}	LVPECL Format 622.08 MHz Out All CKOUTs Enabled[1]	—	251	279	mA
		LVPECL Format 622.08 MHz Out Only 1 CKOUT Enabled[1]	—	217	243	mA
		CMOS Format 19.44 MHz Out All CKOUTs Enabled	—	204	234	mA
		CMOS Format 19.44 MHz Out Only CKOUT1 Enabled	—	194	220	mA
CKIN Input Pins						
Input Common Mode Voltage (Input Threshold Voltage)	V_{ICM}	1.8 V ±5%	0.9	—	1.4	V
		2.5 V ±10%	1.0	—	1.7	V
		3.3 V ±10%	1.1	—	1.95	V
Input Resistance	CKN_{RIN}	Single-ended	20	40	60	kΩ
Input Voltage Level Limits	CKN_{VIN}	See Note [2]	0	—	V_{DD}	V
Single-Ended Input Voltage Swing	V_{ISE}	$f_{CKIN} \leq$ 212.5 MHz See Figure 2.	0.2	—	—	V_{PP}
		f_{CKIN} > 212.5 MHz See Figure 2.	0.25	—	—	V_{PP}

Notes:
1. LVPECL outputs require nominal $V_{DD} \geq$ 2.5 V.
2. No overshoot or undershoot.
3. This is the amount of leakage that the 3L inputs can tolerate from an external driver. See Figure 3 on page 9. In most designs, an external resistor voltage divider is recommended.

Table 2. DC Characteristics (Continued)
(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential Input Voltage Swing	V_{ID}	$f_{CKIN} \leq$ 212.5 MHz See Figure 2.	0.2	—	—	V_{PP}
		f_{CKIN} > 212.5 MHz See Figure 2.	0.25	—	—	V_{PP}
Output Clocks (CKOUTn)[1]						
Common Mode	CKO_{VCM}	LVPECL 100 Ω load line-to-line	V_{DD} – 1.42	—	V_{DD} – 1.25	V
Differential Output Swing	CKO_{VD}	LVPECL 100 Ω load line-to-line	1.1	—	1.9	V_{PP}
Single-ended Output Swing	CKO_{VSE}	LVPECL 100 Ω load line-to-line	0.5	—	0.93	V_{PP}
Differential Output Voltage	CKO_{VD}	CML 100 Ω load line-to-line	350	425	500	mV_{PP}
Common Mode Output Voltage	CKO_{VCM}	CML 100 Ω load line-to-line	—	V_{DD} – 0.36	—	V
Differential Output Voltage	CKO_{VD}	LVDS 100 Ω load line-to-line	500	700	900	mV_{PP}
		Low swing LVDS 100 Ω load line-to-line	350	425	500	mV_{PP}
Common Mode Output Voltage	CKO_{VCM}	LVDS 100 Ω load line-to-line	1.125	1.2	1.275	V
Differential Output Resistance	CKO_{RD}	CML, LVDS, LVPECL	—	200	—	Ω
Output Voltage Low	CKO_{VOLLH}	CMOS	—	—	0.4	V
Output Voltage High	CKO_{VOHLH}	V_{DD} = 1.71 V CMOS	0.8 x V_{DD}	—	—	V
Output Drive Current	CKO_{IO}	CMOS Driving into CKO_{VOL} for output low or CKO_{VOH} for output high. CKOUT+ and CKOUT– shorted externally.				
		V_{DD} = 1.8 V	—	7.5	—	mA
		V_{DD} = 3.3 V	—	32	—	mA

Notes:
1. LVPECL outputs require nominal $V_{DD} \geq$ 2.5 V.
2. No overshoot or undershoot.
3. This is the amount of leakage that the 3L inputs can tolerate from an external driver. See Figure 3 on page 9. In most designs, an external resistor voltage divider is recommended.

Table 2. DC Characteristics (Continued)
(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
2-Level LVCMOS Input Pins						
Input Voltage Low	V_{IL}	V_{DD} = 1.71 V	—	—	0.5	V
		V_{DD} = 2.25 V	—	—	0.7	V
		V_{DD} = 2.97 V	—	—	0.8	V
Input Voltage High	V_{IH}	V_{DD} = 1.89 V	1.4	—	—	V
		V_{DD} = 2.25 V	1.8	—	—	V
		V_{DD} = 3.63 V	2.5	—	—	V
Input Low Current	I_{IL}		—	—	50	µA
Input High Current	I_{IH}		—	—	50	µA
Weak Internal Input Pull-up Resistor	R_{PUP}		—	75	—	kΩ
Weak Internal Input Pull-down Resistor	R_{PDN}		—	75	—	kΩ
3-Level Input Pins						
Input Voltage Low	V_{ILL}		—	—	0.15 x V_{DD}	V
Input Voltage Mid	V_{IMM}		0.45 x V_{DD}	—	0.55 x V_{DD}	V
Input Voltage High	V_{IHH}		0.85 x V_{DD}	—	—	V
Input Low Current	I_{ILL}[3]		–20	—	—	µA
Input Mid Current	I_{IMM}[3]		–2	—	2	µA
Input High Current	I_{IHH}[3]		—	—	20	µA

Notes:
1. LVPECL outputs require nominal $V_{DD} \geq 2.5$ V.
2. No overshoot or undershoot.
3. This is the amount of leakage that the 3L inputs can tolerate from an external driver. See Figure 3 on page 9. In most designs, an external resistor voltage divider is recommended.

Table 2. DC Characteristics (Continued)
(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
LVCMOS Output Pins						
Output Voltage Low	V_{OL}	I_O = 2 mA V_{DD} = 1.71 V	—	—	0.4	V
		I_O = 2 mA V_{DD} = 2.97 V	—	—	0.4	V
Output Voltage High	V_{OH}	I_O = –2 mA V_{DD} = 1.71 V	V_{DD} – 0.4	—	—	V
		I_O = –2 mA V_{DD} = 2.97 V	V_{DD} – 0.4	—	—	V
Disabled Leakage Current	I_{OZ}	$\overline{RST}$ = 0	–100	—	100	µA

Notes:
1. LVPECL outputs require nominal $V_{DD} \geq 2.5$ V.
2. No overshoot or undershoot.
3. This is the amount of leakage that the 3L inputs can tolerate from an external driver. See Figure 3 on page 9. In most designs, an external resistor voltage divider is recommended.

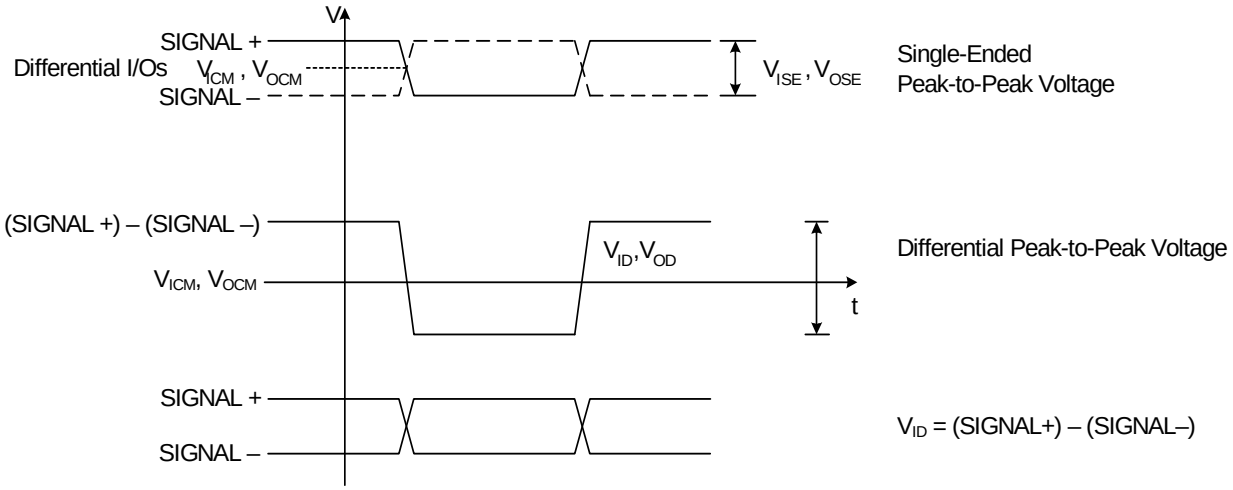


Figure 1. Voltage Characteristics

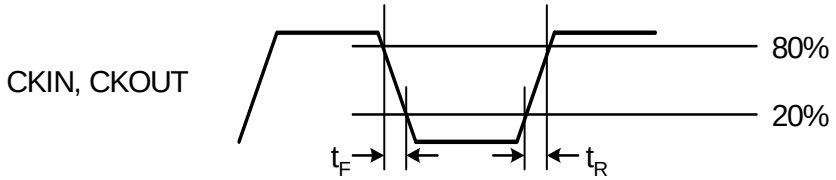


Figure 2. Rise/Fall Time Characteristics

Table 3. AC Characteristics

(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
CKIN Input Pins						
Input Frequency	CKN_F		19.44	—	707.35	MHz
Input Duty Cycle (Minimum Pulse Width)	CKN_{DC}	Whichever is smaller (i.e., the 40%/60% limitation applies only to high clock frequencies)	40	—	60	%
			2	—	—	ns
Input Capacitance	CKN_{CIN}		—	—	3	pF
Input Rise/Fall Time	CKN_{TRF}	20–80% See Figure 2	—	—	11	ns
CKOUTn Output Pins						
Output Frequency (Output not configured for CMOS or disable)	CK_{OF}		19.44	—	1050	MHz
Maximum Output Frequency in CMOS Format	CKO_{FMC}		—	—	212.5	MHz
Single-ended Output Rise/Fall (20–80%)	CKO_{TRF}	CMOS Output V_{DD} = 1.71 Cload = 5 pF	—	—	8	ns
		CMOS Output V_{DD} = 2.97 Cload = 5 pF	—	—	2	ns
Differential Output Rise/Fall Time	CKO_{TRF}	20 to 80 %, f_{OUT} = 622.08	—	230	350	ps
Output Duty Cycle Differential Uncertainty	CKO_{DC}	100 Ω Load Line to Line Measured at 50% Point (not for CMOS)	—	—	±40	ps
LVCMOS Input Pins						
Minimum Reset Pulse Width	t_{RSTMIN}		1	—	—	µs
Input Capacitance	C_{IN}		—	—	3	pF
LVCMOS Output Pins						
Rise/Fall Times	t_{RF}	C_{LOAD} = 20 pf See Figure 2	—	25	—	ns
LOSn Trigger Window	LOS_{TRIG}	From last CKIN↑ to LOS↑		—	750	µs
PLL Performance						
Output Clock Phase Change	t_{P_STEP}	After clock switch f3 ≥ 128 kHz	—	200	—	ps
Closed Loop Jitter Peaking	J_{PK}		—	0.05	0.1	dB
Jitter Tolerance	J_{TOL}	BW determined by BWSEL[1:0]	5000/ BW	—	—	ns pk-pk
Spurious Noise	SP_{SPUR}	Max spur @ n x f3 (n ≥ 1, n x f3 < 100 MHz)	—	–93	–70	dBc
Phase Change due to Temperature Variation	t_{TEMP}	Max phase changes from –40 to +85 ºC	—	300	500	ps

1.1. Three-Level (3L) Input Pins (No External Resistors)

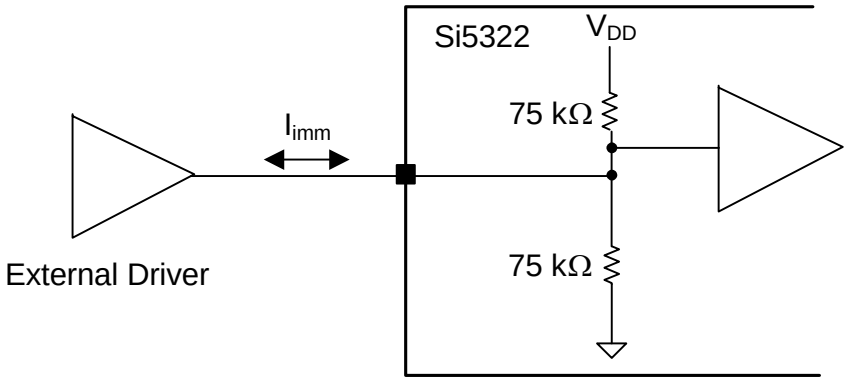
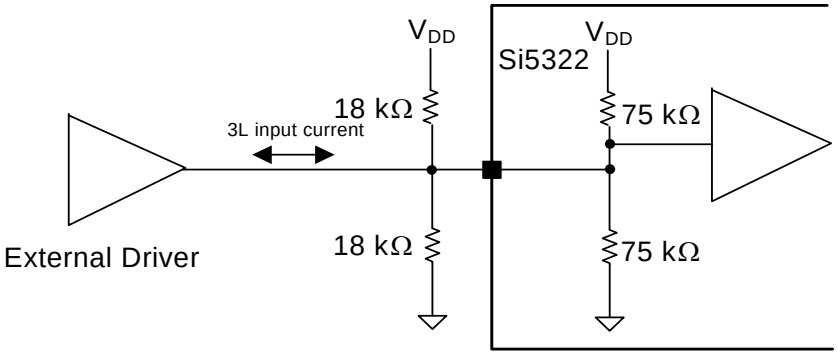


Figure 3. Three-Level Input Pins

1.2. Three-Level Input Pins (Example with External Resistors)



One of eight resistors from a Panasonic EXB-D10C183J (or similar) resistor pack

Figure 4. Three-Level Input Pins

Table 4. Three-Level Input Pins[1,2,3,4]

Parameter	Min	Max
Input Low Current	–30 µA	—
Input Mid Current	–11 µA	–11 µA
Input High Current	—	–30 µA

Notes:
1. The current parameters are the amount of leakage that the 3L inputs can tolerate from an external driver using the external resistor values indicated in this example. In most designs, an external resistor voltage divider is recommended.
2. Resistor packs are only needed if the leakage current of the external driver exceeds the current specified in Table 2, Iimm. Any resistor pack may be used (e.g., Panasonic EXB-D10C183J). PCB layout is not critical.
3. If a pin is tied to ground or V_{DD}, no resistors are needed.
4. If a pin is left open (no connect), no resistors are needed.

Table 5. Performance Specifications[1, 2, 3, 4]

(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Jitter Generation f_{IN} = f_{OUT} = 622.08 MHz, LVPECL Output Format BW = 877 Hz	J_{GEN}	50 kHz–80 MHz	—	.47	—	ps rms
		12 kHz–20 MHz	—	.48	—	ps rms
		4 MHz–80 MHz	—	.23	—	ps rms
Phase Noise f_{IN} = f_{OUT} = 622.08 MHz LVPECL Output Format	CKO_{PN}	1 kHz offset	—	–90	—	dBc/Hz
		10 kHz offset	—	–113	—	dBc/Hz
		100 kHz offset	—	–118	—	dBc/Hz
		1 MHz offset	—	–132	—	dBc/Hz

Notes:
1. BWSEL [1:0] loop bandwidth settings provided in by DSPLLsim.
2. V_{DD} = 3.3 V
3. T_A = 85 °C
4. Test condition: f_{IN} = 622.08 MHz, f_{OUT} = 622.08 MHz, LVPECL clock input: 1.19 Vppd with 0.5 ns rise/fall time (20-80%), LVPECL clock output.

Table 6. Thermal Characteristics

(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	—	32	—	ºC/W
Thermal Resistance Junction to Case	θ_{JC}	Still Air	—	14	—	ºC/W

Table 7. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	–0.5 to 3.8	V
LVCMOS Input Voltage	V_{DIG}	–0.3 to (V_{DD} + 0.3)	V
CKINn Voltage Level Limits	CKN_{VIN}	0 to V_{DD}	V
Operating Junction Temperature	T_{JCT}	–55 to 150	C
Storage Temperature Range	T_{STG}	–55 to 150	C
ESD HBM Tolerance (100 pF, 1.5 kΩ); All pins except CKIN+/CKIN–		2	kV
ESD MM Tolerance; All pins except CKIN+/CKIN–		150	V
ESD HBM Tolerance (100 pF, 1.5 kΩ); CKIN+/CKIN–		750	V
ESD MM Tolerance; CKIN+/CKIN–		100	V
Latch-Up Tolerance		JESD78 Compliant	

Note: Permanent device damage may occur if the Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

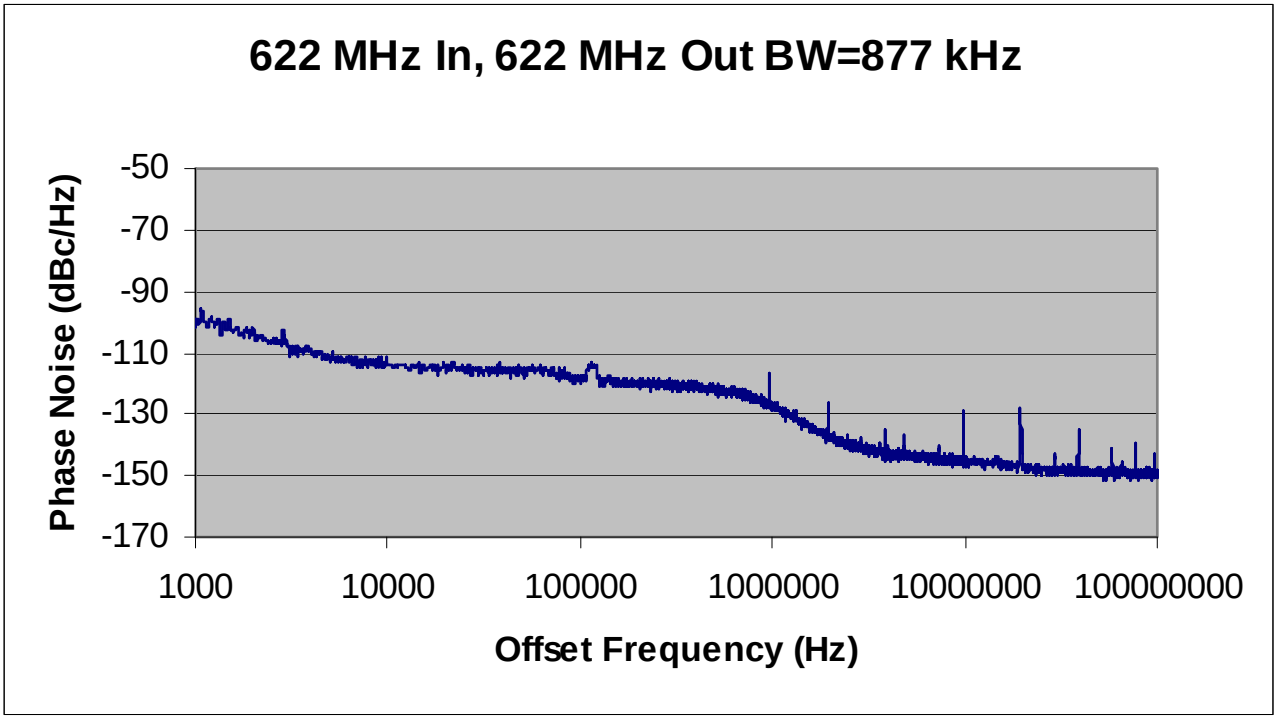
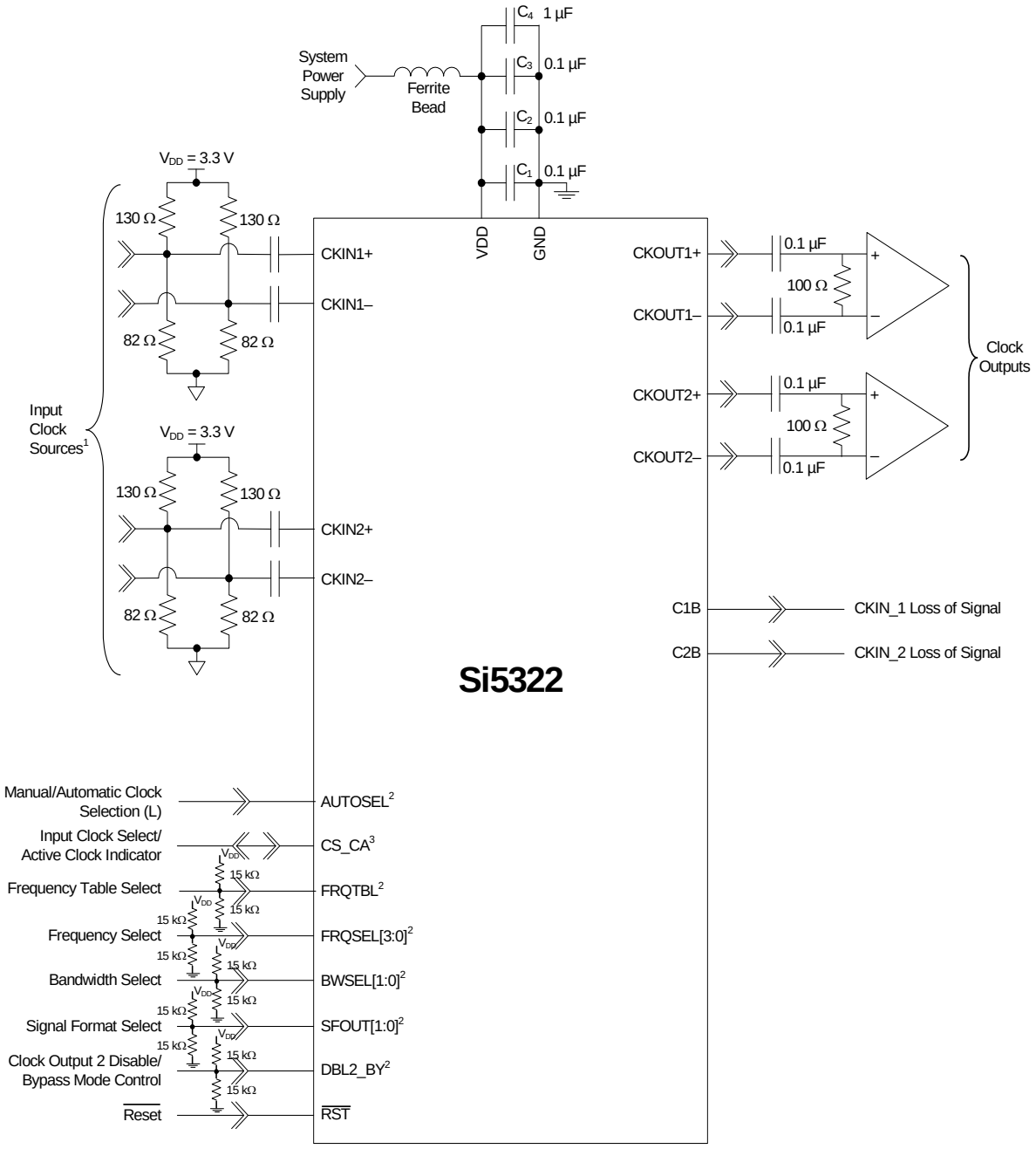


Figure 5. Typical Phase Noise Plot

Table 8. Typical Jitter Data

Jitter Bandwidth	RMS Jitter (fs)
OC-48, 12 kHz to 20 MHz	374
OC-192, 20 kHz to 80 MHz	388
OC-192, 4 MHz to 80 MHz	181
OC-192, 50 kHz to 80 MHz	377
Broadband, 800 Hz to 80 MHz	420



Notes: 1. Assumes differential LVEPECL termination (3.3 V) on clock inputs.
2. Denotes tri-level input pins with states designated as L (ground), M (V_{DD}/2), and H (V_{DD}).
3. Assumes manual input clock selection.

Figure 6. Si5322 Typical Application Circuit

2. Functional Description

The Si5322 is a low jitter, precision clock multiplier for high-speed communication systems, including SONET OC-48/OC-192, SDH STM-16/64 Ethernet, and Fibre Channel. The Si5322 accepts dual clock inputs ranging from 19.44 to 707 MHz and generates two frequency-multiplied clock outputs ranging from 19.44 to 1050 MHz. The two input clocks are at the same frequency and the two output clocks are at the same frequency. The input clock frequency and clock multiplication ratio are selectable from a table of popular SONET, Ethernet, and Fibre Channel rates. In addition to providing clock multiplication in SONET and datacom applications, the Si5322 supports SONET-to-datacom frequency translations. Silicon Laboratories offers a PC-based software utility, DSPLL*sim*, that can be used to look up valid Si5322 frequency translations. This utility can be downloaded from http://www.silabs.com/timing (click on Documentation).

The Si5322 is recommended for applications in which the input clock is relatively low jitter and only clock multiplication is required. The Si5322 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides any-frequency synthesis in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The Si5322 PLL loop bandwidth is selectable via the BWSEL[1:0] pins and supports a range from 150 kHz to 1.5 MHz. The DSPLL*sim* software utility can be used to calculate valid loop bandwidth settings for a given input clock frequency/clock multiplication ratio. The Si5322 monitors all input clocks for loss of signal and provides a LOS alarm when it detects a missing clock.

In the case when the input clocks enter alarm conditions, the PLL will freeze the DCO output frequency near its last value to maintain operation with an internal state close to the last valid operating state.

The Si5322 has two differential clock outputs. The electrical format of the clock outputs is programmable to support LVPECL, LVDS, CML, or CMOS loads. If not required, the second clock output can be powered down to minimize power consumption. For system-level debugging, a bypass mode is available which drives the output clock directly from the input clock, bypassing the internal DSPLL. The device is powered by a single 1.8, 2.5, or 3.3 V supply.

2.1. Further Documentation

Consult the Silicon Laboratories Any-Frequency Precision Clock Family Reference Manual (FRM) for detailed information about the Si5322. Additional design support is available from Silicon Laboratories through your distributor.

Silicon Laboratories has developed a PC-based software utility called DSPLL*sim* to simplify device configuration, including frequency planning and loop bandwidth selection. The FRM and this utility can be downloaded from http://www.silabs.com/timing; click on Documentation.

3. Pin Descriptions: Si5322

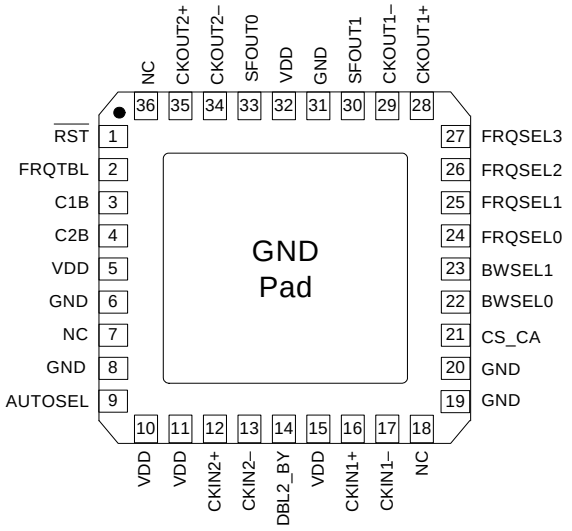


Table 9. Si5322 Pin Descriptions

Pin #	Pin Name	I/O	Signal Level	Description
1	$\overline{\text{RST}}$	I	LVCMOS	**External Reset.** Active low input that performs external hardware reset of device. Resets all internal logic to a known state. Clock outputs are tristated during reset. After rising edge of $\overline{\text{RST}}$ signal, the Si5322 will perform an internal self-calibration. This pin has a weak pull-up.
2	FRQTBL	I	3-Level	**Frequency Table Select.** Selects SONET/SDH, datacom, or SONET/SDH to datacom frequency table. L = SONET/SDH. M = Datacom. H = SONET/SDH to Datacom. The pin has a weak pull-up and weak pull-down and defaults to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
3	C1B	O	LVCMOS	**CKIN1 Loss of Signal.** Active high loss-of-signal indicator for CKIN1. Once triggered, the alarm will remain active until CKIN1 is validated. 0 = CKIN1 present. 1 = LOS on CKIN1.
4	C2B	O	LVCMOS	**CKIN2 Loss of Signal.** Active high loss-of-signal indicator for CKIN2. Once triggered, the alarm will remain active until CKIN2 is validated. 0 = CKIN2 present. 1 = LOS on CKIN2.

Table 9. Si5322 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
5, 10, 11, 15, 32	V_{DD}	V_{DD}	Supply	**Supply.** The device operates from a 1.8, 2.5, or 3.3 V supply. Bypass capacitors should be associated with the following V_{DD} pins: 5 0.1 µF 10 0.1 µF 32 0.1 µF A 1.0 µF should be placed as close to device as is practical.
6, 8,19, 20, 31	GND	GND	Supply	**Ground.** Must be connected to system ground. Minimize the ground path impedance for optimal performance of this device.
9	AUTOSEL	I	3-Level	**Manual/Automatic Clock Selection.** Three level input that selects the method of input clock selection to be used. L = Manual. M = Automatic non-revertive. H = Automatic revertive. The pin has a weak pull-up and weak pull-down and defaults to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
12 13	CKIN2+ CKIN2–	I	Multi	**Clock Input 2.** Differential input clock. This input can also be driven with a single-ended signal. Input frequency selected from a table of values. The same frequency must be applied to CKIN1 and CKIN2.
14	DBL2_BY	I	3-Level	**Output 2 Disable/Bypass Mode Control.** Controls enable of CKOUT2 divider/output buffer path and PLL bypass mode. L = CKOUT2 enabled. M = CKOUT2 disabled. H = Bypass mode with CKOUT2 enabled. CMOS outputs do not support Bypass Mode. The pin has a weak pull-up and weak pull-down and defaults to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
16 17	CKIN1+ CKIN1–	I	Multi	**Clock Input 1.** Differential input clock. This input can also be driven with a single-ended signal. Input frequency selected from a table of values. The same frequency must be applied to CKIN1 and CKIN2.

Table 9. Si5322 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
21	CS_CA	I/O	LVCMOS	**Input Clock Select/Active Clock Indicator.** **Input**: If manual clock selection mode is chosen (AUTOSEL = L), this pin functions as the manual input clock selector. This input is internally deglitched to prevent inadvertent clock switching during changes in the CS input state. 0 = Select CKIN1. 1 = Select CKIN2. If configured as input, must be set high or low. **Output**: If automatic clock selection mode is chosen (AUTOSEL = M or H), this pin indicates which of the two input clocks is currently the active clock. If alarms exist on both CKIN1 and CKIN2, indicating that the digital hold state has been entered, CA will indicate the last active clock that was used before entering the hold state. 0 = CKIN1 active input clock. 1 = CKIN2 active input clock.
23 22	BWSEL1 BWSEL0	I	3-Level	**Bandwidth Select.** Three level inputs that select the DSPLL closed loop bandwidth. Detailed operations and timing characteristics for these pins may be found in the Any-Frequency Precision Clock Family Reference Manual. These pins have both weak pull-ups and weak pull-downs and default to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.
27 26 25 24	FRQSEL3 FRQSEL2 FRQSEL1 FRQSEL0	I	3-Level	**Multiplier Select.** Three level inputs that select the input clock and clock multiplication ratio, depending on the FRQTBL setting. Consult the Any-Frequency Precision Clock Family Reference Manual or DSPLL*sim* configuration software for settings, both available for download at www.silabs.com/timing (click on Documentation). These pins have both weak pull-ups and weak pull-downs and default to M. Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.

Table 9. Si5322 Pin Descriptions (Continued)

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>I/O</th><th>Signal Level</th><th>Description</th></tr>
<tr><td>33
30</td><td>SFOUT0
SFOUT1</td><td>I</td><td>3-Level</td><td>Signal Format Select.
Three level inputs that select the output signal format (common mode voltage and differential swing) for both CKOUT1 and CKOUT2. Valid settings include LVPECL, LVDS, and CML. Also includes selections for CMOS mode, tristate mode, and tristate/sleep mode.
<table>
<tr><th>SFOUT[1:0]</th><th>Signal Format</th></tr>
<tr><td>HH</td><td>Reserved</td></tr>
<tr><td>HM</td><td>LVDS</td></tr>
<tr><td>HL</td><td>CML</td></tr>
<tr><td>MH</td><td>LVPECL</td></tr>
<tr><td>MM</td><td>Reserved</td></tr>
<tr><td>ML</td><td>LVDS—Low Swing</td></tr>
<tr><td>LH</td><td>CMOS</td></tr>
<tr><td>LM</td><td>Disabled</td></tr>
<tr><td>LL</td><td>Reserved</td></tr>
</table>
CMOS outputs do not support Bypass Mode.
These pins have both weak pull-ups and weak pull-downs and default to M.
Some designs may require an external resistor voltage divider when driven by an active device that will tri-state.</td></tr>
<tr><td>34
35</td><td>CKOUT2–
CKOUT2+</td><td>O</td><td>Multi</td><td>Clock Output 2.
Differential output clock with a frequency selected from a table of values. Output signal format is selected by SFOUT pins. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.</td></tr>
<tr><td>29
28</td><td>CKOUT1–
CKOUT1+</td><td>O</td><td>Multi</td><td>Clock Output 1.
Differential output clock with a frequency selected from a table of values. Output signal format is selected by SFOUT pins. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.</td></tr>
<tr><td>7, 18, 36</td><td>NC</td><td>—</td><td>—</td><td>No Connect.
These pins must be left unconnected for normal operation.</td></tr>
<tr><td>GND PAD</td><td>GND</td><td>GND</td><td>Supply</td><td>Ground Pad.
The ground pad must provide a low thermal and electrical impedance to a ground plane.</td></tr>
</table>

4. Ordering Guide

Ordering Part Number	Package	ROHS6, Pb-Free	Temperature Range
Si5322-C-GM*	36-Lead 6 x 6 mm QFN	Yes	–40 to 85 °C
***Note:** Not recommended for new designs. For alternatives, see the Si533x family.			

5. Package Outline: 36-Pin QFN

Figure 7 illustrates the package details for the Si5322. Table 10 lists the values for the dimensions shown in the illustration.

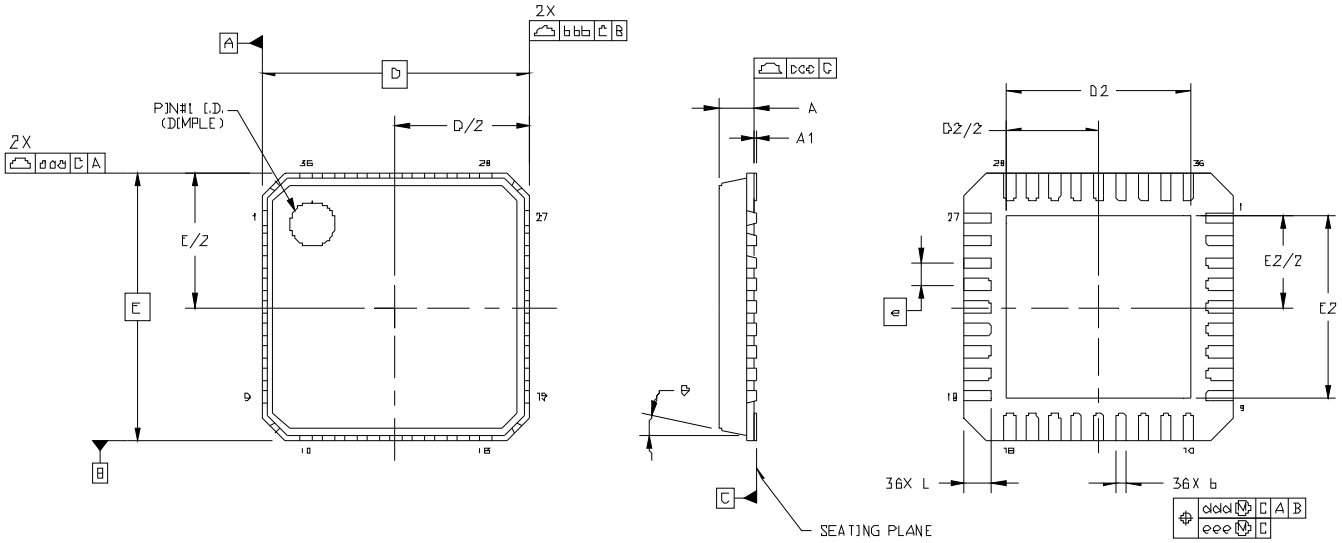


Figure 7. 36-Pin Quad Flat No-lead (QFN)

Table 10. Package Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		6.00 BSC	
D2	3.95	4.10	4.25
e		0.50 BSC	
E		6.00 BSC	
E2	3.95	4.10	4.25

Symbol	Millimeters		
	Min	Nom	Max
L	0.50	0.60	0.70
θ	—	—	12º
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.05

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220, variation VJJD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

6. Land Pattern: 36-Pin QFN

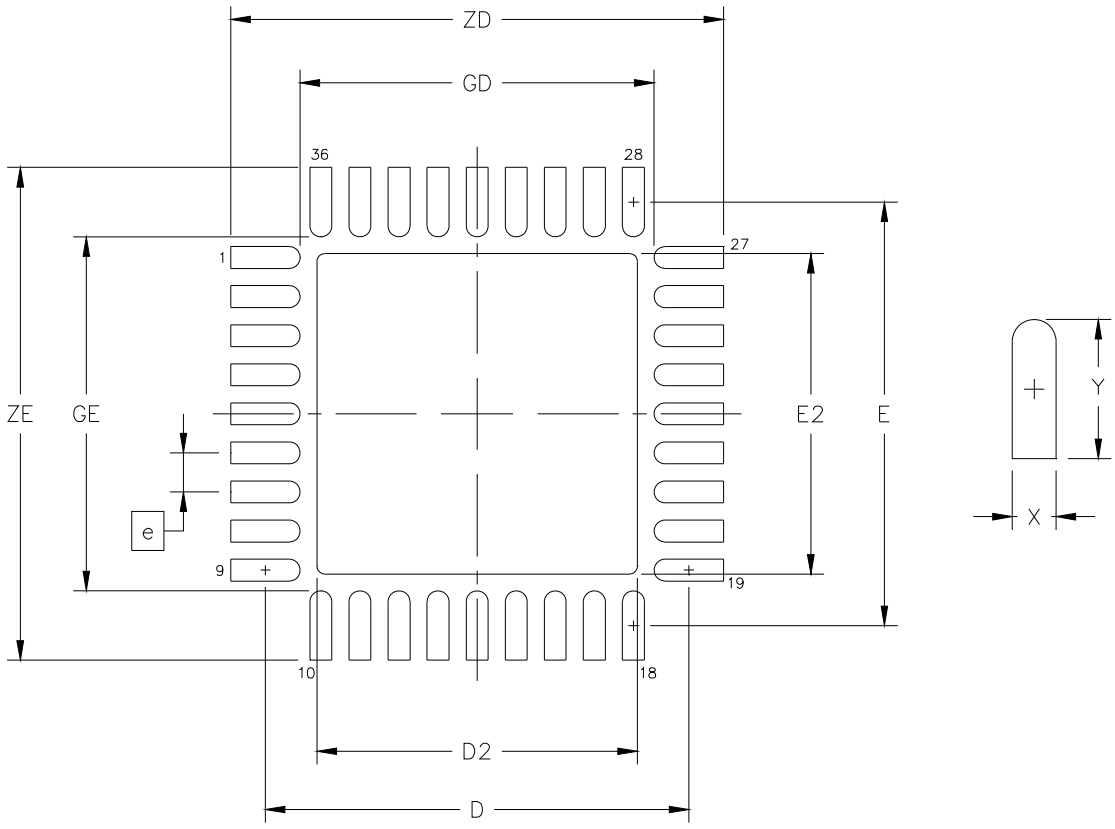


Figure 8. 36-Pin QFN Land Pattern

Table 11. PCB Land Pattern Dimensions

Dimension	MIN	MAX
e	0.50 BSC.	
E	5.42 REF.	
D	5.42 REF.	
E2	4.00	4.20
D2	4.00	4.20
GE	4.53	—
GD	4.53	—
X	—	0.28
Y	0.89 REF.	
ZE	—	6.31
ZD	—	6.31

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

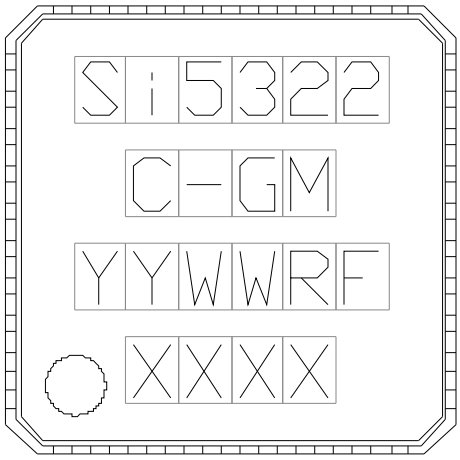
6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
9. A 4 x 4 array of 0.80 mm square openings on 1.05 mm pitch should be used for the center ground pad.

Card Assembly

10. A No-Clean, Type-3 solder paste is recommended.
11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

7. Top Marking

7.1. Si5322 Top Marking (QFN)



7.2. Top Marking Explanation

Mark Method:	Laser	
Font Size:	0.80 mm Right-Justified	
Line 1 Marking:	Si5322	Customer Part Number See Ordering Guide for options
Line 2 Marking:	C-GM	C = Product Revision G = Temperature Range –40 to 85 °C (RoHS6) M = QFN Package
Line 3 Marking:	YYWWRF	YY = Year WW = Work Week R = Die Revision F = Internal code Assigned by the Assembly House. Corresponds to the year and work week of the mold date.
Line 4 Marking:	Pin 1 Identifier	Circle = 0.75 mm Diameter Lower-Left Justified
	XXXX	Internal Code

Document Change List

Revision 0.44 to Revision 0.45

- Condensed format.

Revision 0.45 to Revision 0.46

- Removed references to latency control, INC, and DEC in figures and text.
- Changed LVTTL to LVCMOS in Table 2, “Absolute Maximum Ratings,” on page 5.
- Added Figure 1, “Typical Phase Noise Plot,” on page 4.
- Updated “3. Pin Descriptions: Si5322”.
- Added “6. Land Pattern: 36-Pin QFN”.

Revision 0.46 to Revision 0.47

- Removed Figure 1. “Typical Phase Noise Plot.”
- Changed pins 11 and 15 from NC to VDD in “3. Pin Descriptions: Si5322”.

Revision 0.47 to Revision 0.5

- Changed 1.8 V operating range to ±5%.
- Updated Table 1 on page 4.
- Updated Table 2 on page 5.
- Updated Figure 6 on page 12 to add pull-up/pull-down resistors for 3-level inputs.
- Added figure and table on page 11.
- Updated "2. Functional Description" on page 13.
- Clarified "3. Pin Descriptions: Si5322" on page 14.
- Updated SFOUT values.

Revision 0.5 to Revision 0.51

- Changed “any-rate” to “any-frequency” throughout.
- Expanded spec tables 1 through 7.
- Updated Table 5 on page 10.
- Added "7. Top Marking" on page 22.
- Added clarification that CMOS output format is not available in PLL bypass mode.
- Updated "4. Ordering Guide" on page 18.
- Removed note from "3. Pin Descriptions: Si5322" on page 14.

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