

## P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY		
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)
- 20	0.027 at V <sub>GS</sub> = - 4.5 V	- 8.2
	0.032 at V <sub>GS</sub> = - 2.5 V	- 7.5
	0.045 at V <sub>GS</sub> = - 1.8 V	- 6.6

### FEATURES

- Halogen-free according to IEC 61249-2-21 Definition
- TrenchFET<sup>®</sup> Power MOSFET
- MICRO FOOT<sup>®</sup> Chipscale Packaging  
Reduces Ultra-Low Footprint Area Profile (0.62 mm) and On-Resistance
- Compliant to RoHS Directive 2002/95/EC

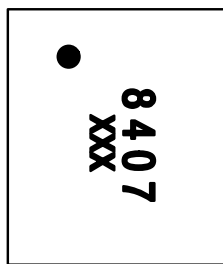
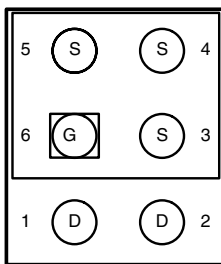


**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### MICRO FOOT

Bump Side View

Backside View

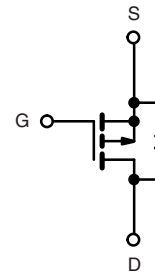


Device Marking: 8407  
xxx = Date/Lot Traceability Code

Ordering Information: Si8407DB-T2-E1 (Lead (Pb)-free and Halogen-free)

### APPLICATIONS

- Portable Devices
  - PA Switch
  - Battery Switch
  - Load Switch



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)				
Parameter	Symbol	5 s	Steady State	Unit
Drain-Source Voltage	V <sub>DS</sub>	- 20		V
Gate-Source Voltage	V <sub>GS</sub>	± 8		
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a</sup>	I <sub>D</sub>	T <sub>A</sub> = 25 °C	- 8.2	- 5.8
		T <sub>A</sub> = 70 °C	- 6.5	- 4.6
Pulsed Drain Current	I <sub>DM</sub>	- 15		A
Continuous Source Current (Diode Conduction) <sup>a</sup>	I <sub>S</sub>	- 2.6	- 1.34	
Maximum Power Dissipation <sup>a</sup>	P <sub>D</sub>	T <sub>A</sub> = 25 °C	2.9	1.47
		T <sub>A</sub> = 70 °C	1.86	0.94
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C
Package Reflow Conditions <sup>b</sup>	IR/Convection	260		

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>a</sup>	R <sub>thJA</sub>	t ≤ 5 s	33	43	°C/W
		Steady State	72	85	
Maximum Junction-to-Foot (drain)	R <sub>thJF</sub>	15	19		

Notes:

- Surface mounted on 1" x 1" FR4 board.
- Refer to IPC/JEDEC (J-STD-020), no manual or hand soldering.



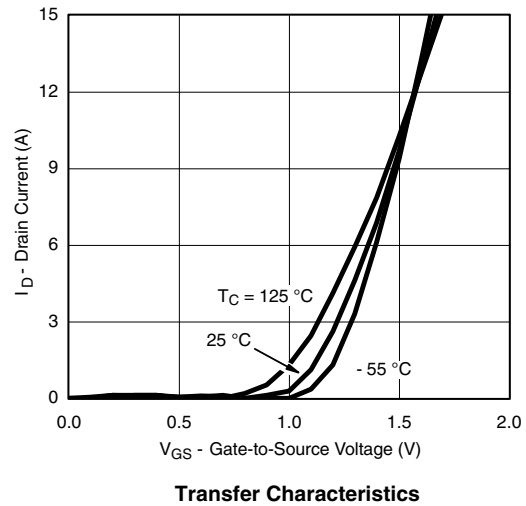
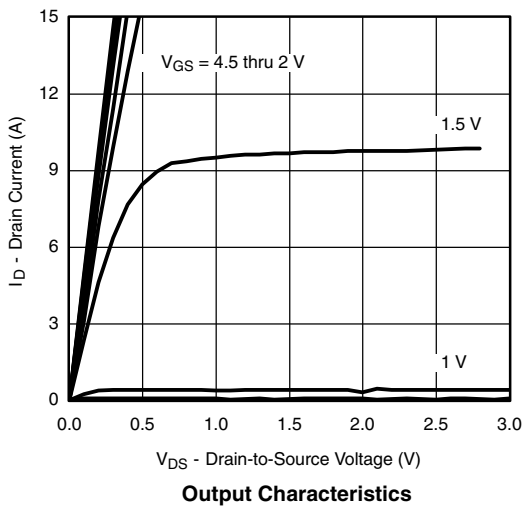
SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = - 350 μA	- 0.4		- 0.9	V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 8 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = - 20 V, V <sub>GS</sub> = 0 V			- 1	μA
		V <sub>DS</sub> = - 20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C			- 5	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≤ - 5 V, V <sub>GS</sub> = - 4.5 V	- 5			A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 1 A		0.022	0.027	Ω
		V <sub>GS</sub> = - 2.5 V, I <sub>D</sub> = - 1 A		0.026	0.032	
		V <sub>GS</sub> = - 1.8 V, I <sub>D</sub> = - 1 A		0.033	0.045	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = - 10 V, I <sub>D</sub> = - 1 A		10		S
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = - 1 A, V <sub>GS</sub> = 0		- 0.6	- 1.1	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = - 10 V, V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 1 A		32	50	nC
Gate-Source Charge	Q <sub>gs</sub>			3.6		
Gate-Drain Charge	Q <sub>gd</sub>			8.5		
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = - 10 V, R <sub>L</sub> = 10 Ω I <sub>D</sub> ≅ - 1 A, V <sub>GEN</sub> = - 4.5 V, R <sub>g</sub> = 6 Ω		30	45	ns
Rise Time	t <sub>r</sub>			45	70	
Turn-Off Delay Time	t <sub>d(off)</sub>			550	825	
Fall Time	t <sub>f</sub>			220	330	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = - 1 A, di/dt = 100 A/μs		265	500	

Notes:

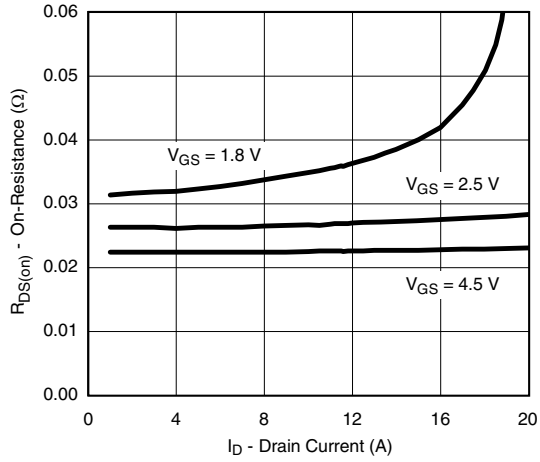
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

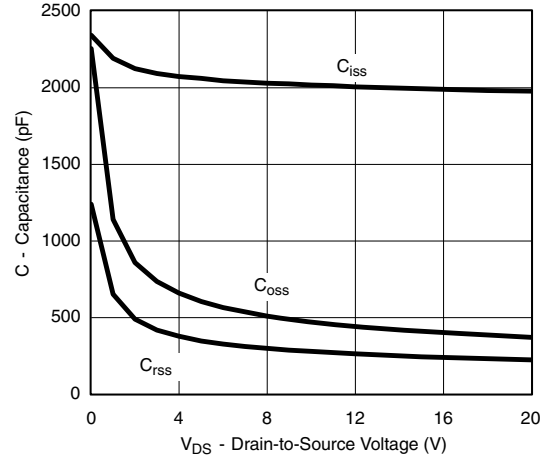
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



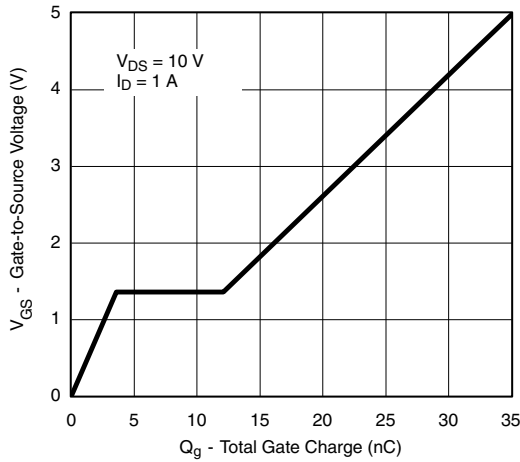
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



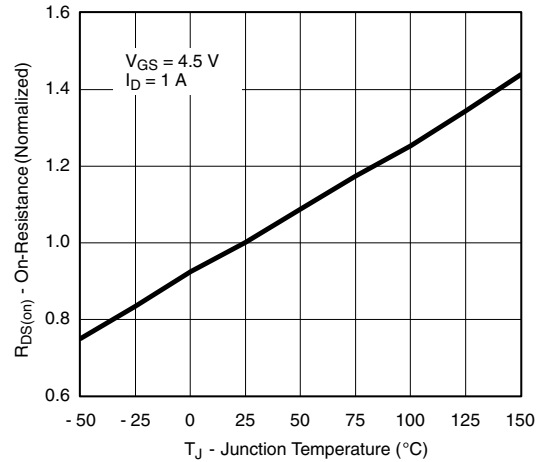
**On-Resistance vs. Drain Current**



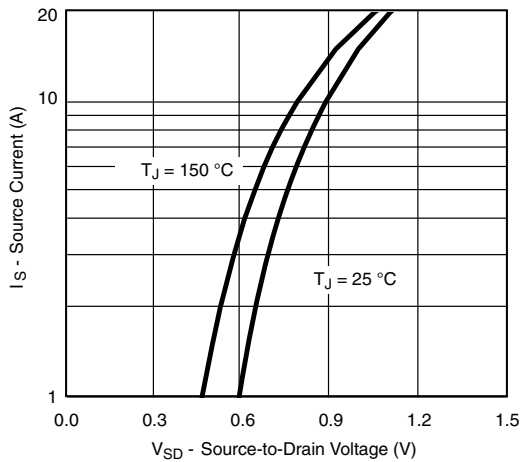
**Capacitance**



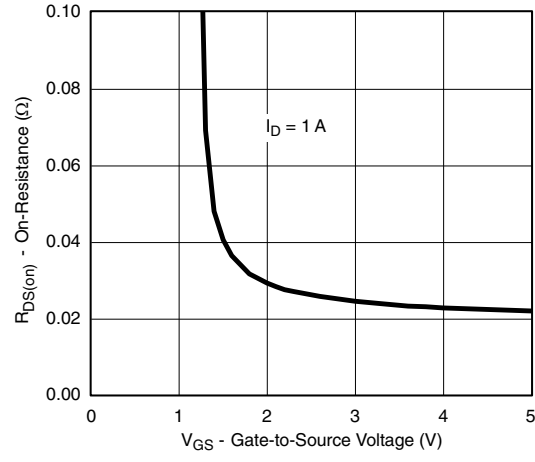
**Gate Charge**



**On-Resistance vs. Junction Temperature**

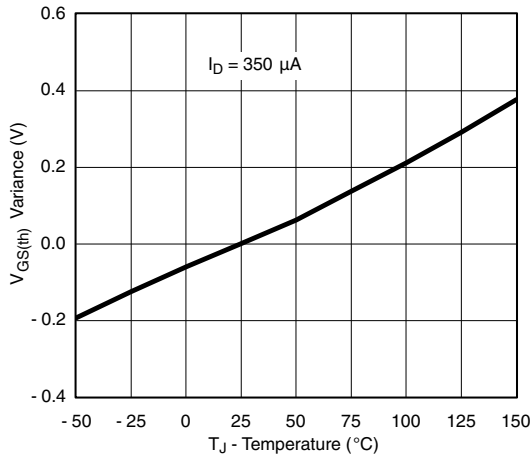


**Source-Drain Diode Forward Voltage**

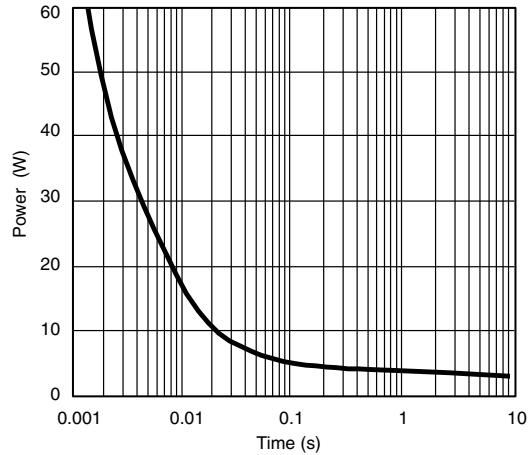


**On-Resistance vs. Gate-to-Source Voltage**

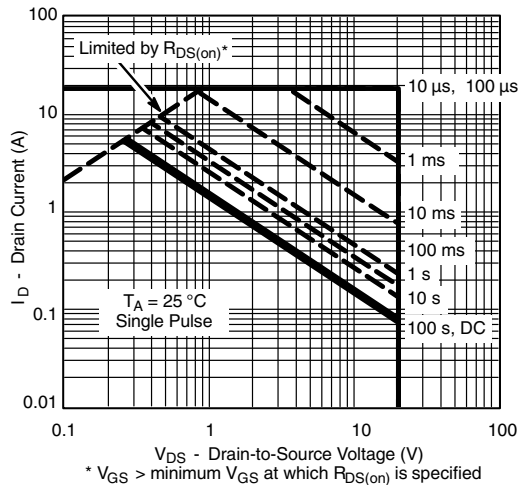
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



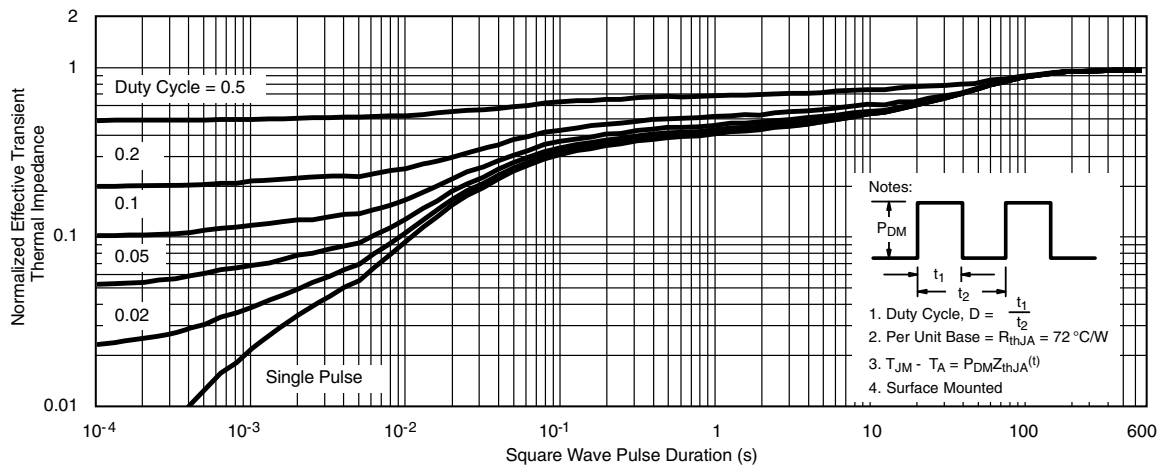
**Threshold Voltage**



**Single Pulse Power, Junction-to-Ambient**

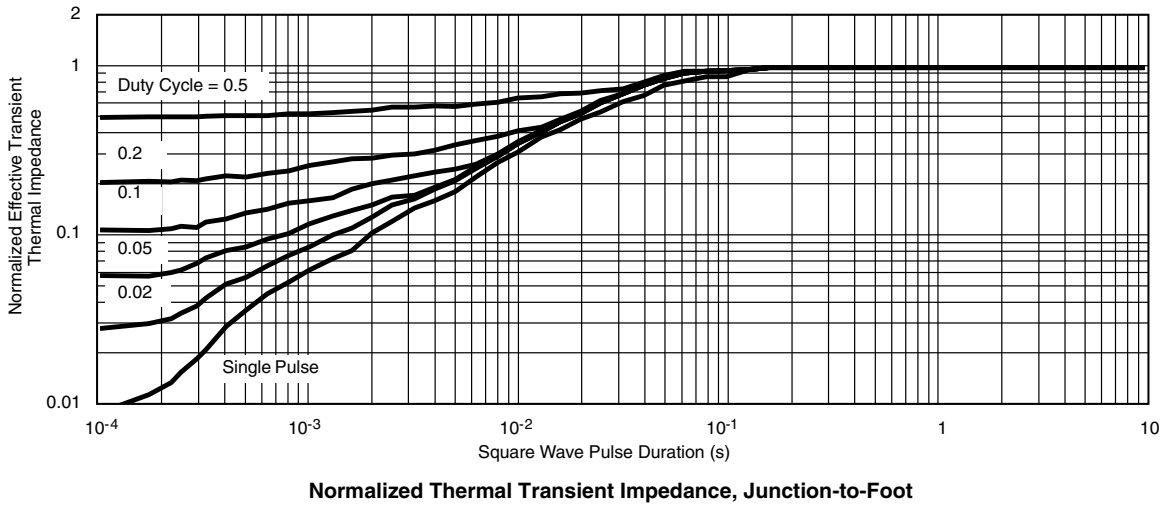


**Safe Operating Area**



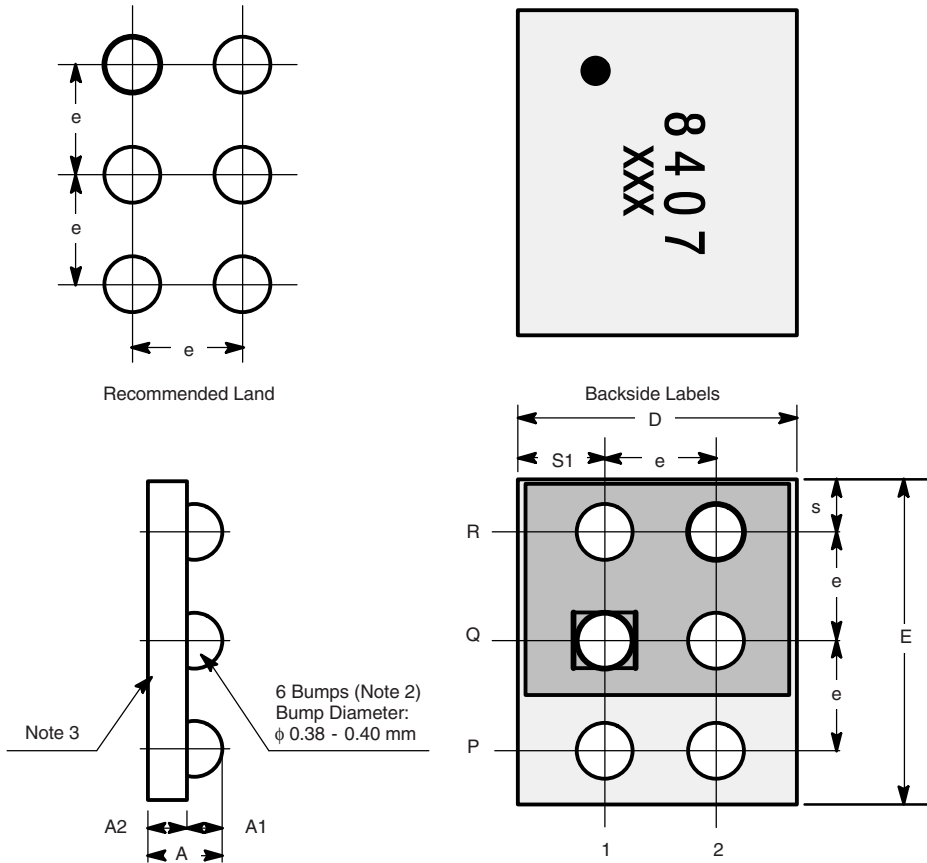
**Normalized Thermal Transient Impedance, Junction-to-Ambient**

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**PACKAGE OUTLINE**

**MICRO FOOT: 6-BUMP (2.4 mm x 2 mm, 0.8 mm PITCH)**



Notes (Unless Otherwise Specified):

1. All dimensions are in millimeters.
2. Bumps are 95.5/3.8/0.7 Sn/Ag/Cu with diameter  $\phi$  0.38 mm - 0.40 mm.
3. Backside surface is coated with a Ti/Ni/Ag layer.
4. Non-solder mask defined copper landing pad.
5. The flat side of wafers is oriented at the bottom.
6. • is location of Pin 1P.

Dim.	Millimeters <sup>a</sup>		Inches	
	Min.	Max.	Min.	Max.
A	0.600	0.650	0.0236	0.0256
A <sub>1</sub>	0.260	0.290	0.0102	0.0114
A <sub>2</sub>	0.340	0.360	0.0134	0.0142
b	0.370	0.410	0.0146	0.0161
D	1.920	2.000	0.0756	0.0787
E	2.320	2.400	0.0913	0.0945
e	0.750	0.850	0.0295	0.0335
S	0.370	0.400	0.0150	0.0157
S1	0.580	0.600	0.0228	0.0236

PAD DISTRIBUTION TABLE			
	P	Q	R
1	Drain	Gate	Source
2	Drain	Source	Source

Notes:

- a. Use millimeters as the primary measurement.

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