Si8901 SERIES

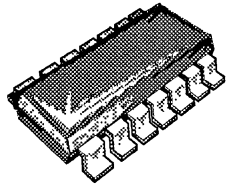
Siliconix incorporated

DMOS Double-Balanced Mixers

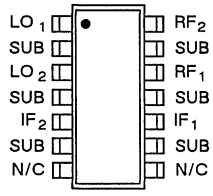
The Si8901 Ring Demodulator/Balanced Mixer offers significant improvements for RF mixer application where low third order harmonic distortion has been a problem. Combining matching with very low junction capacitance, (< 3 pF), low on-resistance (30 Ω) and very high off-resistance (> 10^9 Ω), the Si8901 accepts an RF and a local oscillator (LO) input and provides a high fidelity IF output with typical conversion loss of −8 dB at frequencies up to 200 MHz. Available in an 8-pin TO-78 and SO-14 package, this device is specified over −55 to 125°C temperature range.

PART NUMBER	PACKAGE	$V_{(BR)DS}$ MIN (V)	$V_{GS}(th)$ MAX (V)	$r_{ds(ON)}$ MAX (Ω)
Si8901A	TO-78	15	2.0	70
Si8901CY	SO-14	15	2.0	70

SO-14



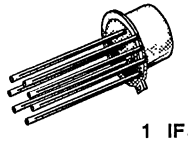
TOP VIEW



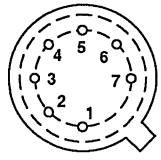
SIMILAR PRODUCTS

- Chips, order Si8901CHP

TO-78



BOTTOM VIEW



1 IF_1
2 RF_1
3 RF_2
4 SUB
5 LO_1
6 LO_2
7 IF_2

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT		UNITS
		Si8901A	Si8901CY	
Gate-Source, Gate-Drain Voltage	V_{GS}, V_{GD}	30/−22.5	30/−22.5	V
Drain-Substrate, Source-Substrate Voltage	V_{DB}, V_{SB}	22.5	22.5	
Drain-Source Voltage	V_{DS}	15	15	
Gate-Substrate Voltage [1]	V_{GB}	30/−0.3	30/−0.3	
Drain Current	I_D	50		mA
Power Dissipation (Package)	P_D	500		mW
Power Derating		5		mW/°C
Operating Junction Temperature	T_J	−55 to 125		°C
Storage Temperature	T_{stg}	−65 to 150		
Lead Temperature (1/16" from case for 10 seconds)	T_L	300		

[1] These devices feature an internal Zener protected gate.

ELECTRICAL CHARACTERISTICS [1]				LIMITS				
				Si8901A		Si8901CY		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP [2]	MIN	MAX	MIN	MAX	UNIT
STATIC								
Drain-Source Breakdown Voltage	$V_{(BR)DS}$	$V_{GS} = V_{BS} = -5$ V, $I_D = 10$ nA	30	15		15		V
Source-Drain Breakdown Voltage	$V_{(BR)SD}$	$V_{GD} = V_{BD} = -5$ V, $I_S = 10$ nA	22	15		15		V
Drain-Substrate Breakdown Voltage	$V_{(BR)DB}$	$V_{GB} = 0$ V, $I_D = 10$ nA, Source OPEN	35	22.5		22.5		V
Source-Substrate Breakdown Voltage	$V_{(BR)SB}$	$V_{GB} = 0$ V, $I_S = 10$ nA, Drain OPEN	35	22.5		22.5		V
Drain-Source Leakage	$I_{DS(OFF)}$	$V_{GS} = V_{BS} = -5$ V, $V_{DS} = 15$ V	0.7					nA
Source-Drain Leakage	$I_{SD(OFF)}$	$V_{GD} = V_{BD} = -5$ V, $V_{SD} = 15$ V	0.8					nA
Gate Leakage	I_{GBS}	$V_{DB} = V_{SB} = 0$ V, $V_{GB} = 30$ V	0.01		2		2	µA
Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS} = V_{GS(th)}$, $I_S = 1$µA, $V_{SB} = 0$ V	0.7	0.1	2	0.1	2	V
Drain-Source On-Resistance	$r_{DS(ON)}$	$I_D = 10$ mA, $V_{SB} = 0$ V, $V_{GS} = 5$ V	60		75		75	Ω
		$I_D = 10$ mA, $V_{SB} = 0$ V, $V_{GS} = 10$ V	40					Ω
		$I_D = 10$ mA, $V_{SB} = 0$ V, $V_{GS} = 15$ V	33					Ω
		$I_D = 10$ mA, $V_{SB} = 0$ V, $V_{GS} = 20$ V	29					Ω
Resistance Match		$I_D = 10$ mA, $V_{SB} = 0$ V, $V_{GS} = 5$ V	1		7		7	Ω
DYNAMIC								
$LO_1 - LO_2$ Capacitance	C_{gg}	$V_{DS} = 0$ V, $V_{BS} = -5.5$ V, $V_{GS} = 4$ V	4.4					pF
Conversion Loss	L_c	See Figure 1, $P_{LO} = +17$ dBm	8					dB
Third Order Intercept	IMD_3	See Figure 1, $P_{LO} = +17$ dBm	35					dB
Maximum Operation Frequency	f_{MAX}		250					MHz

NOTES: 1. $T_A = 25$ °C unless otherwise noted.
2. For design aid only, not subject to production testing.

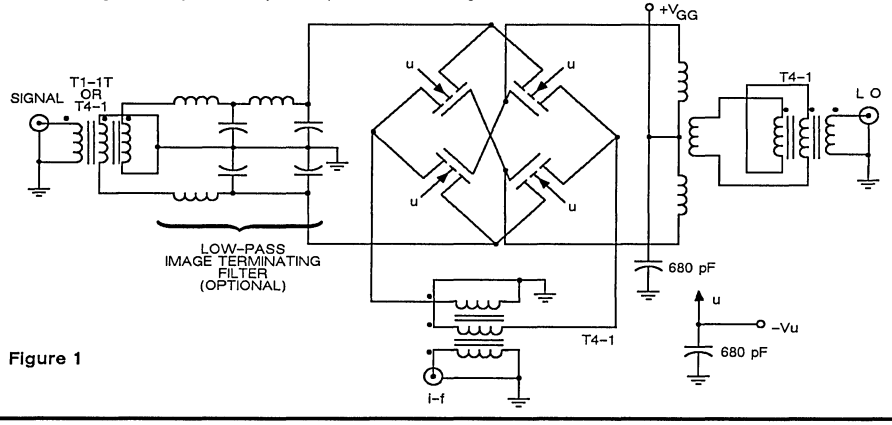


Figure 1

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