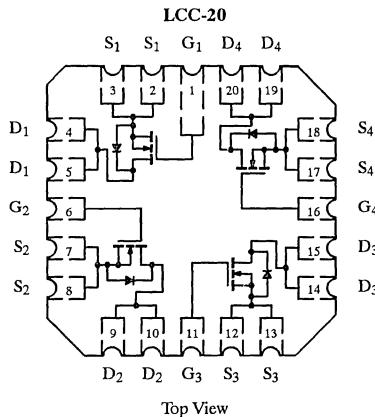


Quad N-Channel Enhancement-Mode MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
20	0.1 @ $V_{GS} = 10$ V	5
	0.2 @ $V_{GS} = 4.5$ V	1

**Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ^a	I_D	5	A
		3	
Pulsed Drain Current ^a	I_{DM}	14	A
Continuous Source Current (Diode Conduction)	I_S	3	
Maximum Power Dissipation	P_D	3	W
		1.3	
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C

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N/P-Channel
MOSFETs**Thermal Resistance Ratings**

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Case	R_{thJC}	40	°C/W

Notes:

a. Drain current limited by package construction.

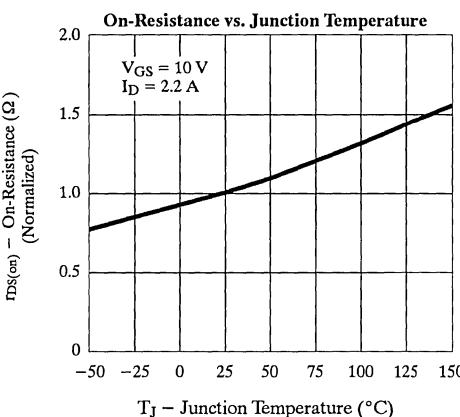
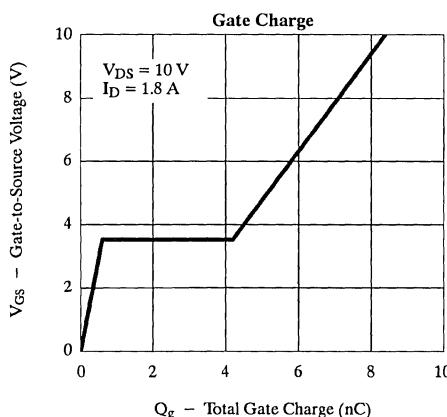
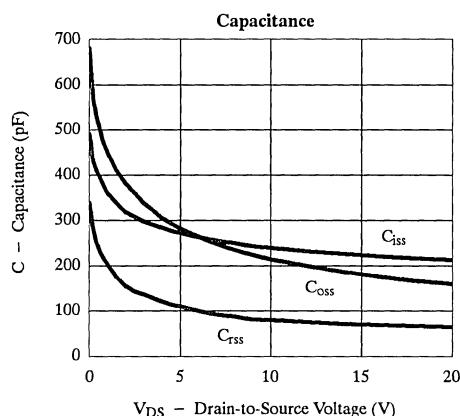
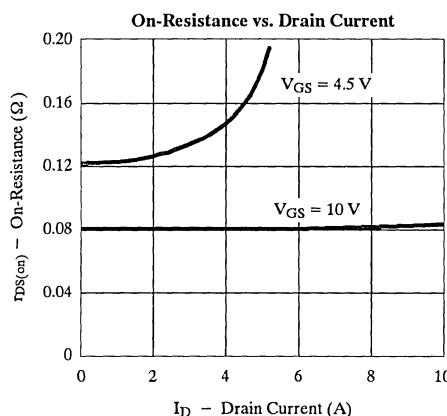
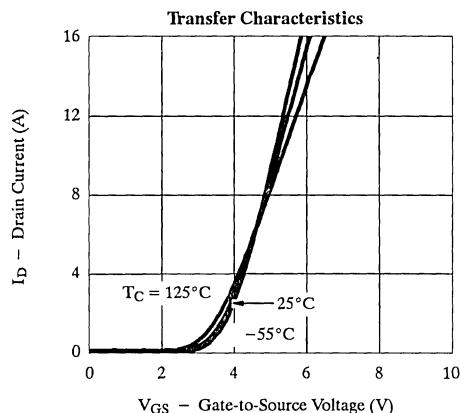
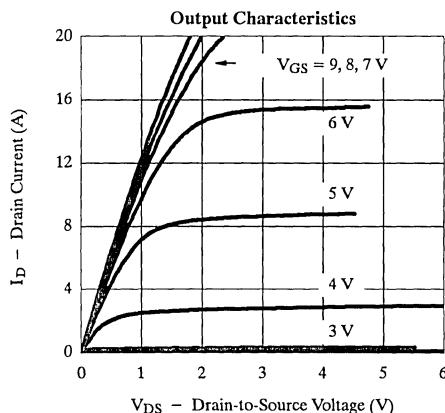
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Max	Unit
Static					
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	20		V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1	3.5	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$		± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}$		10	μA
		$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 125^\circ\text{C}$		25	
On-State Drain Current ^b	$I_{D(\text{on})}$	$V_{DS} = 10 \text{ V}, V_{GS} = 10 \text{ V}$	7		A
Drain-Source On-State Resistance ^b	$r_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}, I_D = 3 \text{ A}$		0.1	Ω
		$V_{GS} = 4.5 \text{ V}, I_D = 1 \text{ A}$		0.2	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15 \text{ V}, I_D = 3 \text{ A}$	2		S
Dynamic					
Input Capacitance ^a	C_{iss}	$V_{GS} = 0 \text{ V}, V_{DS} = 16 \text{ V}, f = 1 \text{ MHz}$		500	nC
Output Capacitance ^a	C_{oss}			300	
Reverse Transfer Capacitance ^a	C_{rss}			125	
Total Gate Charge ^{a, c}	Q_g	$V_{DS} = 10 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 5 \text{ A}$		30	
Gate-Source Charge ^{a, c}	Q_{gs}			5	
Gate-Drain Charge ^{a, c}	Q_{gd}			8	
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = 10 \text{ V}, R_L = 2 \Omega$ $I_D \equiv 3 \text{ A}, V_{GEN} = 10 \text{ V}, R_G = 6 \Omega$		30	ns
Rise Time ^c	t_r			35	
Turn-Off Delay Time ^c	$t_{d(off)}$			70	
Fall Time ^c	t_f			30	
Source-Drain Diode ($T_C = 25^\circ\text{C}$)					
Pulsed Current	I_{SM}			3	A
Diode Forward Voltage ^b	V_{SD}	$I_F = 3 \text{ A}, V_{GS} = 0 \text{ V}$		1.6	V
Reverse Recovery Time	t_{rr}	$I_F = 3 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}$		100	ns

Notes:

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
- c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)



Si8956AZ/883

Siliconix

Typical Characteristics (25°C Unless Otherwise Noted)