

Single-Ended Bus Transceiver

DESCRIPTION

The Si9241AEY is a monolithic bus transceiver designed to provide bidirectional serial communication in automotive diagnostic applications.

The device incorporates protection against overvoltages and short circuits to V_{BAT} . The transceiver pin is protected and can be driven beyond the V_{BAT} voltage.

The Si9241AEY is built on the Vishay Siliconix BiC/DMOS process. An epitaxial layer prevents latchup.

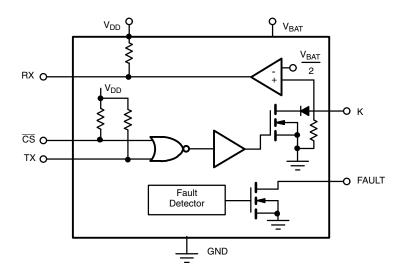
The RX output is capable of driving CMOS or 1 x LSTTL load.

The Si9241AEY is available in a space efficient 8-pin SO package. It operates reliably over the automotive temperature range (- 40 to 125 °C). The Si9241AEY is available in both standard and lead (Pb)-free packages.

FEATURES

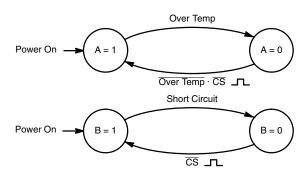
- · Operating Power Supply Range $6 \text{ V} \leq \text{ V}_{BAT} \leq 36 \text{ V}$
- Reverse Battery Protection Down to $V_{BAT} \geq$ 24 V
- Standby Mode With Very Low Current Consumption $I_{BAT(SB)} = 1 \mu A$ at $V_{DD} = 0.5 V$
- Low Quiescent Current in OFF Condition I_{BAT} = 120 μA and $I_{DD} \leq$ 10 A
- ISO 9141 Compatible
- Overtemperature Shutdown Function For K Output
- Defined K Output OFF for Open GND
- Defined Receive Output Status for Open K Input
- Defined K Output OFF for TX Input Open
- Open Drain Fault Output
- 2 kV ESD
- Typical Transmit Speeds of 200 kBaud

PIN CONFIGURATION AND FUNCTIONAL BLOCK DIAGRAM





OUTPUT TABLE AND STATE DIAGRAMS



Note: Over Temp is an internal condition, not meant to be a logic signal.

INPUTS STATE VARIABLE			OUTPUT TABLE				
CS	TX	Α	В	RX	K	FAULT	Comments
0	0	1	1	0	0	1	
0	1	1	1	1	1	1	
Х	Х	0	1	K	HiZ	0	Over Temp
0	Х	1	0	K	HiZ	0	Short Circuit
1	X	1	1	0	0	1	Receive Mode
1	Χ	1	1	1	1	1	
X = "1" or "0" HiZ = High Impedance State							

Parameter	Limit	Unit	
Voltages Referenced to Ground	·	•	
Voltage On V _{BAT}	- 24 to 45		
Voltage K	- 16 to (V _{BAT} + 1)	V	
Voltage Difference V _(VBAT, K)	55		
Voltage or Max. Current On Any Pin (Except V _{BAT} , K)	- 0.3 to (V _{DD} + 0.3 V) or 10	mA	
Voltage on V _{DD}	7	V	
K Pin Only, Short Circuit Duration (to V _{BAT} or GND)	Continuous		
Operating Temperature (T _A)	- 40 to 125	°C	
Junction and Storage Temperature	- 55 to 150	7	
Thermal Impedance (Θ_{JA})	125	°C/W	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE				
Parameter	Limit	Unit		
Voltages Referenced to Ground	·			
V_{DD}	4.5 to 5.5			
V _{BAT}	6 to 36	V		
K	6 to 36	v		
Digital Inputs	0 to V _{DD}			



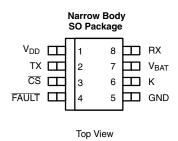


SPECIFICATIONS								
		Test Conditions Unless Specified V _{DD} = 4.5 V to 5.5 V			Limits - 40 to 125 °C			
Parameter	Symbol	$V_{BAT} = 6 \text{ V to } 36 \text{ V}$		Temp.a	Min.b	Typ. ^c	Max.b	Unit
Transmitter and Logic Levels					L	L		
CS, TX Input Low Voltage	V _{ILT}			Full			1.5	V
CS, TX Input High Voltage	V _{IHT}			Full	3.5			V
TX Input Capacitanced	C _{INT}			Full			10	pF
CS, TX Input Pull-up Resistance	R _{TX} ,	V _{DD} = 5.5 V, TX or CS = 1.5 \	/, 3.5 V	Full	10	20	40	kΩ
K Transmit								
		$R_L = 510 \Omega \pm 5 \%$, $V_{BAT} = 6 \text{ to } 18$		Full			0.2 V _{BAT}	
K Output Low Voltage	V_{OLK}	$R_L = 1 \text{ k}\Omega \pm 5 \text{ %, V}_{BAT} = 16 \text{ to } 36$		Full			0.2 V _{BAT}	
		$R_L = 510 \Omega \pm 5 \%$, $V_{BAT} =$		Full			1.2	٧
K Output High Voltage	V _{OHK}	$R_L = 510 \Omega \pm 5 \%$, $V_{BAT} = 4.5 \text{ to } 18$		Full	0.95 V _{BAT}			1
R Output Flight Voltage	OHK	$R_L = 1 \text{ k}\Omega \pm 5 \text{ %, } V_{BAT} = 16$	to 36	Full	0.95 V _{BAT}			
K Rise, Fall Times	t _r , tf	See Test Circuit		Full			9.6	μs
K Output Sink Resistance	Rsi	CS = 0 V, TX = 0 V		Full			110	Ω
K Output Capacitance ^d	Co	03 = 0 V, 1X = 0 V		Full			20	pF
Receiver								
K Input Low Voltage	V _{ILK}			Full			0.35 V _{BAT}	
K Input High Voltage	V_{IHK}			Full	0.65 V _{BAT}			V
K Input Hysteresis ^{c, d}	V _{HYS}			Full		0.05 V _{BAT}		
K Input Currents	I_{IHK}		= V _{BAT}	Full			20	μΑ
RX Output Low Voltage	V _{OLR}	$\overline{\text{CS}} = 4$ $V_{\text{ILK}} = 0$ $I_{\text{OLR}} = 0$.35 V _{BAT} = 1 mA	Full			0.4	٧
RX Pull-up Resistance	R _{RX}			Full	5		20	kΩ
RX Turn On Delay		$R_L = 510 \Omega \pm 5 \%$, $V_{BAT} = 6 V$ $C_L = 10 \text{ nF, See Test Circ}$	to 18 V cuit	Full		3	10	
nx full on belay	^t d(on)	$R_L = 1 \text{ k}\Omega \pm 5 \text{ %, V}_{BAT} = 16 \text{ V}$ $C_L = 4.7 \text{ nF, See Test Circ}$	to 36 V cuit	Full		3	10	110
RX Turn Off Delay	t _{d(off)}	R_L = 510 Ω ± 5 %, V_{BAT} = 6 V to 18 V C_L = 10 nF, See Test Circuit		Full		3	10	μs
	-d(oii)	$R_L = 1 \text{ k}\Omega \pm 5 \text{ %}, V_{BAT} = 16 \text{ V}$ $C_L = 4.7 \text{ nF}, \text{ See Test Circ}$	to 36 V cuit	Full		3	10	
Supplies					I	T T	I	_
Bat Supply Current On	I _{BAT(on)}	$\overline{\text{CS}} = \text{TX} = 0 \text{ V}, \text{ V}_{\text{BAT}} \le 16$	5 V	Full		1.2	3	mA
Bat Supply Current Off	I _{BAT(off)}	CS = High, V _{BAT} ≤ 12 V, TX =		Full		120	220	μΑ
Bat Supply Current Standby	I _{BAT(SB)}	$V_{DD} \le 0.5 \text{ V}, V_{BAT} \le 12 \text{ V}$	V	Full		< 1	10	J
Logic Supply Current On	I _{DD(on)}	$V_{DD} \le 5.5 \text{ V}, \text{ TX} = 0 \text{ V}$		Full		1.4	2.3	mA
Logic Supply Current Off	I _{DD(off)}	$\overline{\text{CS}}$ = High, $V_{\text{BAT}} \le 12 \text{ V, TX}$ =	= High ^f	Full			10	μΑ
Miscellaneous					ı		1	
TX Transmit Baud Rate	BR _T	$R_L = 510 \Omega, C_L = 10 \text{nF}$		Full	10.4			kBaud
RX Receive Baud Rate ^c	BR _R	$6 \text{ V} < \text{V}_{\text{BAT}} < 16 \text{ V}, \text{C}_{\text{RX}} = 2$		Full		200		
Transmission Frequency	f _{K-RXK}	$6 \text{ V} < \text{V}_{BAT} < 16 \text{ V}, R_K = 510 \Omega, C$		Full	50	200		kHz
Fault Output Low Voltage	V _{OLF}	$\overline{\text{CS}} = \text{TX} = 0, \text{ K} = \text{V}_{\text{BAT}}, \text{ I}_{\text{OLF}} = \text{CS}$	= 1 mA	Full			0.4	V
CS Minimum Pulse Width ^{d, e}	t _{cs}			Full	1			μs
Over Temperature Shutdown ^d				160	180		°C	
Temperature Shutdown Hysteresis ^c	T _{HYST}					30		Ŭ

Notes:

- Notes:
 a. Room = 25 °C, Cold and Hot = as determined by the operating temperature suffix.
 b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
 c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
 d. Guaranteed by design, not subject to production test.
 e. Minimum pulse width to reset a fault condition.
 f. High referes to Logic High and Low refers to Logic Low.

PIN CONFIGURATION



ORDERING INFORMATION			
Part Number	Temperature Range		
Si9241AEY-T1	- 40 °C to 125 °C		
Si9241AEY-T1-E3 (Lead (Pb)-free)			

PIN DESCRIPTION					
Pin Number	Symbol Description				
1	V_{DD}	Positive Power Supply			
2	TX	Transmit, Input			
3	CS	Chip Select, Input			
4	FAULT	Fault, Open Drain Output			
5	GND	Ground Connection			
6	K	Transmit/Receive, Bidirectional			
7	V _{BAT}	Battery Power Supply			
8	RX	Receiver, Output			

FUNCTIONAL DESCRIPTION

The Si9241AEY can be either in transmit or receive mode and it contains over temperature, and short circuit V_{BAT} fault detection circuits.

The voltage on K is internally compared to $V_{\text{BAT/2}}$. If the voltage on the K pin is less than $V_{BAT/2}$ then RX output will be "low". If the voltage on the K pin is greater than V_{BAT/2} then RX output will be "high".

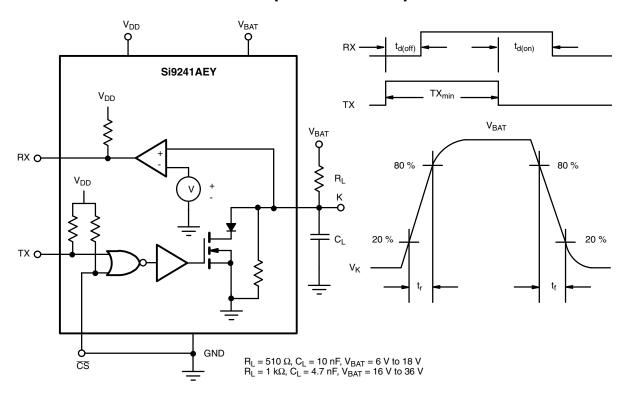
In order to be in transmit mode, $\overline{\text{CS}}$ must be set "low". When CS and TX are set "low" the internal MOSFET will turn on, causing the K pin to be "low". In the transmit mode, the processor monitors RX and TX. When the two mirror each other there is no fault. In the event of over temperature, or short circuit to V_{BAT} , the Si9241AEY will turn off the K output to protect the IC and the external open drain FAULT pin will be asserted. The K pin will stay in high impedance and RX will follow the K pin. The fault will be reset when $\overline{\text{CS}}$ is toggled high. RX, CS and TX pins have an internal pull up resistor to V_{DD} while the K pin has internal pull down resistors. When any one of the TX, V_{BAT} or GND pins is open the K output is

When CS is set "high" the Si9241AEY is in receive mode and the internal MOSFET for the K pin is turned off. The RX output will follow the K pin. If $\overline{\text{CS}}$ is "low" while the IC is receiving data, an incorrect fault signal will occur.

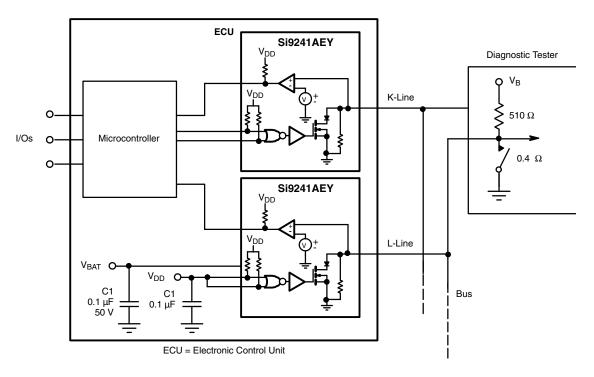
To inhibit the short detect, tie $\overline{\text{CS}}$ and TX together.



TEST CIRCUIT AND TIMING DIAGRAMS (TRANSMIT ONLY)



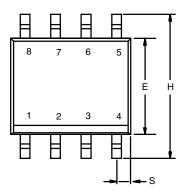
APPLICATIONS CIRCUIT



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?70787.



SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







	MILLIM	IETERS	INCHES			
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A ₁	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
E	3.80	4.00	0.150	0.157		
е	1.27	BSC	0.050 BSC			
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
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