

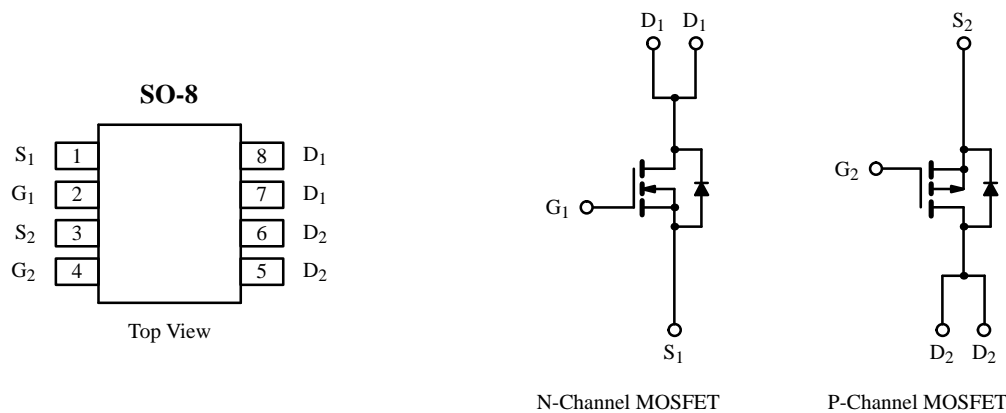
Dual Enhancement-Mode MOSFET (N- and P-Channel)

Product Summary

	V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
N-Channel	20	0.125 @ V _{GS} = 10 V	± 3.0
		0.250 @ V _{GS} = 4.5 V	± 2.0
P-Channel	-20	0.200 @ V _{GS} = -10 V	± 2.5
		0.350 @ V _{GS} = -4.5 V	± 2.0

Recommended upgrade: Si4532DY or Si4539DY

Lower profile/smaller size—see LITE FOOT® equivalent: Si6452DQ



Absolute Maximum Ratings (T_A = 25° C Unless Otherwise Noted)

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V _{DS}	20	-20	V
Gate-Source Voltage	V _{GS}	± 20	± 20	
Continuous Drain Current (T _J = 150°C) ^a	I _D	T _A = 25°C	± 3.0	A
		T _A = 70°C	± 2.5	
Pulsed Drain Current	I _{DM}	± 10	± 10	A
Continuous Source Current (Diode Conduction) ^a	I _S	1.6	-1.6	
Maximum Power Dissipation ^a	P _D	T _A = 25°C	2.0	W
		T _A = 70°C	1.3	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150		°C

Thermal Resistance Ratings

Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	62.5	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Subsequent updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #1212. A SPICE Model data sheet is available for this product (FaxBack document #5107).

Specifications (T_J = 25°C Unless Otherwise Noted)

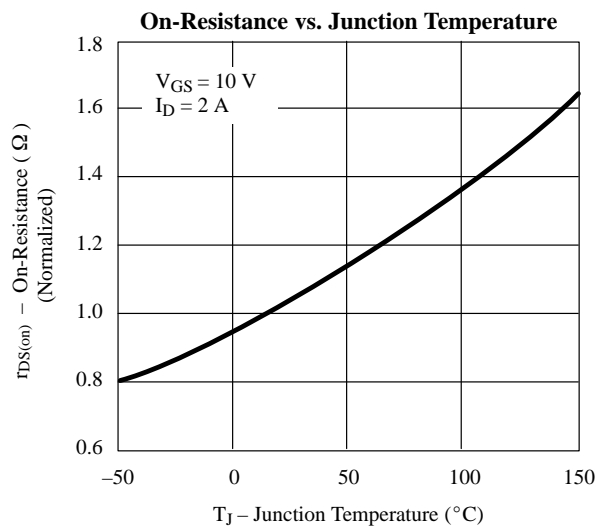
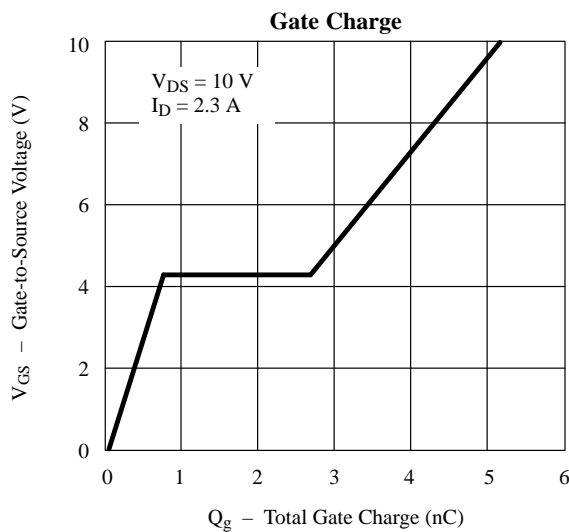
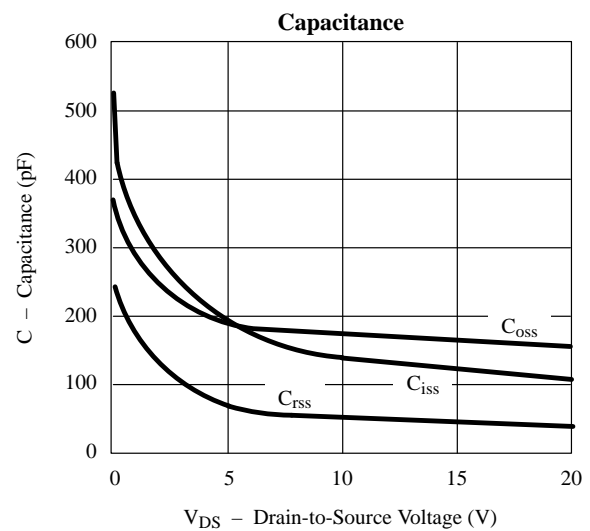
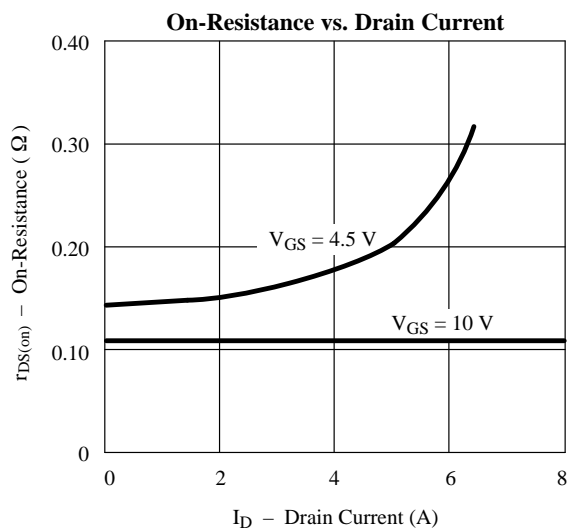
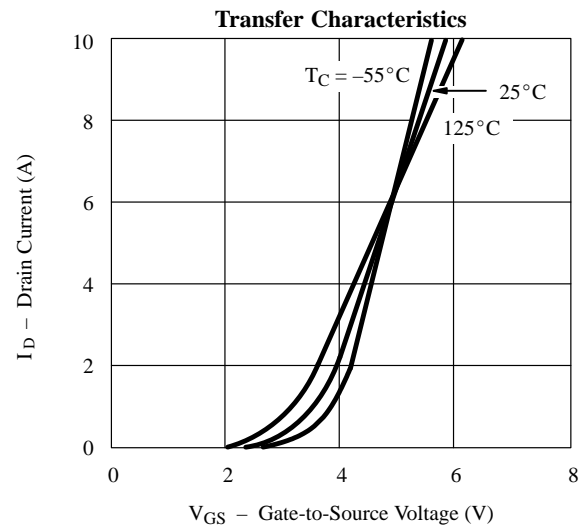
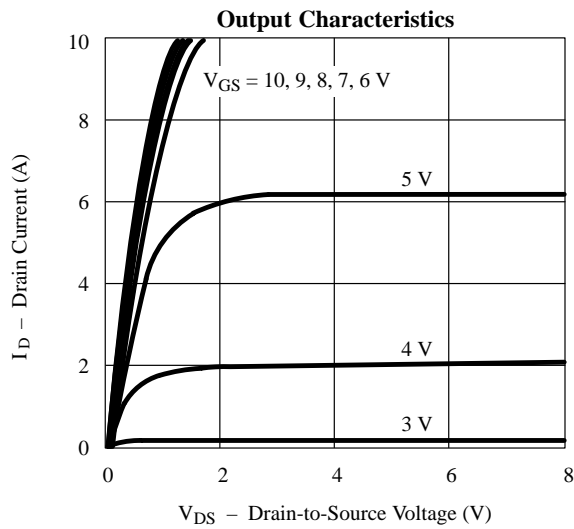
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit	
Static							
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	1.0		V	
		V _{DS} = V _{GS} , I _D = -250 μA	P-Ch	-1.0			
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 16 V, V _{GS} = 0 V	N-Ch		2	μA	
		V _{DS} = -16 V, V _{GS} = 0 V	P-Ch		-2		
		V _{DS} = 16 V, V _{GS} = 0 V, T _J = 55°C	N-Ch		25		
		V _{DS} = -16 V, V _{GS} = 0 V, T _J = 55°C	P-Ch		-25		
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	N-Ch	10		A	
		V _{DS} ≤ -5 V, V _{GS} = -10 V	P-Ch	-10			
		V _{DS} ≥ 5 V, V _{GS} = 4.5 V	N-Ch	2			
		V _{DS} ≤ -5 V, V _{GS} = -4.5 V	P-Ch	-2			
Drain-Source On-State Resistance ^b	r _{DS(on)}	V _{GS} = 10 V, I _D = 1.0 A	N-Ch		0.11	0.125	Ω
		V _{GS} = -10 V, I _D = 1.0 A	P-Ch		0.16	0.200	
		V _{GS} = 4.5 V, I _D = 0.5 A	N-Ch		0.15	0.250	
		V _{GS} = -4.5 V, I _D = 0.5 A	P-Ch		0.30	0.350	
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 3.0 A	N-Ch		3.7	S	
		V _{DS} = -15 V, I _D = -3.0 A	P-Ch		3.0		
Diode Forward Voltage ^b	V _{SD}	I _S = 1.25 A, V _{GS} = 0 V	N-Ch		0.9	1.2	V
		I _S = -1.25 A, V _{GS} = 0 V	P-Ch		-0.9	-1.6	
Dynamic^a							
Total Gate Charge	Q _g	N-Channel V _{DS} = 10 V, V _{GS} = 10 V, I _D = 2.3 A P-Channel V _{DS} = -10 V, V _{GS} = -10 V, I _D = -2.3 A	N-Ch		5.2	25	nC
Gate-Source Charge	Q _{gs}		N-Ch		0.8		
Gate-Drain Charge	Q _{gd}		P-Ch		0.9		
			N-Ch		2.0		
Turn-On Delay Time	t _{d(on)}		N-Ch		5	15	ns
Rise Time	t _r	N-Channel V _{DD} = 20 V, R _L = 20 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω	P-Ch		10	40	
			N-Ch		10	20	
Turn-Off Delay Time	t _{d(off)}	P-Channel V _{DD} = -20 V, R _L = 20 Ω I _D ≅ -1 A, V _{GEN} = -10 V, R _G = 6 Ω	P-Ch		10	40	
			N-Ch		25	50	
Fall Time	t _f		P-Ch		38	90	
		N-Ch		22	50		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 1.25 A, di/dt = 100 A/μs	P-Ch		69	100	
			N-Ch		69	100	

Notes

- a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

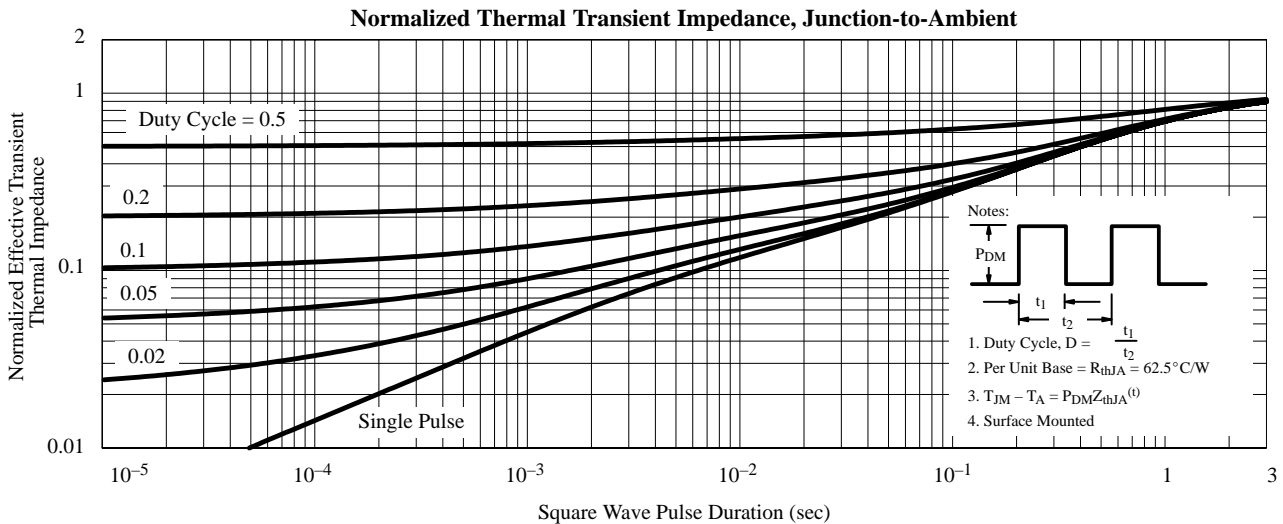
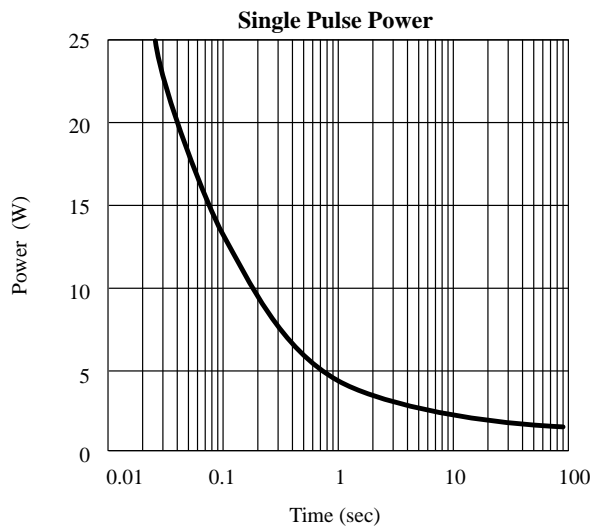
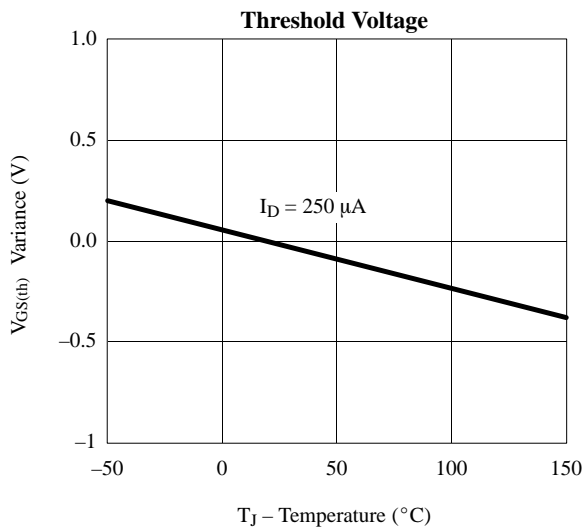
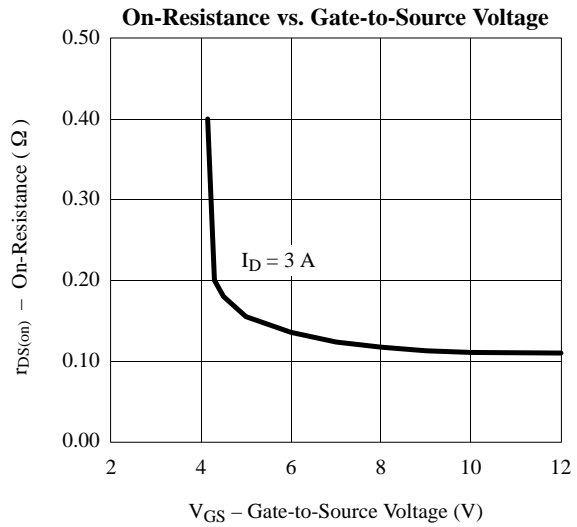
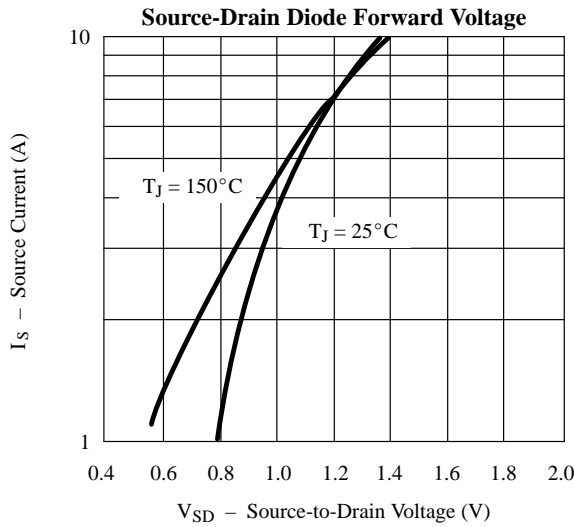
Typical Characteristics (25°C Unless Noted)

N-Channel



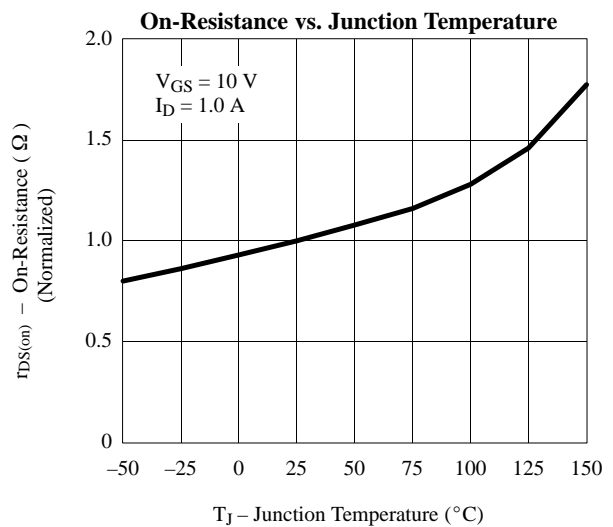
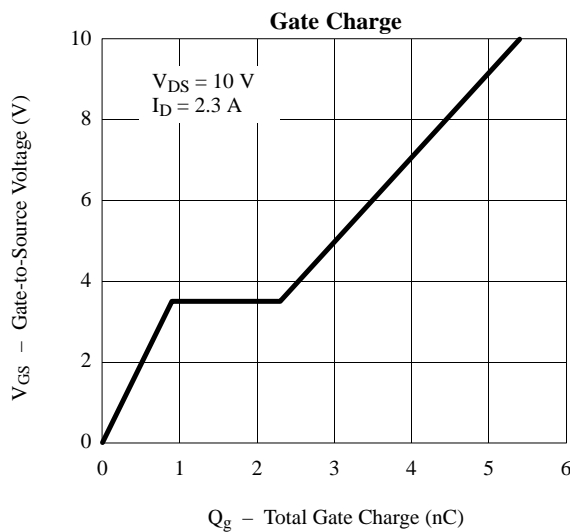
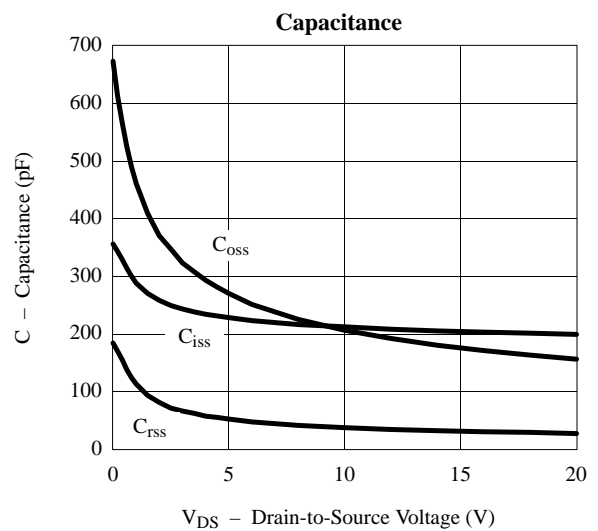
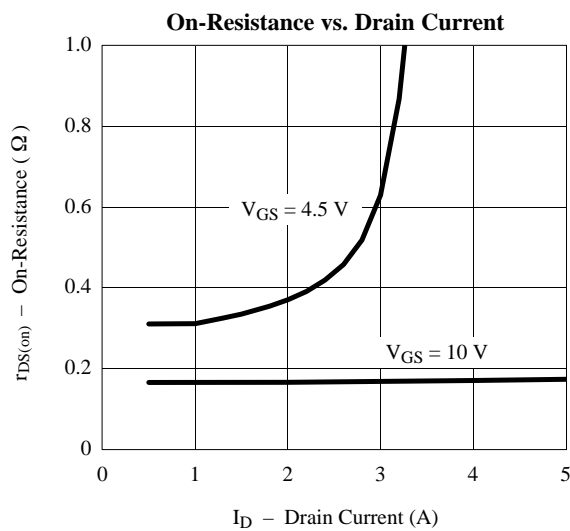
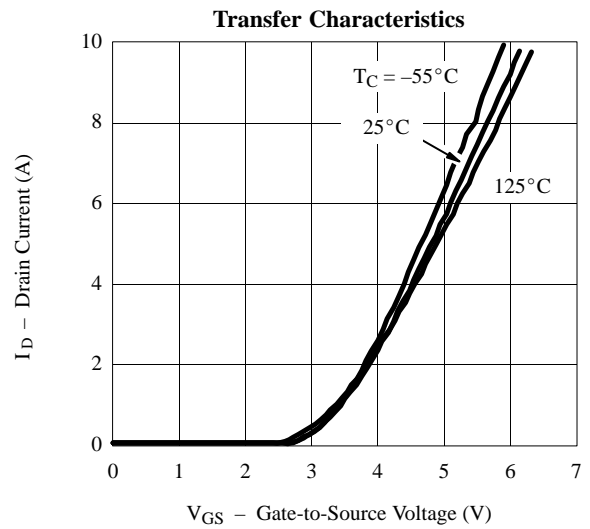
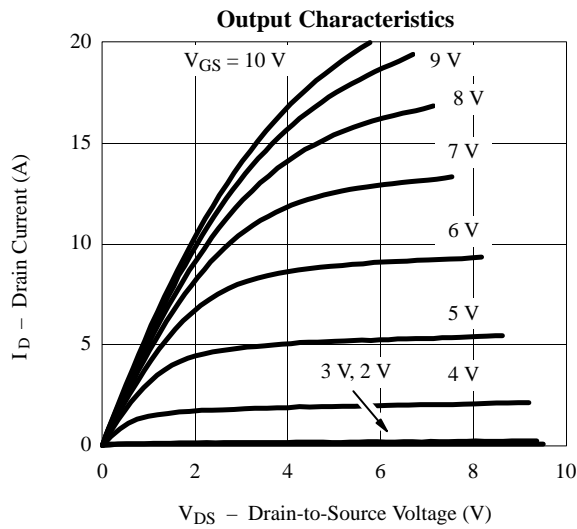
Typical Characteristics (25°C Unless Noted)

N-Channel



Typical Characteristics (25°C Unless Noted)

P-Channel



Typical Characteristics (25°C Unless Noted)

P-Channel

