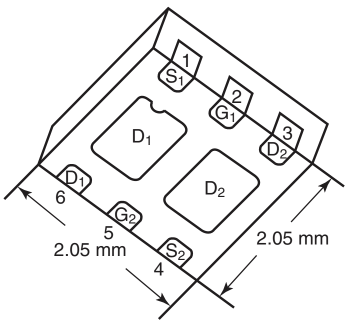
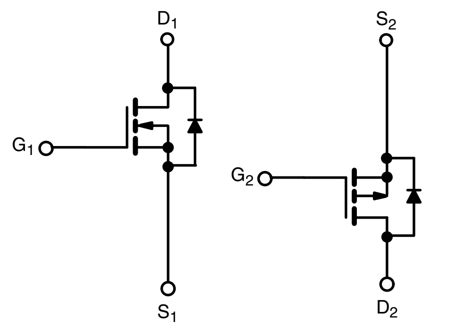
N- and P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY				
	V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
N-Channel	20	0.040 at V_{GS} = 4.5 V	4.2	3.7 nC
		0.065 at V_{GS} = 2.5 V	3.3	
P-Channel	- 20	0.090 at V_{GS} = - 4.5 V	- 2.9	5.3 nC
		0.137 at V_{GS} = - 2.5 V	- 2.3	



DFNWB2*2-6L-A



N-Channel MOSFET   P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)					
Parameter		**Symbol**	**N-Channel**	**P-Channel**	**Unit**
Drain-Source Voltage		V_{DS}	20	- 20	V
Gate-Source Voltage		V_{GS}	± 12		
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	4.2	- 2.9	A
Pulsed Drain Current		I_{DM}	15	- 15	
Source Drain Current Diode Current	T_C = 25 °C	I_S	4.5	- 4.5	
Maximum Power Dissipation	T_C = 25 °C	P_D	7.8	7.8	W
	T_A = 25 °C		1.9	1.9	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature)[d, e]			260		

THERMAL RESISTANCE RATINGS							
			N-Channel		P-Channel		
Parameter		**Symbol**	**Typ.**	**Max.**	**Typ.**	**Max.**	**Unit**
Maximum Junction-to-Ambient[b, f]	t ≤ 5 s	R_{thJA}	52	65	52	65	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	12.5	16	12.5	16	

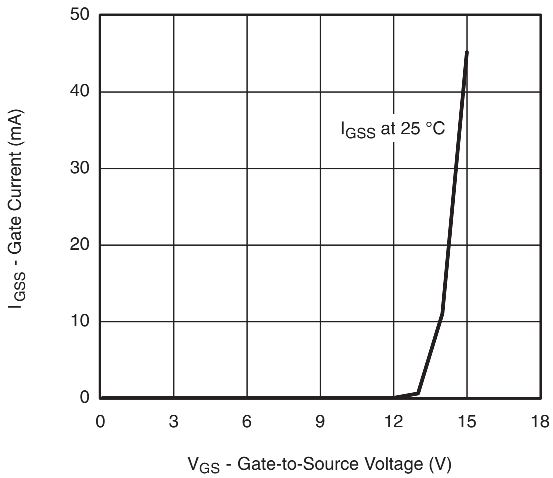
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
Parameter	**Symbol**	**Test Conditions**		**Min.**	**Typ.**	**Max.**	**Unit**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	N-Ch	20			V
		V_{GS} = 0 V, I_D = - 250 µA	P-Ch	- 20			
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 µA	N-Ch		23		mV/°C
		I_D = - 250 µA	P-Ch		- 11		
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I_D = 250 µA	N-Ch		- 3.3		
		I_D = - 250 µA	P-Ch		2.6		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA	N-Ch	0.6		1.4	V
		$V_{DS} = V_{GS}$, I_D = - 250 µA	P-Ch	- 0.5		- 1.3	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 12 V	N-Ch			± 0.1	µA
			P-Ch			± 0.1	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V	N-Ch			0.1	
		V_{DS} = - 20 V, V_{GS} = 0 V	P-Ch			- 0.1	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 4.5 V	N-Ch	10			A
		V_{DS} ≤ - 5 V, V_{GS} = - 4.5 V	P-Ch	- 10			
Drain-Source On-State Resistance[b]	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 4.2 A	N-Ch		0.032	0.040	Ω
		V_{GS} = - 4.5 V, I_D = - 2.9 A	P-Ch		0.074	0.090	
		V_{GS} = 2.5 V, I_D = 3.3 A	N-Ch		0.053	0.065	
		V_{GS} = - 2.5 V, I_D = - 2.3 A	P-Ch		0.113	0.137	
Forward Transconductance[b]	g_{fs}	V_{DS} = 10 V, I_D = 4.2 A	N-Ch		12		S
		V_{DS} = - 10 V, I_D = - 2.9 A	P-Ch		7		
Dynamic[a]							
Input Capacitance	C_{iss}	N-Channel V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	N-Ch		350		pF
			P-Ch		340		
Output Capacitance	C_{oss}		N-Ch		82		
			P-Ch		105		
Reverse Transfer Capacitance	C_{rss}	P-Channel V_{DS} = - 10 V, V_{GS} = 0 V, f = 1 MHz	N-Ch		50		
			P-Ch		95		
Total Gate Charge	Q_g	V_{DS} = 10 V, V_{GS} = 10 V, I_D = 5.5 A	N-Ch		7.7	12	nC
		V_{DS} = - 10 V, V_{GS} = - 10 V, I_D = - 3.7 A	P-Ch		10.5	16	
		N-Channel V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 5.5 A	N-Ch		3.7	6	
			P-Ch		5.3	8	
Gate-Source Charge	Q_{gs}		N-Ch		0.85		
		P-Channel V_{DS} = - 10 V, V_{GS} = - 4.5 V, I_D = - 3.7 A	P-Ch		0.75		
Gate-Drain Charge	Q_{gd}		N-Ch		0.95		
			P-Ch		2		
Gate Resistance	R_g	f = 1 MHz	N-Ch	0.7	3.5	7	Ω
			P-Ch	0.2	10	20	

Notes:
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

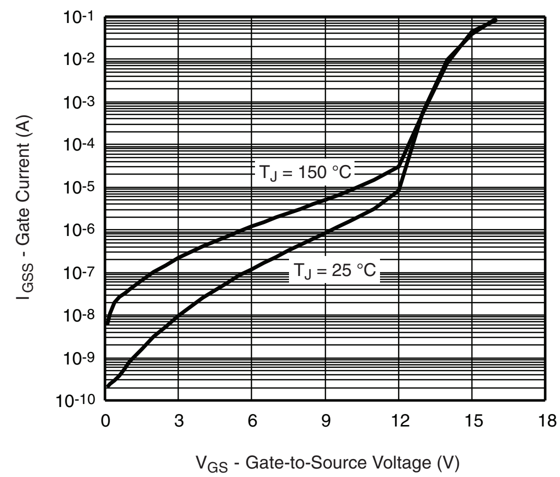
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
Parameter	**Symbol**	**Test Conditions**		**Min.**	**Typ.**	**Max.**	**Unit**
Dynamic[a]							
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 10 V, R_L = 2.3 Ω $I_D \cong$ 4.4 A, V_{GEN} = 4.5 V, R_g = 1 Ω; P-Channel V_{DD} = - 10 V, R_L = 3.3 Ω $I_D \cong$ - 3 A, V_{GEN} = - 4.5 V, R_g = 1 Ω	N-Ch		10	15	ns
			P-Ch		20	30	
Rise Time	t_r		N-Ch		12	20	
			P-Ch		20	30	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		21	35	
			P-Ch		25	40	
Fall Time	t_f		N-Ch		16	25	
			P-Ch		10	15	
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = 10 V, R_L = 2.3 Ω $I_D \cong$ 4.4 A, V_{GEN} = 10 V, R_g = 1 Ω; P-Channel V_{DD} = - 10 V, R_L = 3.3 Ω $I_D \cong$ - 3 A, V_{GEN} = - 10 V, R_g = 1 Ω	N-Ch		5	10	
			P-Ch		5	10	
Rise Time	t_r		N-Ch		10	15	
			P-Ch		10	15	
Turn-Off Delay Time	$t_{d(off)}$		N-Ch		15	25	
			P-Ch		20	30	
Fall Time	t_f		N-Ch		10	15	
			P-Ch		10	15	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C	N-Ch			4.5	A
			P-Ch			- 4.5	
Pulse Diode Forward Current[a]	I_{SM}		N-Ch			15	
			P-Ch			- 15	
Body Diode Voltage	V_{SD}	I_S = 4.4 A, V_{GS} = 0 V	N-Ch		0.8	1.2	V
		I_S = - 3 A, V_{GS} = 0 V	P-Ch		- 0.8	- 1.2	
Body Diode Reverse Recovery Time	t_{rr}	N-Channel I_F = 4.4 A, dI/dt = 100 A/µs, T_J = 25 °C; P-Channel I_F = - 3 A, dI/dt = - 100 A/µs, T_J = 25 °C	N-Ch		15	30	ns
			P-Ch		26	50	
Body Diode Reverse Recovery Charge	Q_{rr}		N-Ch		8	20	nC
			P-Ch		13	25	
Reverse Recovery Fall Time	t_a		N-Ch		8		ns
			P-Ch		14		
Reverse Recovery Rise Time	t_b		N-Ch		7		
			P-Ch		12		

Notes:
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

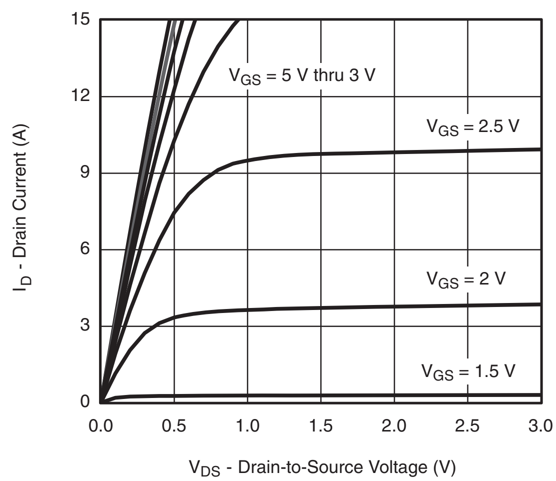
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



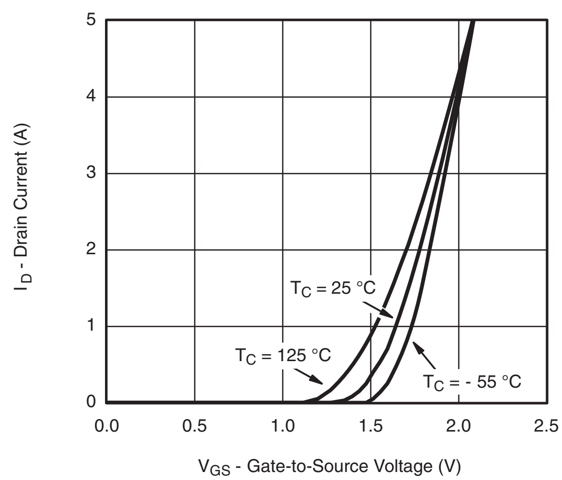
Gate Current vs. Gate-Source Voltage



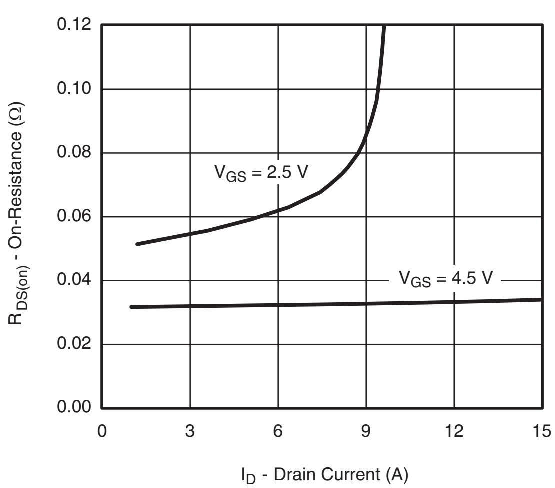
Gate Current vs. Gate-Source Voltage



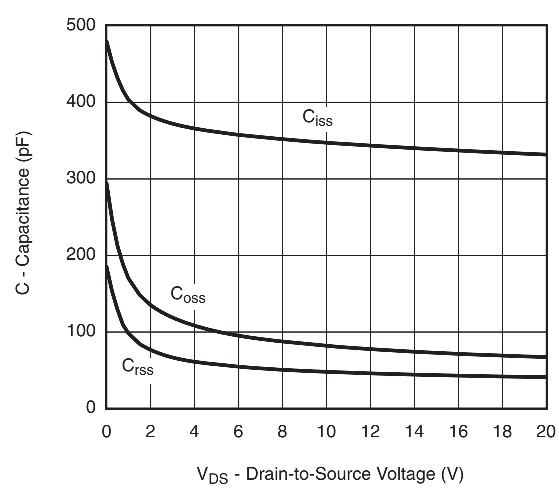
Output Characteristics



Transfer Characteristics

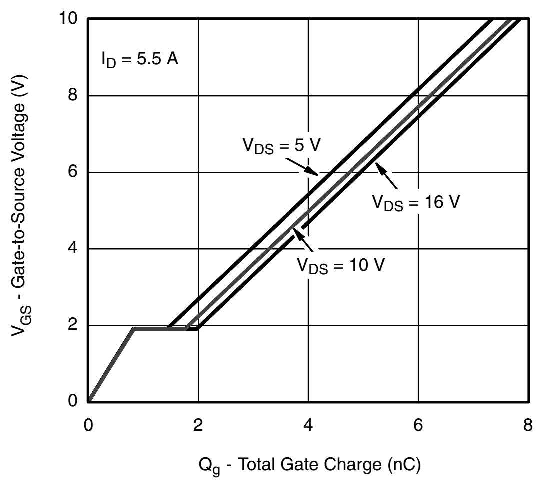


On-Resistance vs. Drain Current and Gate Voltage

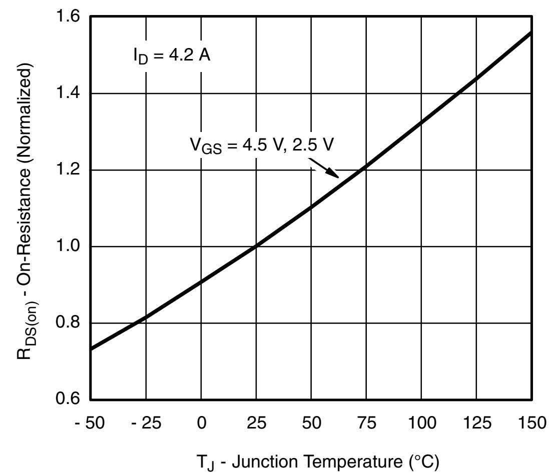


Capacitance

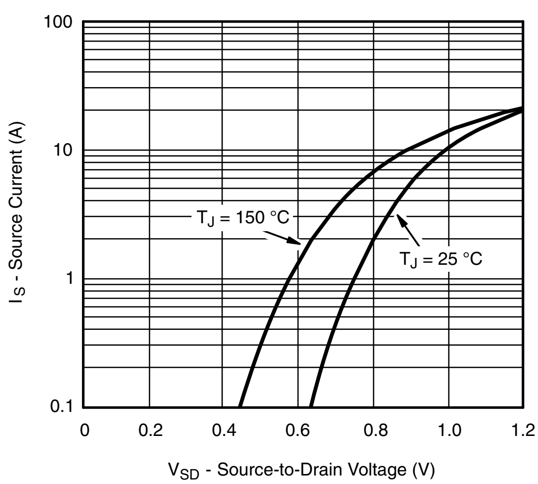
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



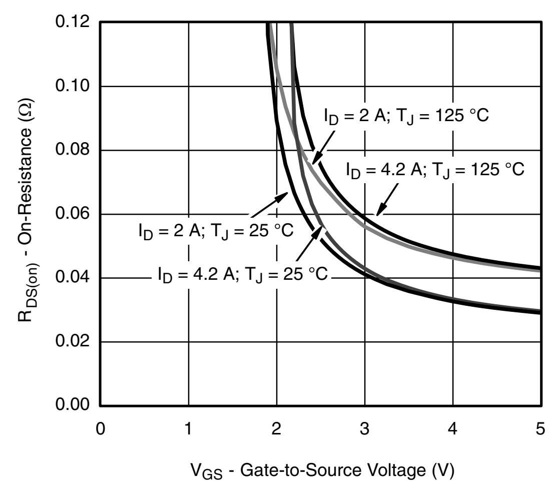
Gate Charge



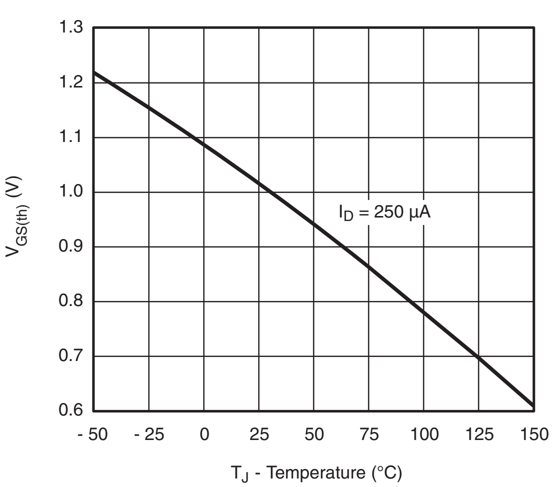
On-Resistance vs. Junction Temperature



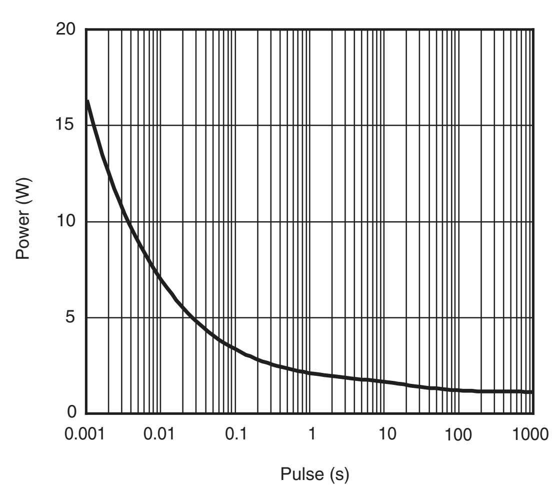
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

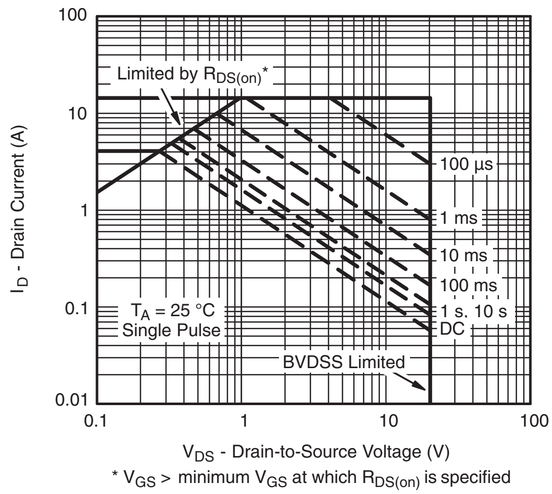


Threshold Voltage

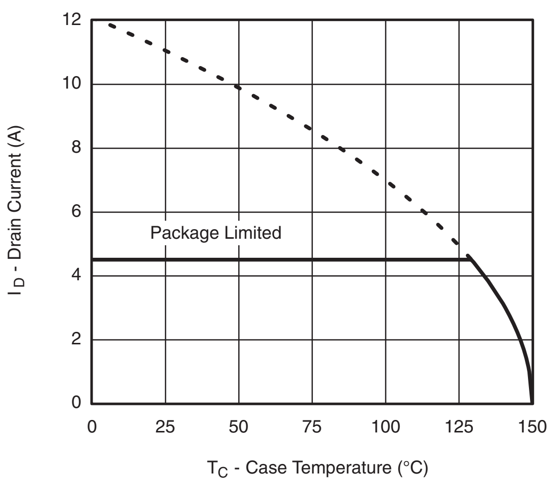


Single Pulse Power (Junction-to-Ambient)

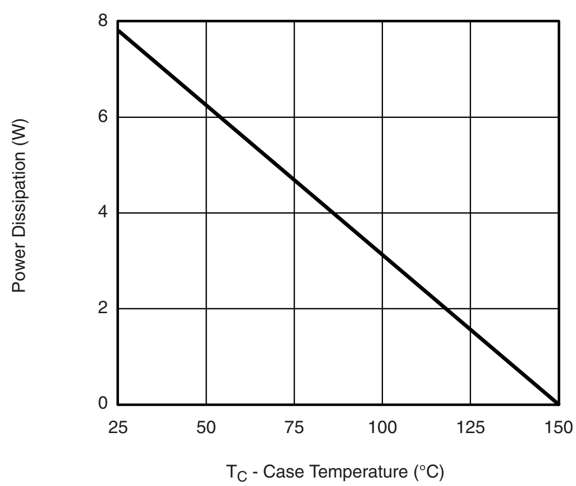
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Safe Operating Area, Junction-to-Ambient



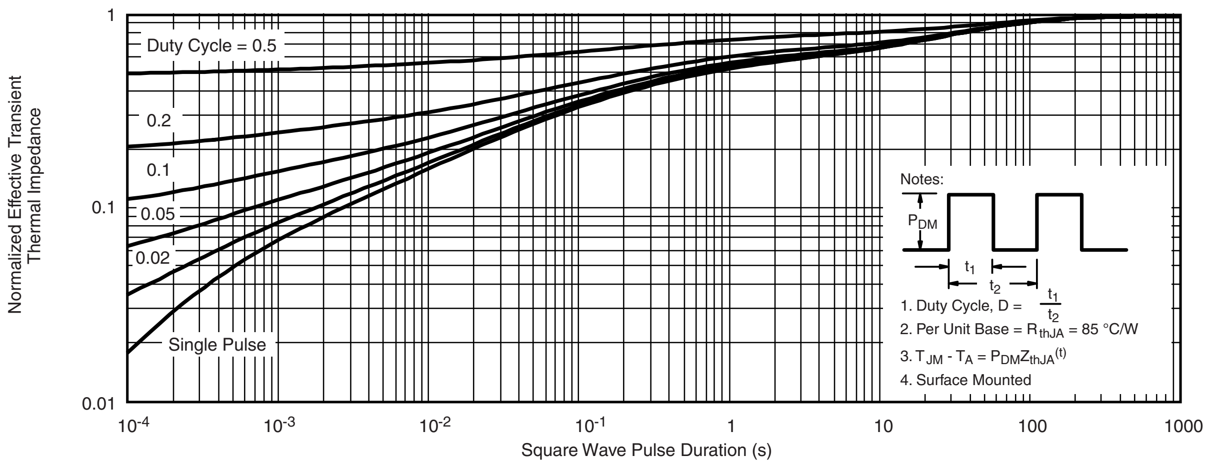
Current Derating*



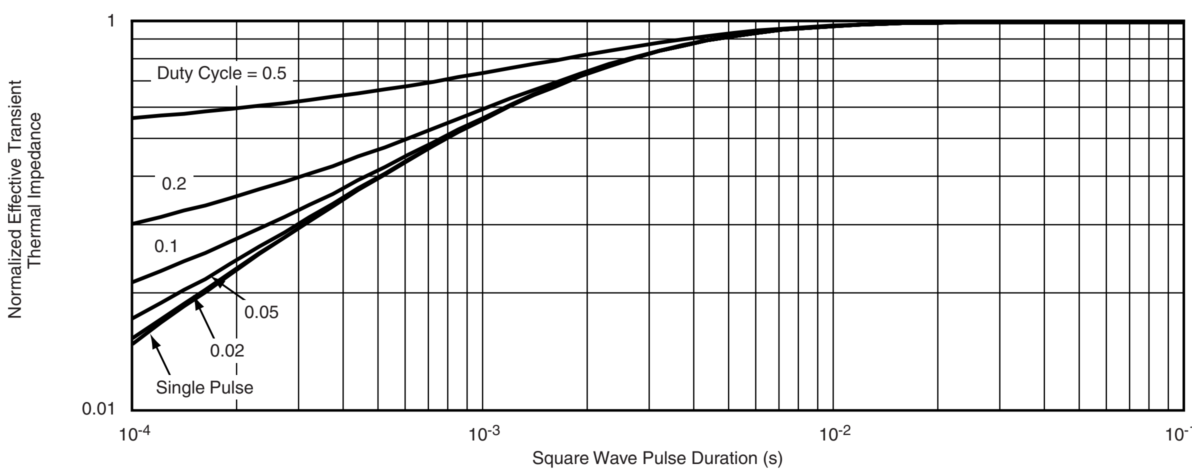
Power Derating

* The power dissipation P_D is based on $T_{J(max.)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

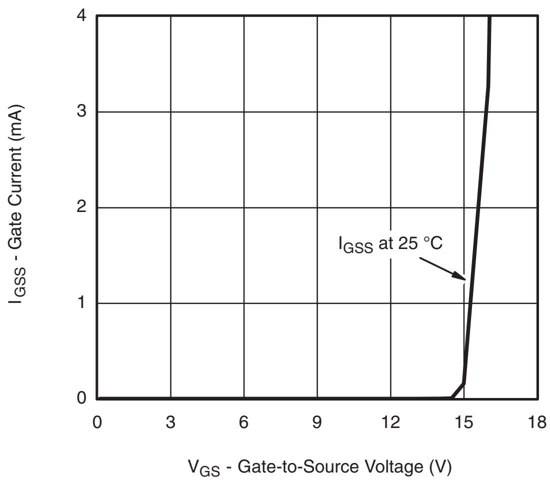


Normalized Thermal Transient Impedance, Junction-to-Ambient

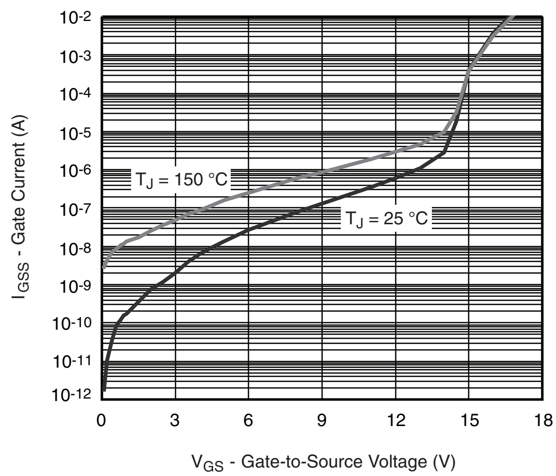


Normalized Thermal Transient Impedance, Junction-to-Case

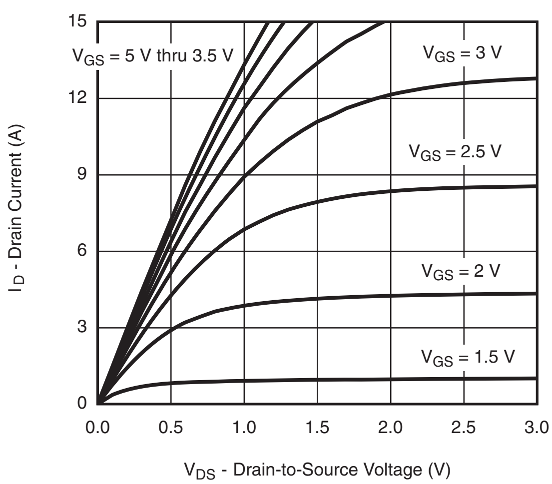
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



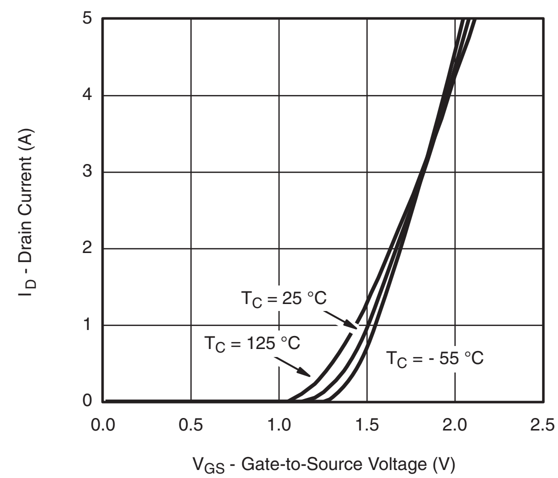
Gate Current vs. Gate-Source Voltage



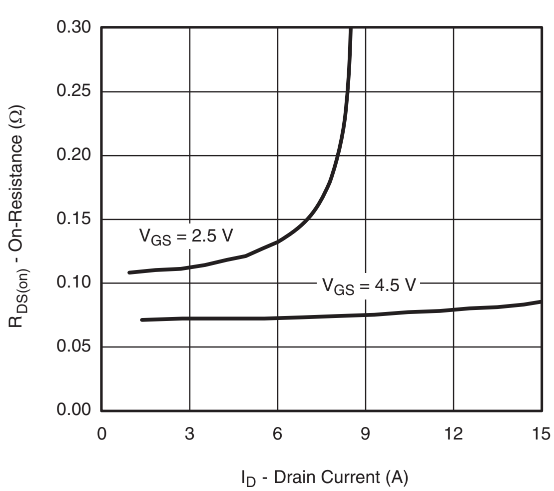
Gate Current vs. Gate-Source Voltage



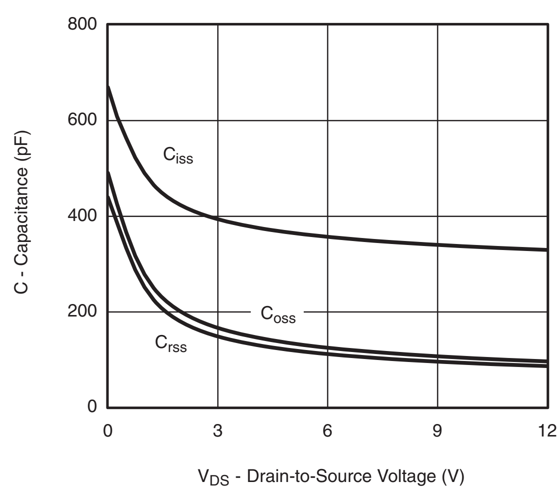
Output Characteristics



Transfer Characteristics

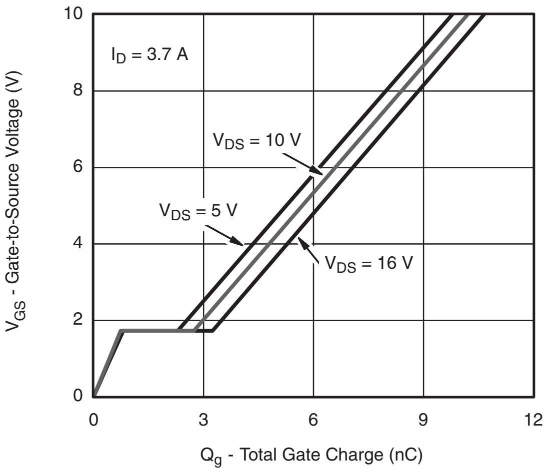


On-Resistance vs. Drain Current and Gate Voltage

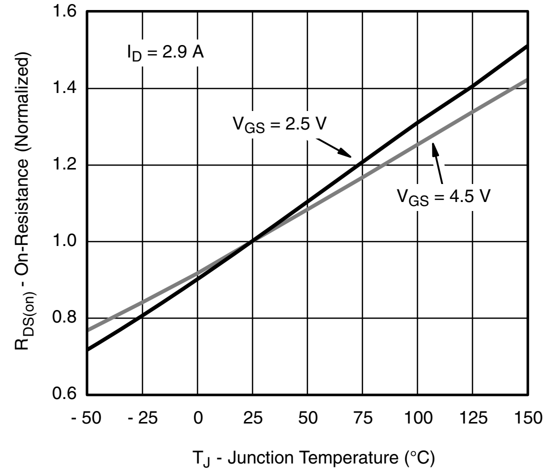


Capacitance

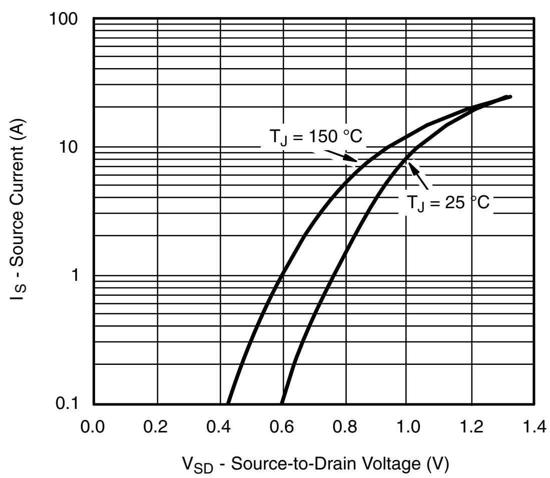
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



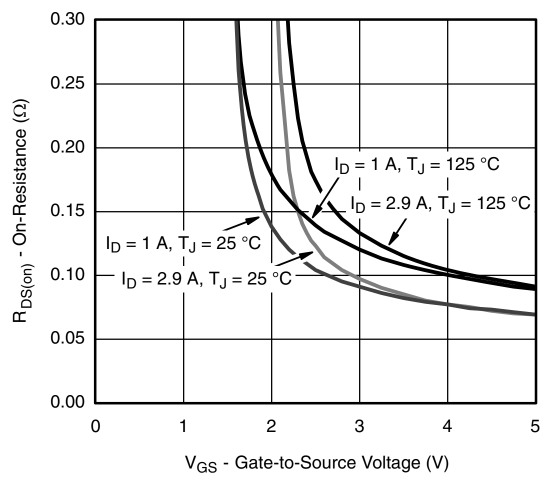
Gate Charge



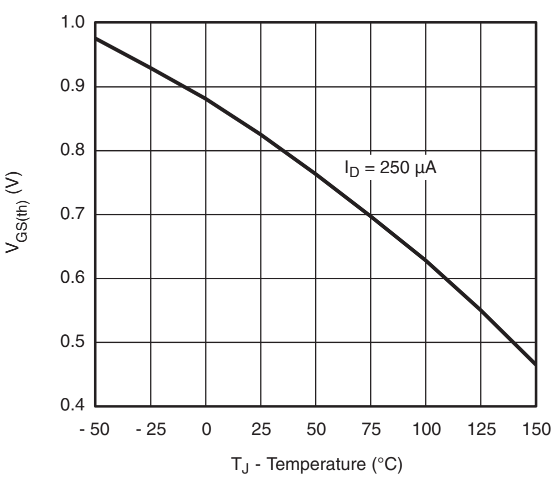
On-Resistance vs. Junction Temperature



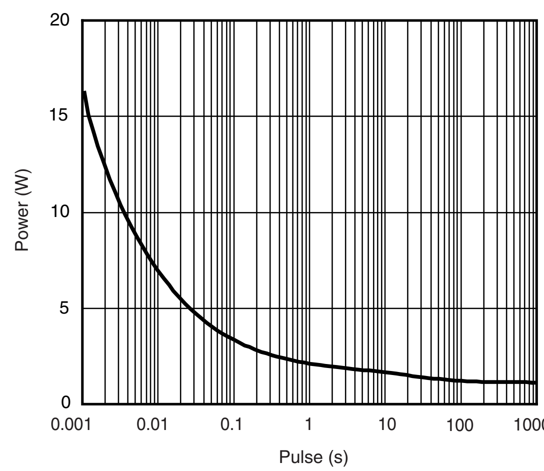
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

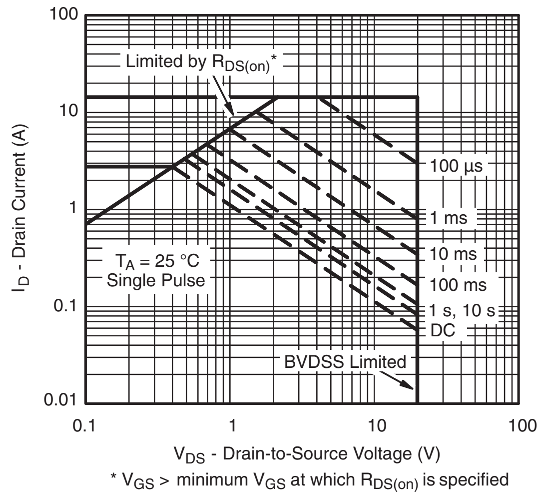


Threshold Voltage

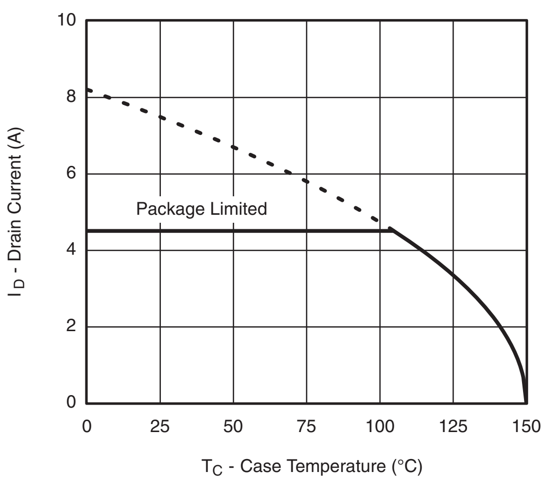


Single Pulse Power (Junction-to-Ambient)

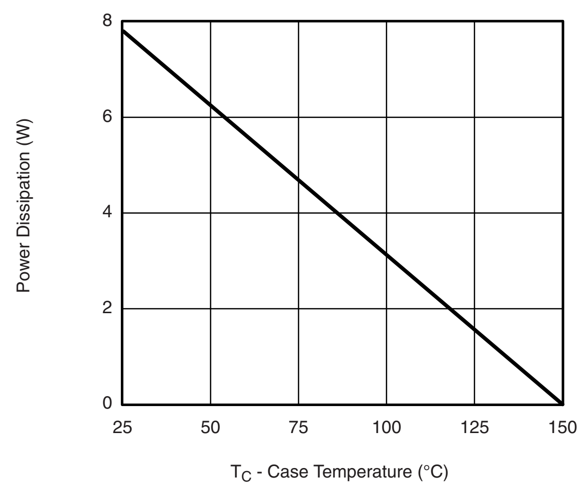
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Safe Operating Area, Junction-to-Ambient



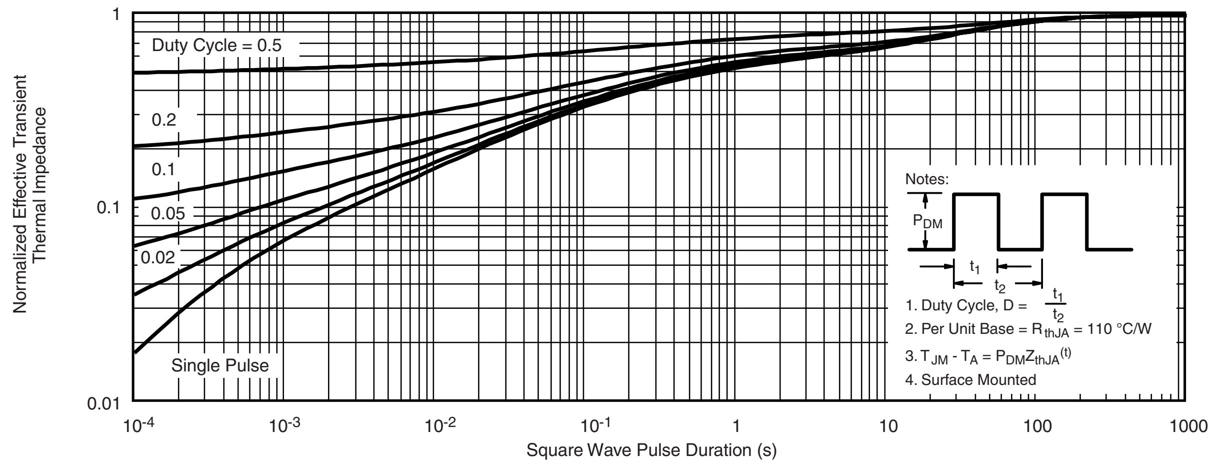
Current Derating*



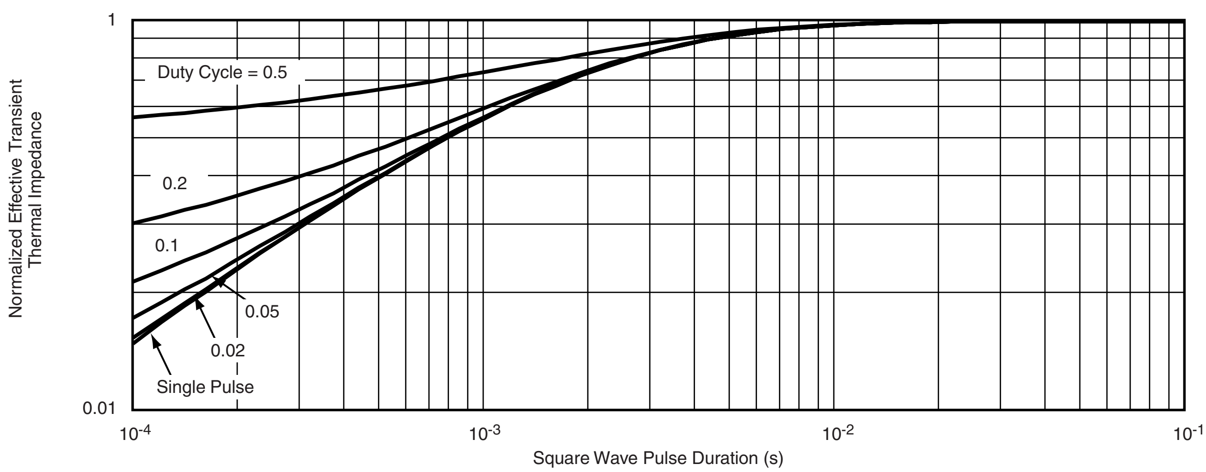
Power Derating

* The power dissipation P_D is based on $T_{J(max.)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

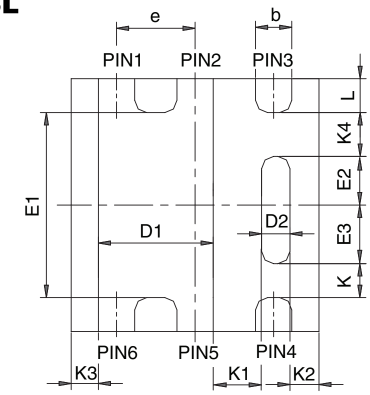


Normalized Thermal Transient Impedance, Junction-to-Ambient

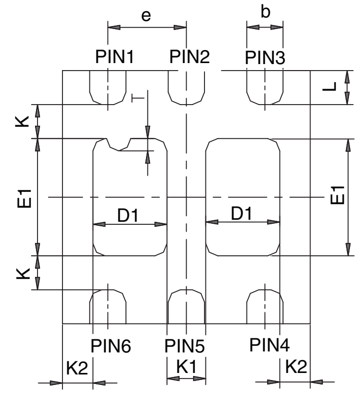


Normalized Thermal Transient Impedance, Junction-to-Case

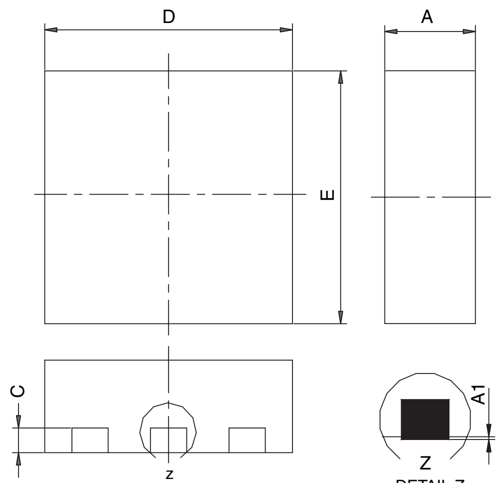
PowerPAK® SC70-6L



BACKSIDE VIEW OF SINGLE



BACKSIDE VIEW OF DUAL



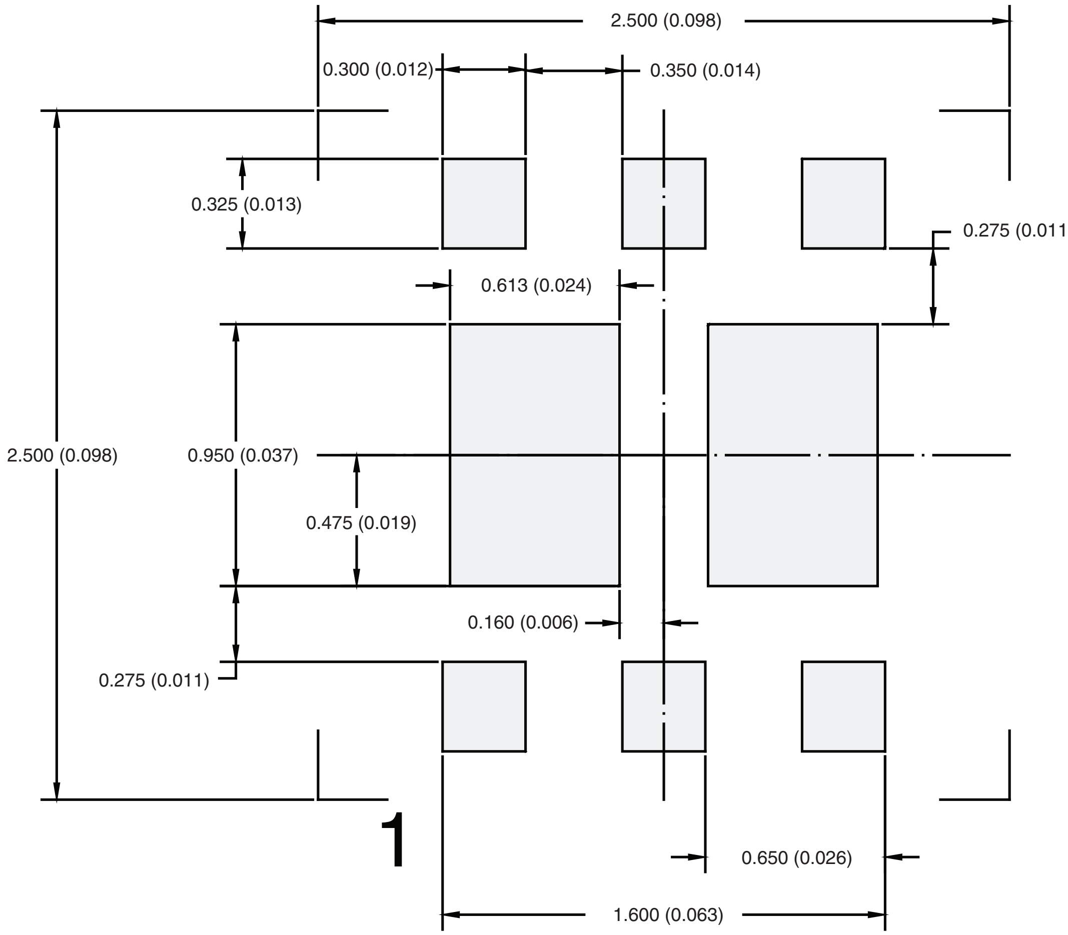
DETAIL Z

Notes:
1. All dimensions are in millimeters
2. Package outline exclusive of mold flash and metal burr
3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
e		0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC	
K		0.275 TYP			0.011 TYP			0.275 TYP			0.011 TYP	
K1		0.400 TYP			0.016 TYP			0.320 TYP			0.013 TYP	
K2		0.240 TYP			0.009 TYP			0.252 TYP			0.010 TYP	
K3		0.225 TYP			0.009 TYP							
K4		0.355 TYP			0.014 TYP							
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006

ECN: C-07431 – Rev. C, 06-Aug-07
DWG: 5934

RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Dual



Dimensions in mm (inches)

Return to Index