55 A VRPower® Integrated Power Stage

DESCRIPTION

The SiC641 and SiC641A are high frequency integrated power stage optimized for synchronous buck applications to offer high current, high efficiency, and high power density performance with very low shutdown current. Packaged in Vishay's proprietary 5 mm x 5 mm MLP package, SiC641 and SiC641A enable voltage regulator designs to deliver up to 55 A continuous current per phase.

The internal power MOSFETs utilize Vishay's latest TrenchFET® technology that delivers industry benchmark performance to significantly reduce switching and conduction losses.

The SiC641 and SiC641A incorporate an advanced MOSFET gate driver IC that features high current driving capability, adaptive dead-time control, an integrated bootstrap switch, and user selectable zero current detection to improve light load efficiency. The driver is also compatible with a wide range of PWM controllers, supports tri-state PWM, and 5 V and 3.3 V PWM logic.

The device also supports PS4 mode to reduce power consumption when the system is in standby state.

The SiC641 and SiC641A offer operating temperature monitoring, protection features, and warning flags that improve system monitoring and reliability.

APPLICATIONS

- Multi-phase VRDs for computing, graphics card and memory
- Intel core processor power delivery
  - V_{CORE}, $V_{GRAPHICS}$, $V_{SYSTEM\ AGENT}$
  - V_{CCGI}
- Up to 16 V rail input DC/DC VR modules

FEATURES

RoHS COMPLIANT
HALOGEN FREE

- Highly efficient
  - Thermally enhanced PowerPAK® MLP55-31L package
  - Vishay's latest TrenchFET technology and low side MOSFET with integrated Schottky diode
    - Integrated, low impedance, bootstrap switch
    - Power MOSFETs optimized for 12 V input stage
    - Supports PS4 mode light load requirement with low shutdown supply current (5 V, 3 µA)
    - Zero current detection for improved light load efficiency
- Highly versatile
  - 5 V and 3.3 V PWM logic with tri-state and hold-off timer
  - 5 V DSBL#, ZCD_EN# logic with PS4 state support
  - High frequency operation up to 2 MHz
- Robust and reliable
  - Delivers in excess of 55 A continuous current, 70 A, peak (10 ms) and 100 A, peak (10 µs)
  - Over current protection
  - Over temperature flag
  - Over temperature protection
  - Undervoltage lockout protection
  - High side MOSFET short detection
- Effective monitoring and reporting
  - Accurate temperature reporting
  - Warnings and faults reporting flag
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

TYPICAL APPLICATION DIAGRAM

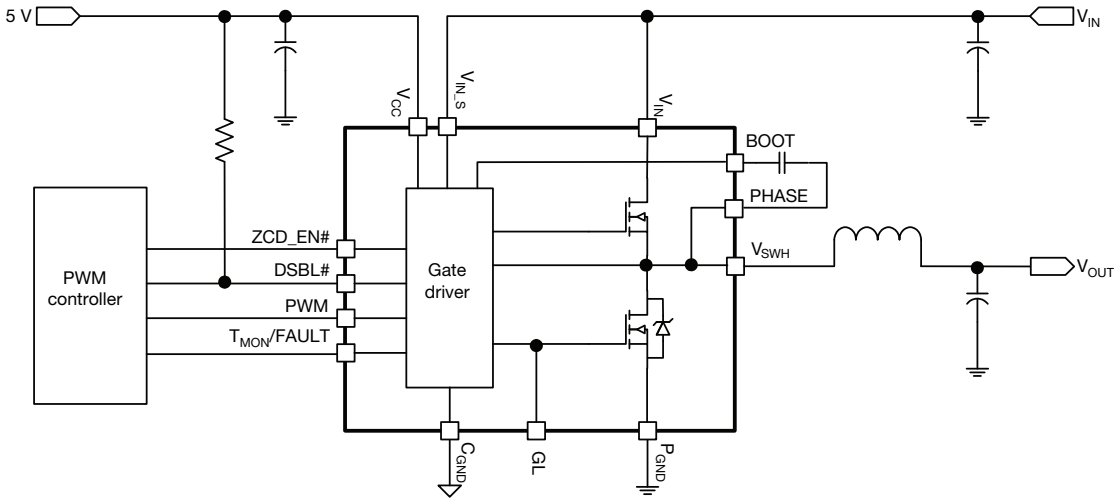
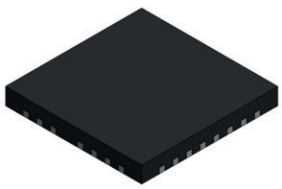
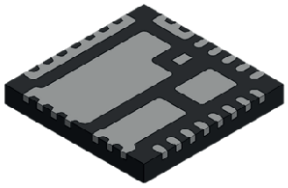
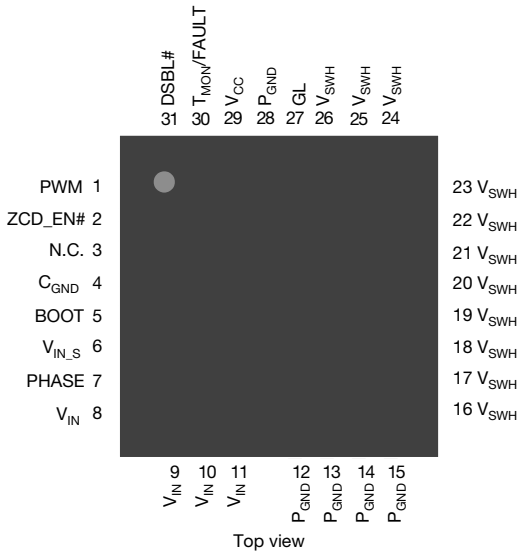


Fig. 1 - Typical Application Diagram

PINOUT CONFIGURATION







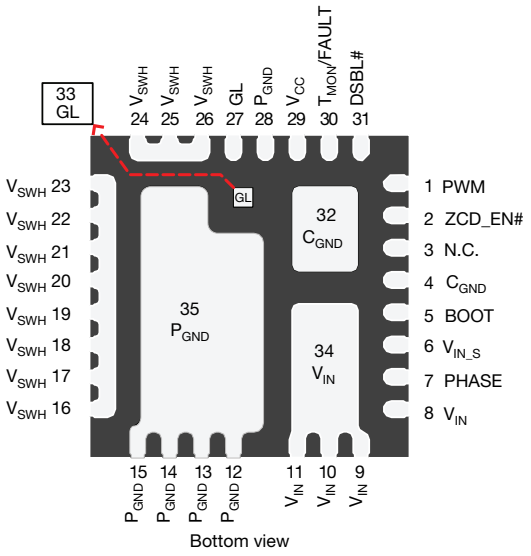
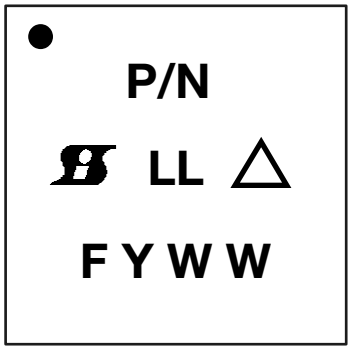


Fig. 2 - Pin Configuration

PIN CONFIGURATION		
PIN NUMBER	**NAME**	**FUNCTION**
1	PWM	PWM input
2	ZCD_EN#	The ZCD_EN# pin enables or disables diode emulation. When ZCD_EN# is LOW, diode emulation is allowed. When ZCD_EN# is HIGH, continuous conduction mode is forced. ZCD_EN# can also be put in a high impedance mode by floating the pin. If ZCD_EN# is floating, the device shuts down and consumes typically 3 µA (10 µA max.) current
3	N.C.	Not connected
5	BOOT	High side driver bootstrap voltage
4, 32	C_{GND}	Analog ground
6	V_{IN_S}	Over current protection input voltage, connect this pin to power stage input voltage
7	PHASE	Return path of high side gate driver
8 to 11, 34	V_{IN}	Power stage input voltage. Drain of high side MOSFET
12 to 15, 28, 35	P_{GND}	Power ground
16 to 26	V_{SWH}	Phase node of the power stage
27, 33	GL	Low side MOSFET gate signal
29	V_{CC}	Supply voltage
30	T_{MON}/FAULT	Temperature monitor output, FAULT flag output
31	DSBL#	Disable input, active low

ORDERING INFORMATION			
PART NUMBER	**PACKAGE**	**MARKING CODE**	**OPTION**
SiC641CD-T1-GE3	PowerPAK MLP55-31L	SiC641	5 V PWM optimized
SiC641ACD-T1-GE3		SiC641A	3.3 V PWM optimized
SiC641DB	Reference board		
SiC641ADB			

PART MARKING INFORMATION



●	=	pin 1 indicator
P/N	=	part number code
	=	Siliconix logo
△	=	ESD symbol
F	=	assembly factory code
Y	=	year code
WW	=	week code
LL	=	lot code

ABSOLUTE MAXIMUM RATINGS

ELECTRICAL PARAMETER	SYMBOL	LIMIT	UNIT
Input voltage	V_{IN}, V_{IN_S}	-0.3 to +24	V
Control logic supply voltage	V_{CC}	-0.3 to +7	
Switch node (DC voltage)	V_{SWH}	-0.3 to +24	
Switch node (AC voltage) (1)		-7 to +35	
BOOT voltage (DC voltage)	V_{BOOT}	32	
BOOT voltage (AC voltage) (2)		40	
BOOT to PHASE (DC voltage)	$V_{BOOT-PHASE}$	-0.3 to +7	
BOOT to PHASE (AC voltage) (3)		-0.3 to +8	
All logic inputs and outputs	PWM, ZCD_EN#, DSBL#, T_{MON}/FAULT	-0.3 to V_{CC} +0.3	
Max. operating junction temperature	T_J	150	°C
Ambient temperature	T_A	-40 to +125	
Storage temperature	T_{stg}	-65 to +150	
Electrostatic discharge protection	Human body model, JESD22-A114	2000	V
	Charged device model, JESD22-C101	1000	

Notes

- Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

(1) The specification values indicated “AC” is V_{SWH} to P_{GND} -7 V (< 20 ns, 10 µJ), min. and 35 V (< 50 ns), max.

(2) The specification value indicates “AC voltage” is V_{BOOT} to P_{GND}, 40 V (< 50 ns) max.

(3) The specification value indicates “AC voltage” is V_{BOOT} to V_{PHASE}, 8 V (< 50 ns) max.

RECOMMENDED OPERATING RANGE

ELECTRICAL PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNIT
Input voltage (V_{IN})	2.5	-	16	V
Control logic supply voltage (V_{CC})	4.5	5	5.5	
BOOT to PHASE ($V_{BOOT-PHASE}$, DC voltage)	4	4.5	5.5	
Thermal resistance from junction to ambient	-	10.6	-	°C/W
Thermal resistance from junction to case	-	1.6	-	

ELECTRICAL SPECIFICATIONS

(ZCD_EN# = 5 V, V_{IN} = 12 V, V_{CC} = 5 V, DSBL# = 5 V, T_A = 25 °C, unless otherwise stated)

PARAMETER	SYMBOL	TEST CONDITION	LIMITS			UNIT
			MIN.	TYP.	MAX.	
POWER SUPPLY						
Control logic supply current	I_{VCC}	V_{PWM} = FLOAT	-	80	-	µA
		V_{PWM} = FLOAT, $V_{ZCD\_EN\#}$ = 0 V	-	120	-	
Drive supply current		f_S = 300 kHz, D = 0.1	-	10.3	20	mA
		f_S = 1 MHz, D = 0.1	-	30	-	
PS4 mode supply current	I_{VCC}	V_{PWM} = $V_{ZCD\_EN\#}$ = FLOAT, T_A = -10 °C to +100 °C	-	3	9	µA
		DSBL# = 0 V	-	3	9	
BOOTSTRAP SUPPLY						
Bootstrap switch $R_{DS(on)}$	R_{BS}	V_{CC} = 5 V	-	3	-	Ω
DSBL# CONTROL INPUT						
DSBL# logic input voltage	$V_{IH\_DSBL\#}$	Input logic high	2	-	-	V
	$V_{IL\_DSBL\#}$	Input logic low	-	-	0.8	
DSBL# input current	$I_{DSBL\#}$	$V_{DSBL\#}$ = 5 V	-	0.25	1	µA
PWM CONTROL INPUT (SiC641)						
Rising threshold	$V_{TH\_PWM\_R}$		3.6	3.9	4.2	V
Falling threshold	$V_{TH\_PWM\_F}$		0.72	1	1.3	
Tri-state voltage	V_{TRI}	V_{PWM} = FLOAT	-	2.5	-	
Tri-state rising threshold	$V_{TRI\_TH\_R}$		1.1	1.35	1.6	
Tri-state falling threshold	$V_{TRI\_TH\_F}$		3.4	3.7	4	
Tri-state rising threshold hysteresis	$V_{HYS\_TRI\_R}$		-	325	-	mV
Tri-state falling threshold hysteresis	$V_{HYS\_TRI\_F}$		-	225	-	
PWM input current	I_{PWM}	V_{PWM} = 5 V	-	-	350	µA
		V_{PWM} = 0 V	-	-	-350	
PWM CONTROL INPUT (SiC641A)						
Rising threshold	$V_{TH\_PWM\_R}$		2.2	2.45	2.7	V
Falling threshold	$V_{TH\_PWM\_F}$		0.72	0.9	1.1	
Tri-state voltage	V_{TRI}	V_{PWM} = FLOAT	-	1.8	-	
Tri-state rising threshold	$V_{TRI\_TH\_R}$		0.9	1.15	1.38	
Tri-state falling threshold	$V_{TRI\_TH\_F}$		1.95	2.2	2.45	
Tri-state rising threshold hysteresis	$V_{HYS\_TRI\_R}$		-	325	-	mV
Tri-state falling threshold hysteresis	$V_{HYS\_TRI\_F}$		-	225	-	
PWM input current	I_{PWM}	V_{PWM} = 3.3 V	-	-	225	µA
		V_{PWM} = 0 V	-	-	-225	
ZCD_EN# CONTROL INPUT (SiC641)						
Rising threshold	$V_{TH\_ZCD\_EN\#\_R}$		3.3	3.6	3.9	V
Falling threshold	$V_{TH\_ZCD\_EN\#\_F}$		1.1	1.4	1.7	
Tri-state voltage	$V_{TRI\_ZCD\_EN\#}$	$V_{ZCD\_EN\#}$ = FLOAT	-	2.5	-	
Tri-state rising threshold	$V_{TRI\_ZCD\_EN\#\_R}$		1.4	1.8	2.1	
Tri-state falling threshold	$V_{TRI\_ZCD\_EN\#\_F}$		2.9	3.15	3.4	
Tri-state rising threshold hysteresis	$V_{HYS\_TRI\_ZCD\#\_R}$		-	600	-	mV
Tri-state falling threshold hysteresis	$V_{HYS\_TRI\_ZCD\#\_F}$		-	450	-	
ZCD_EN# input current	$I_{ZCD\_EN\#}$	$V_{ZCD\_EN\#}$ = 5 V	-	-	100	µA
		$V_{ZCD\_EN\#}$ = 0 V	-	-	-100	

ELECTRICAL SPECIFICATIONS

(ZCD_EN# = 5 V, V_{IN} = 12 V, V_{CC} = 5 V, DSBL# = 5 V, T_A = 25 °C, unless otherwise stated)

PARAMETER	SYMBOL	TEST CONDITION	LIMITS			UNIT
			MIN.	TYP.	MAX.	
ZCD_EN# CONTROL INPUT (SiC641A)						
Rising threshold	$V_{TH\_ZCD\_EN\#\_R}$		2.1	2.4	2.8	V
Falling threshold	$V_{TH\_ZCD\_EN\#\_F}$		0.7	0.9	1.2	
Tri-state voltage	$V_{TRI\_ZCD\_EN\#}$	$V_{ZCD\_EN\#}$ = FLOAT	-	1.8	-	
Tri-state rising threshold	$V_{TRI\_ZCD\_EN\#\_R}$		0.9	1.3	1.5	
Tri-state falling threshold	$V_{TRI\_ZCD\_EN\#\_F}$		1.9	2.1	2.6	
Tri-state rising threshold hysteresis	$V_{HYS\_TRI\_ZCD\#\_R}$		-	325	-	mV
Tri-state falling threshold hysteresis	$V_{HYS\_TRI\_ZCD\#\_F}$		-	250	-	
ZCD_EN# input current	$I_{ZCD\_EN\#}$	$V_{ZCD\_EN\#}$ = 3.3 V	-	-	100	µA
		$V_{ZCD\_EN\#}$ = 0 V	-	-	-100	
TIMING SPECIFICATIONS						
Tri-state to GH/GL rising propagation delay	$t_{PD\_TRI\_R}$	No load, see Fig. 4	-	35	-	ns
Tri-state hold-off time	t_{TSHO}		-	30	-	
GH - turn off propagation delay	$t_{PD\_OFF\_GH}$		-	15	-	
GH - turn on propagation delay (dead time rising)	$t_{PD\_ON\_GH}$		-	30	-	
GL - turn off propagation delay	$t_{PD\_OFF\_GL}$		-	25	-	
GL - turn on propagation delay (dead time falling)	$t_{PD\_ON\_GL}$		-	25	-	
PWM minimum on-time	$t_{PWM\_ON\_MIN.}$		-	30	-	
PS4 exit latency	$t_{PS4EXIT}$		-	-	5.5	µs
UNDER VOLTAGE LOCKOUT						
V_{CC} under voltage lockout	V_{UVLO}	V_{CC} rising, on threshold	-	3.8	4	V
		V_{CC} falling, off threshold	3.4	3.6	-	
V_{CC} under voltage lockout hysteresis	V_{UVLO_HYST}		-	200	-	mV
V_{BOOT} under voltage lockout	V_{BOOT_UVLO}	V_{BOOT} rising, on threshold	-	3.6	3.8	V
		V_{BOOT} falling, off threshold	3.2	3.4	-	
V_{BOOT} under voltage lockout hysteresis	$V_{BOOT\_UVLO\_HYST}$		-	200	-	mV
THERMAL MONITOR AND FAULT FLAG						
Gain	T_{OUT_GAIN}		-	8	-	mV/°C
Offset voltage at 0 °C	V_{OFF_0C}		0.4	0.6	0.8	V
T_{OUT} range 125 °C (temp. reporting)	T_{OUT_125C}		1.4	-	1.836	
FAULT mode	$FAULT_{HIGH}$		2.4	-	3.6	
FAULT drive current	$FAULT_{DRIVE}$		5	-	-	mA
Thermal flag	T_{THDN}		-	140	-	°C
Thermal flag hysteresis	T_{THDN_HYS}		-	25	-	
PROTECTIONS						
Over current protection	I_{OCP}		90	110	-	A
Over temperature protection	T_{SHDN}		-	165	-	°C

Notes

(1) Typical limits are established by characterization and are not production tested

(2) Guaranteed by design

DETAILED OPERATIONAL DESCRIPTION

DSBL# Input, Enable Function

The DSBL# pin shuts down the driver and disables both high side and low side MOSFETs. In this state, standby current is minimized. When DSBL# is low, both PWM and ZCD_EN# internal dividers are disconnected to reduce current consumption. If DSBL# is left unconnected, an internal pull-up resistor will pull the pin to V_{CC} and enable the SiC641.

PWM Input with Tri-state Function

The PWM input receives the PWM control signal from the VR controller IC. The PWM input is designed to be compatible with standard controllers using two state logic (H and L) and advanced controllers that incorporate tri-state logic (H, L and tri-state) on the PWM output. For two state logic, the PWM input operates as follows. When PWM is driven above $V_{PWM\_TH\_R}$ the low side is turned OFF and the high side is turned ON. When PWM input is driven below $V_{PWM\_TH\_F}$ the high side is turned OFF and the low side is turned ON. For tri-state logic, the PWM input operates as previously stated for driving the MOSFETs when PWM is logic high and logic low. However, there is a third state that is entered as the PWM output of a tri-state compatible controller enters its high impedance state. The high impedance state of the controller's PWM output allows the SiC641 to pull the PWM input into the tri-state region (see definition of PWM logic and tri-state, fig. 4). If the PWM input stays in this region for the tri-state hold-off period, t_{TSHO}, both high side and low side MOSFETs are turned OFF. The function allows the VR phase to be disabled without negative output voltage swing caused by inductor ringing and saves a Schottky diode clamp. The PWM and tri-state regions are separated by hysteresis to prevent false triggering. The SiC641 incorporates PWM voltage thresholds that are compatible with 5 V logic.

Diode Emulation Mode and PS4 Mode (ZCD_EN#)

The ZCD_EN# pin enables or disables diode emulation mode. When ZCD_EN# is driven below $V_{TH\_ZCD\_EN\#\_F}$, diode emulation is allowed. When ZCD_EN# is driven above $V_{TH\_ZCD\_EN\#\_R}$, continuous conduction mode is forced. Diode emulation mode allows for higher converter efficiency under light load situations. With diode emulation active, the SiC641 will detect the zero current crossing of the output inductor and turn off the low side MOSFET. This ensures that discontinuous conduction mode (DCM) is achieved. Diode emulation is asynchronous to the PWM signal, therefore, the SiC641 will respond to the ZCD_EN# input immediately after it changes state.

The ZCD_EN# pin can be floated resulting in a high impedance state. The SiC641 will pull a floated ZCD_EN# to the internally set tri-state level. A tri-state ZCD_EN# combined with a tri-stated PWM output will shut down the SiC641, reducing current consumption to typically 3 µA. This is an important feature in achieving the low standby current required in the PS4 state in ultrabooks and notebooks.

Voltage Input (V_{IN})

This is the power input to the drain of the high side power MOSFET. This pin is connected to the high power intermediate BUS rail.

Switch Node (V_{SWH} and PHASE)

The switch node, V_{SWH}, is the power stage output. This is the output applied to the power inductor and output filter to deliver the output for the buck converter. The PHASE pin is internally connected to the switch node V_{SWH}. This pin is to be used exclusively as the return pin for the BOOT capacitor.

Ground Connections (C_{GND} and P_{GND})

P_{GND} (power ground) should be externally connected to C_{GND} (control analog ground). The layout of the printed circuit board should be such that the inductance separating C_{GND} and P_{GND} is minimized. Transient differences due to inductance effects between these two pins should not exceed 0.5 V.

Control and Drive Supply Voltage Input (V_{CC})

V_{CC} is the bias supply for the control IC and for the gate drivers.

Bootstrap Circuit (BOOT)

A bootstrap switch and an external bootstrap capacitor form a charge pump that supplies voltage to the BOOT pin. An integrated bootstrap switch is incorporated so that only an external capacitor is necessary to complete the bootstrap circuit. Connect a bootstrap capacitor with one leg tied to BOOT pin and the other tied to PHASE pin.

Shoot-Through Protection and Adaptive Dead Time

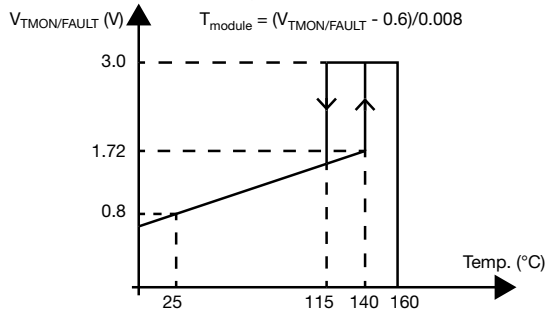
The SiC641 has an internal adaptive logic to avoid shoot-through and optimize dead time. The shoot-through protection ensures that both high side and low side MOSFETs are not turned on at the same time. The adaptive dead time control operates as follows. The high side and low side gate voltages are monitored to prevent one from turning on until the other gate voltage is sufficiently low (< 1 V). Built-in delays also ensure that one power MOS is completely off, before the other can be turned on. This feature helps to adjust dead time as gate transitions change with respect to output current and temperature.

Under Voltage Lockout (UVLO)

During the start up cycle the UVLO disables the gate drive, holding high side and low side MOSFET gates low until the supply voltage has reached a point at which the logic circuitry can be safely activated. The SiC641 also incorporates logic to clamp the gate drive signals to zero when the UVLO falling edge triggers the shutdown of the device.

T_{MON}/FAULT Temperature Monitor and Fault Flag Functions

The T_{MON}/FAULT output is used to report operating conditions detected by the logic of the driver that require attention.
A fault is reported by the T_{MON}/FAULT output going high to 3.3 V.
The reported conditions are high temperature, insufficient bootstrap voltage, persistent over-current, high side MOSFET short.
The T_{MON}/FAULT output also reports the operating temperature of the SiC641.
The temperature is converted to a voltage with a conversion gain of 8 mV/°C and a target value of 600 mV at 0 °C.



In a multi-phase topology, all T_{MON}/FAULT signals are connected to the PWM controller and will indicate the temp. of the warmest device.
If the operating temperature exceeds 140 °C the T_{MON}/FAULT output will signal a fault condition. The fault is reset when the temperature is below the temperature hysteresis threshold.

For proper operation, the T_{MON} output must be biased with a resistor to ground. A 1 kΩ resistor is recommended.The SiC641 also has an over temperature shutdown feature that stops operation when the temperature is above 160 °C.
The over temperature shutdown fault is reset by DISBL# cycling or power cycling.

Over Current Protection Function

The SiC641 is equipped with over-current protection.
An over-current condition will also be reported through the T_{MON}/FAULT flag. The flag is automatically reset after 128 switching cycles that do not trigger the protection.
When the output current exceeds safe operating levels the SiC641 will protect the power devices by forcing an early termination of the high side conduction time and eventually folding the operating frequency (skipping PWM cycles) as needed.

High Side MOSFET Short Detection

A failure of the high side MOSFET may cause significant system damage. For this reason the SiC641 monitors the switching node (PHASE) cycle by cycle in order to promptly detect a short of the high side power device.
After four consecutive HS short condition cycles are detected, the SiC641 will report the fault with the T_{MON}/FAULT flag, and will ignore the incoming PWM signal. The low side MOSFET is activated to protect the load from high voltage.
The fault flag can only be reset by cycling power to the driver's logic.

FUNCTIONAL BLOCK DIAGRAM

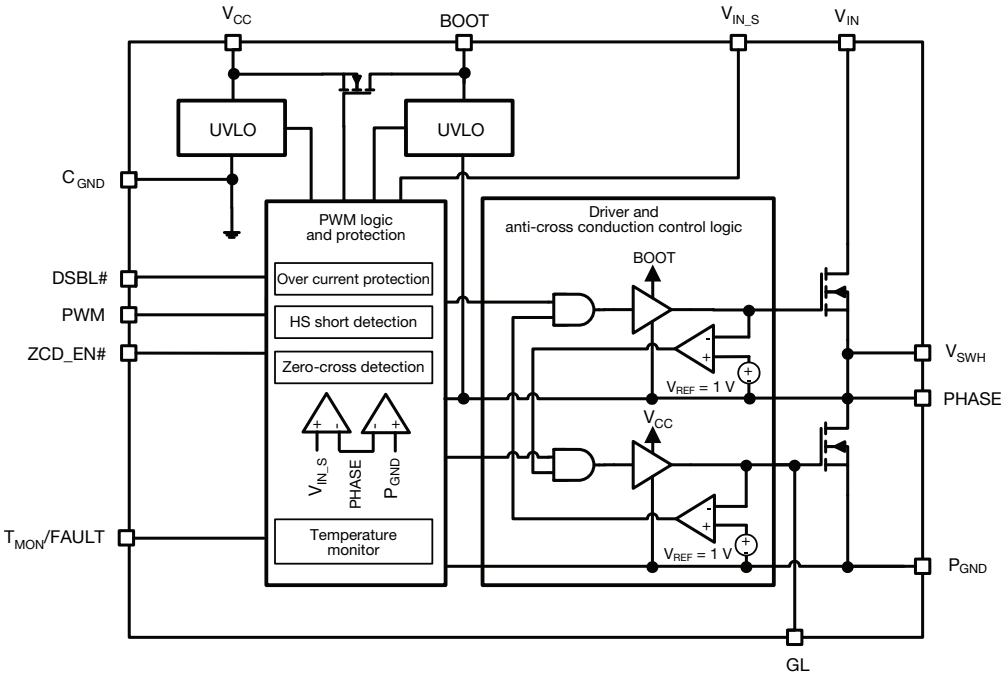


Fig. 3 - Functional Block Diagram

DEVICE TRUTH TABLE				
DSBL#	**ZCD_EN#**	**PWM**	**GH**	**GL**
L	X	X	L	L
H	Tri-state	X	L	L
H	L	L	L	H, I_L > 0 A L, I_L < 0 A
H	L	H	H	L
H	L	Tri-state	L	L
H	H	L	L	H
H	H	H	H	L
H	H	Tri-state	L	L

PWM TIMING DIAGRAM

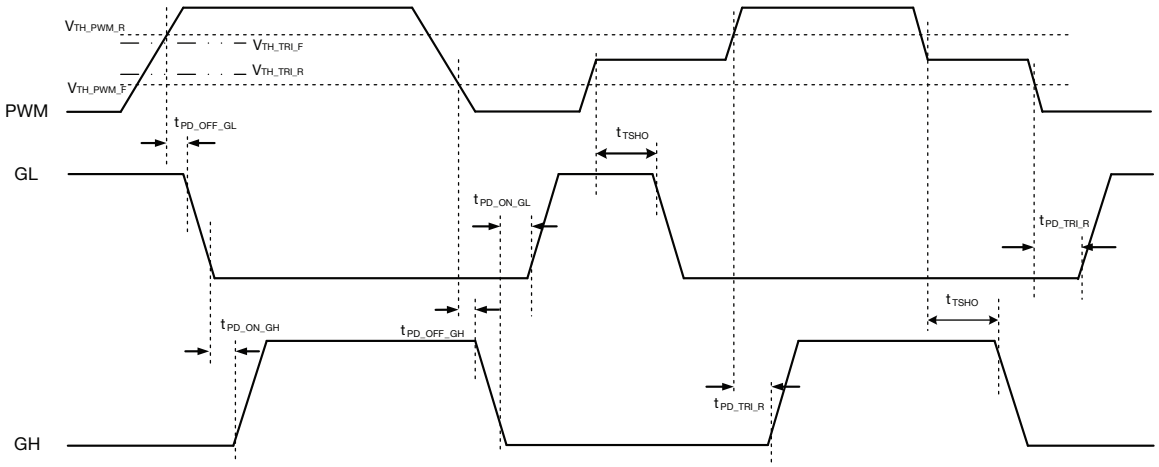


Fig. 4 - Definition of PWM Logic and Tri-state

ZCD_EN# - PS4 EXIT TIMING

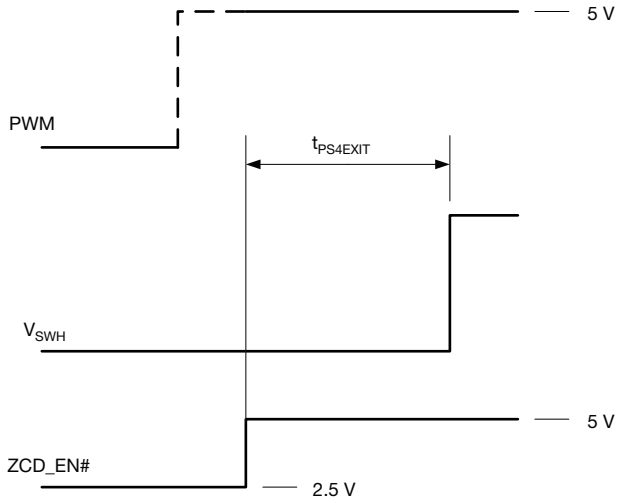


Fig. 5 - ZCD_EN# - PS4 Exit Timing

ELECTRICAL CHARACTERISTICS

Test condition: V_{IN} = 12 V (unless otherwise stated), V_{CC} = 5 V, ZCD_EN# = 5 V, DSBL# = 5 V, V_{OUT} = 1.05 V, L_{OUT} = 220 nH (DCR = 0.29 mΩ), T_A = 25 °C, natural convection cooling (all power loss and normalized power loss curves show SiC641 losses only unless otherwise stated)

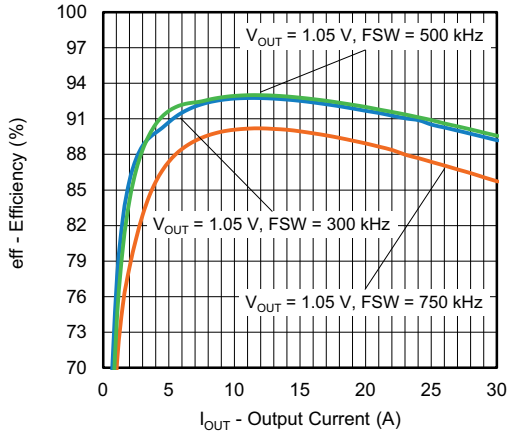


Fig. 6 - Efficiency vs. Output Current (V_{IN} = 12 V)

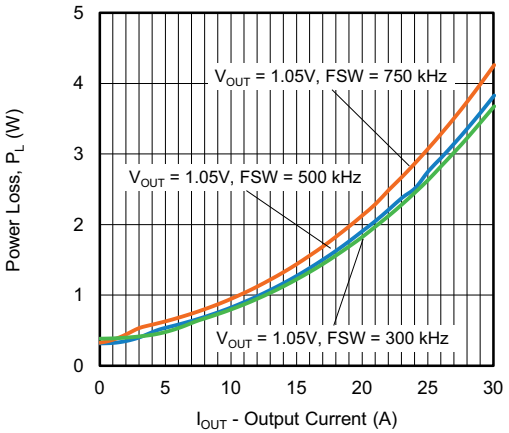


Fig. 8 - Power Loss vs. Output Current (V_{IN} = 12 V)

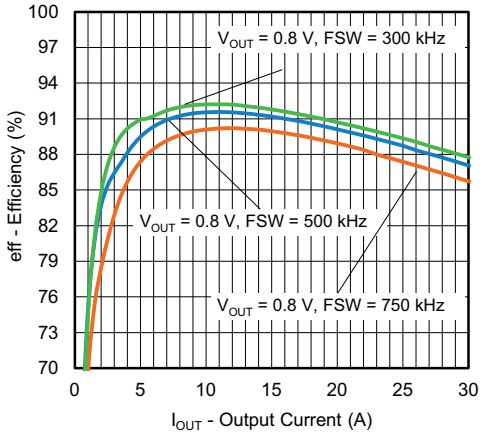


Fig. 7 - Efficiency vs. Output Current (V_{IN} = 12 V)

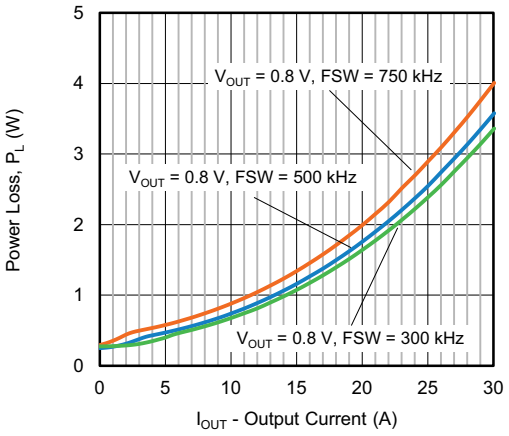


Fig. 9 - Power Loss vs. Output Current (V_{IN} = 12 V)

ELECTRICAL CHARACTERISTICS

Test condition: V_{IN} = 13 V (unless otherwise stated), V_{CC} = 5 V, ZCD_EN# = 5 V, DSBL# = 5 V, V_{OUT} = 1.05 V, L_{OUT} = 220 nH (DCR = 0.29 mΩ), T_A = 25 °C, natural convection cooling (all power loss and normalized power loss curves show SiC641 losses only unless otherwise stated)

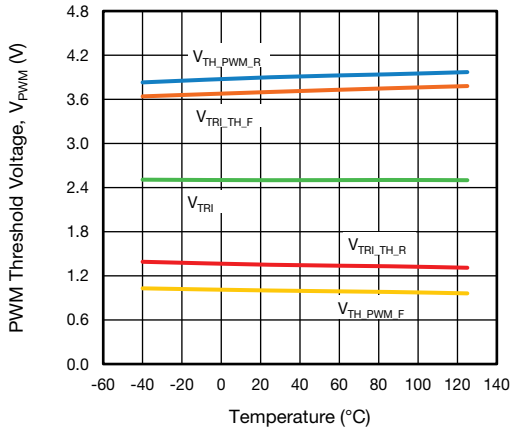


Fig. 10 - PWM Threshold vs. Temperature

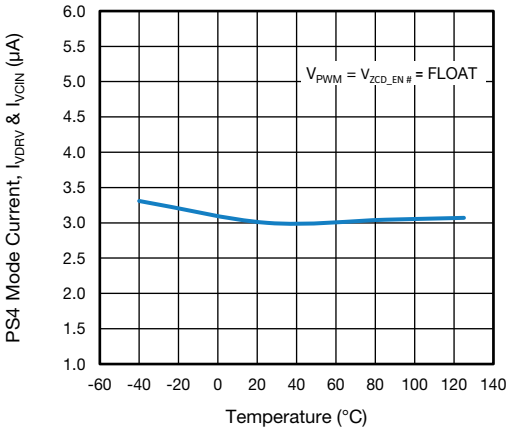


Fig. 12 - PS4 Mode Current vs. Temperature

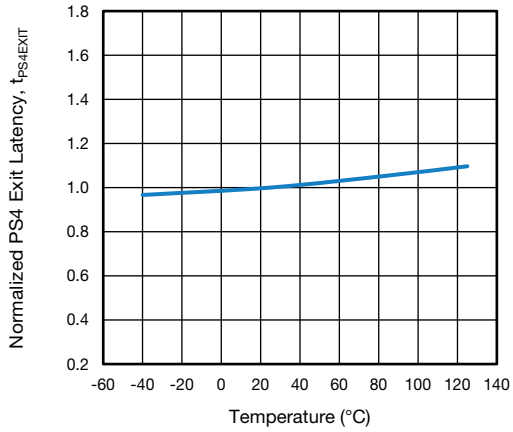
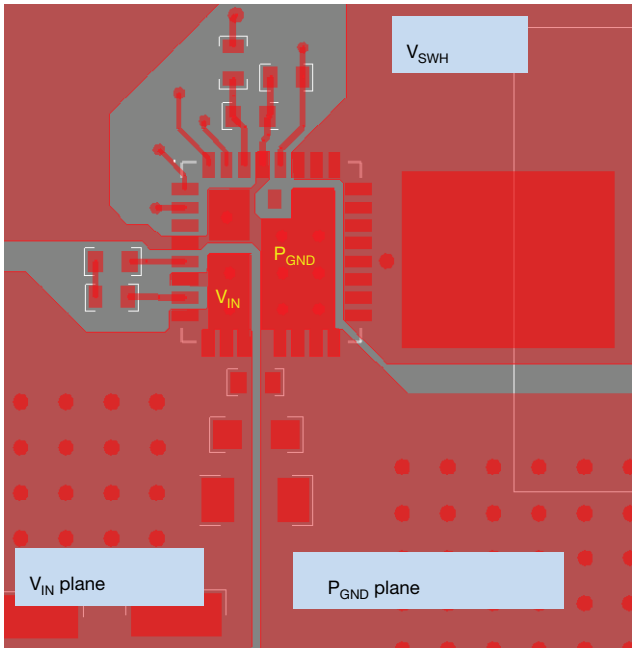


Fig. 11 - PS4 Exit Latency vs. Temperature

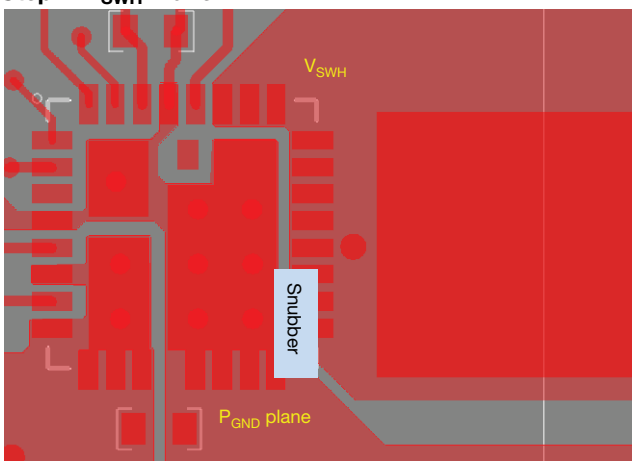
PCB LAYOUT RECOMMENDATIONS

Step 1: V_{IN} / GND Planes and Decoupling



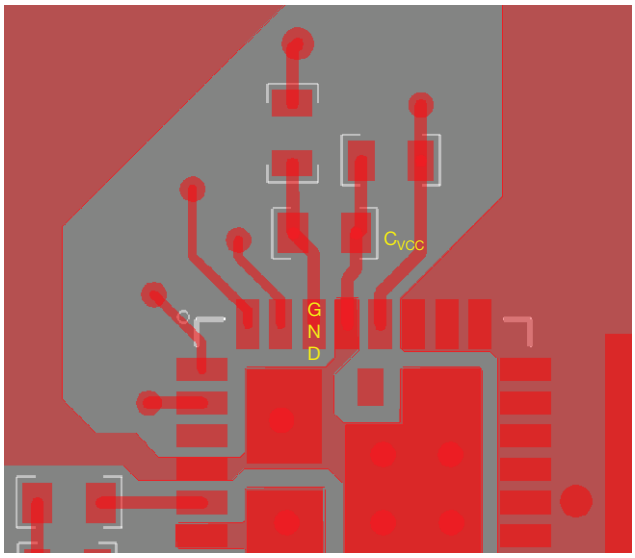
1. Layout V_{IN} and P_{GND} planes as shown above
2. Ceramic capacitors should be placed right between V_{IN} and P_{GND}, and very close to the device for best decoupling effect
3. Difference values / packages of ceramic capacitors should be used to cover entire decoupling spectrum e.g. 1210, 0805, 0603, and 0402
4. Smaller capacitance value, closer to device V_{IN} pin(s) - better high frequency noise absorbing

Step 2: V_{SWH} Plane



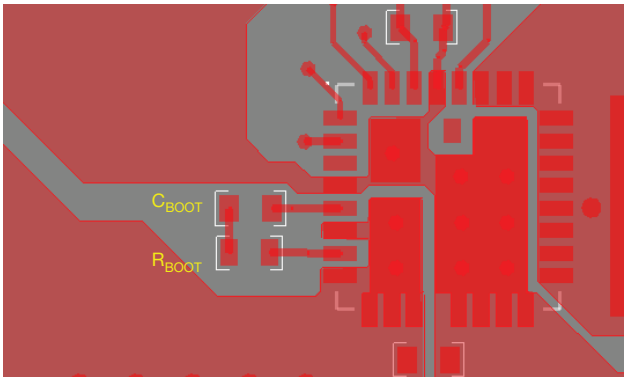
1. Connect output inductor to DrMOS with large plane to lower the resistance
2. If any snubber network is required, place the components as shown above and the network can be placed at bottom

Step 3: V_{CIN} / V_{DRV} Input Filter



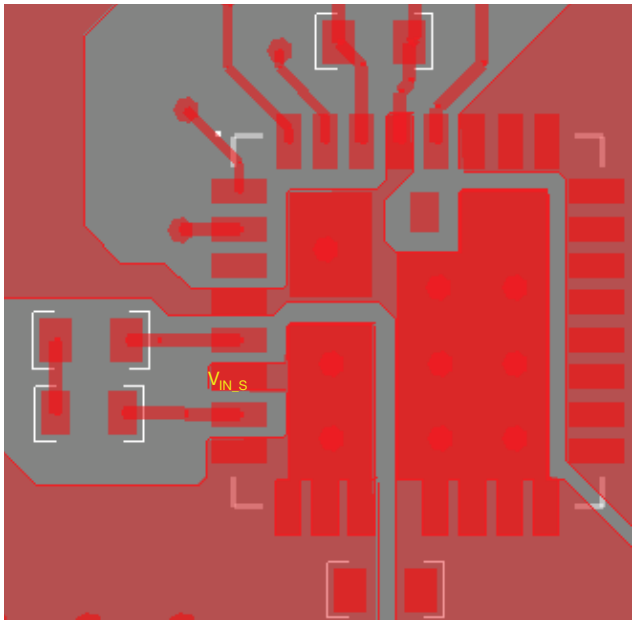
1. The V_{CC} input filter ceramic cap should be placed very close to DrMOS
2. C_{VCC} cap should be placed between pin 28 (P_{GND} of driver IC) and pin 29 to provide maximum instantaneous driver current for low side MOSFET during switching cycle

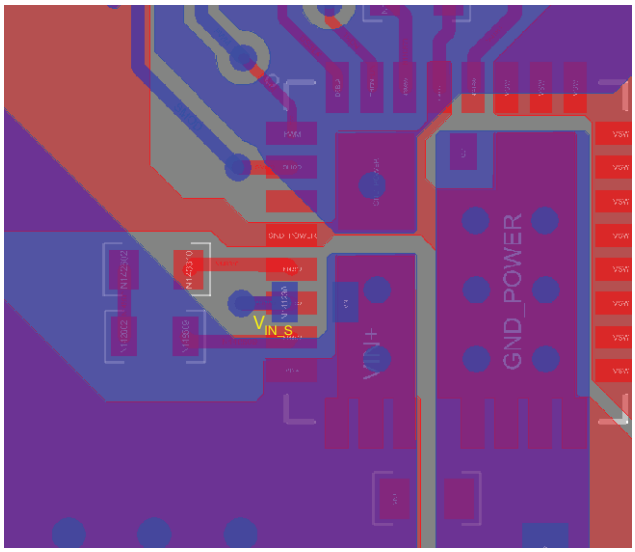
Step 4: BOOT Resistor and Capacitor Placement



1. These components need to be placed very close to DrMOS, right between PHASE (pin 7) and BOOT (pin 5)
2. To reduce parasitic inductance, chip size 0402 can be used

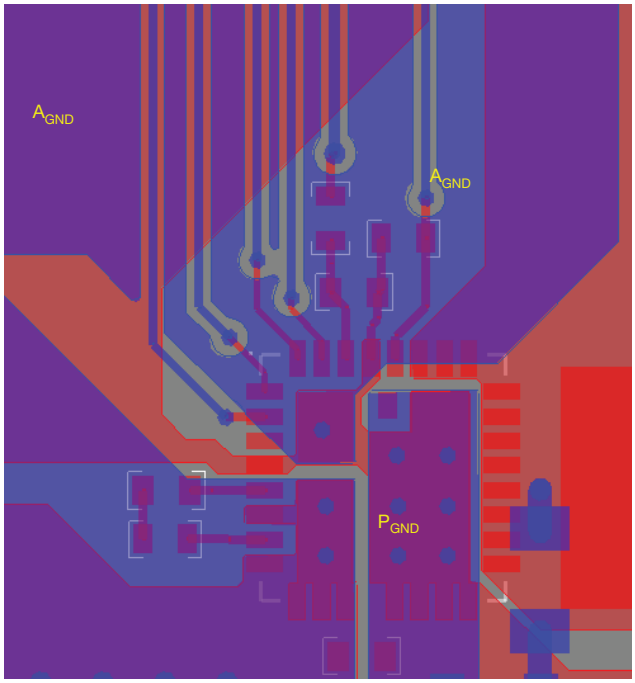
Step 5: V_{IN_S} Connection





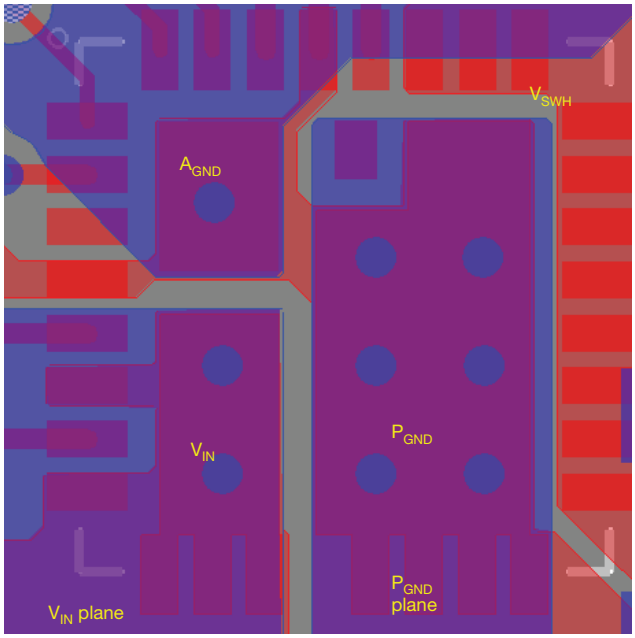
1. V_{IN_S} (pin 6) is used to detect HS MOSFET over current. Connect this pin to the V_{IN} pad
2. To keep the connection flexibility, V_{IN_S} (pin 6) can be connected with V_{IN} through a Via and resistor like the right side. Floating the V_{IN_S} pin by unpopulating the resistor will NOT affect normal operation, but this will make the device lose HS OCP function

Step 6: Signal Routing



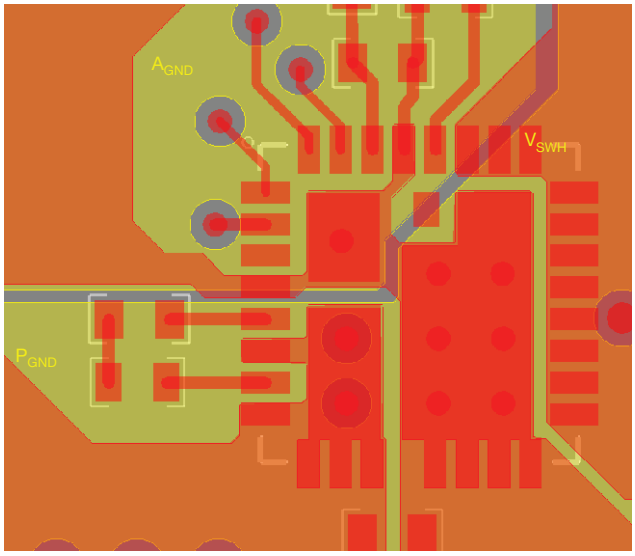
1. Route the PWM / SMOD / DSBL / THDN signal traces out of the top left corner next DrMOS pin1
2. PWM signal is very important signal, both signal and return traces need to pay special attention of not letting this trace cross any power nodes on any layer
3. It is best to “shield” them with GND island form power switching nodes, e.g. V_{SWH}, to improve signal integrity
4. GL (pin27) has been connected with GL pad internally and does not to connect externally

Step 7: Adding Thermal Relief Vias



1. Thermal relief Vias can be added on the V_{IN} and GND pads to utilize inner layers for high current and thermal dissipation
2. To achieve better thermal performance, additional Vias can be put on V_{IN} plane and P_{GND} plane
3. V_{SWH} pad is a noise source and not recommended to put Vias on this plane
4. 8 mil drill for pads and 10 mils drill for plane can be the optional Via size with 40 mils pitch. The Vias on pad may drain solder during assembly and cause assembly issue. Please consult with the assembly house for guideline

Step 8: Ground Connection



1. It is recommended to make single connection between A_{GND} and P_{GND} and this connection can be done on top layer
2. It is recommended to make the whole inner 1 layer (next to top layer) ground plane and separate them into A_{GND} and P_{GND} plane
3. These ground planes provide shielding between noise source on top layer and signal trace on bottom layer

Multi-Phases VRPower PCB Layout

The following is an example of 6 phase layout. As can be seen, all the VRPower stages are lined in X-direction compactly with decoupling capacitors next to them. The inductors are placed as close as possible to the SiC641 to minimize the PCB copper loss. Vias are applied on all PADs (V_{IN}, P_{GND}, C_{GND}) of the SiC641 to ensure that both electrical and thermal performance are optimized. Large copper planes are used for all high current loops, such as V_{IN}, V_{SWH}, V_{OUT} and P_{GND}. These copper planes are duplicated in other layers to minimize the inductance and resistance. All the control signals are routed from the SiC641 to a controller placed to the north of the power stage through inner layers to avoid the overlap of high current loops. This achieves a compact design with the output from the inductors feeding a load located to the south of the design as shown in the figure.

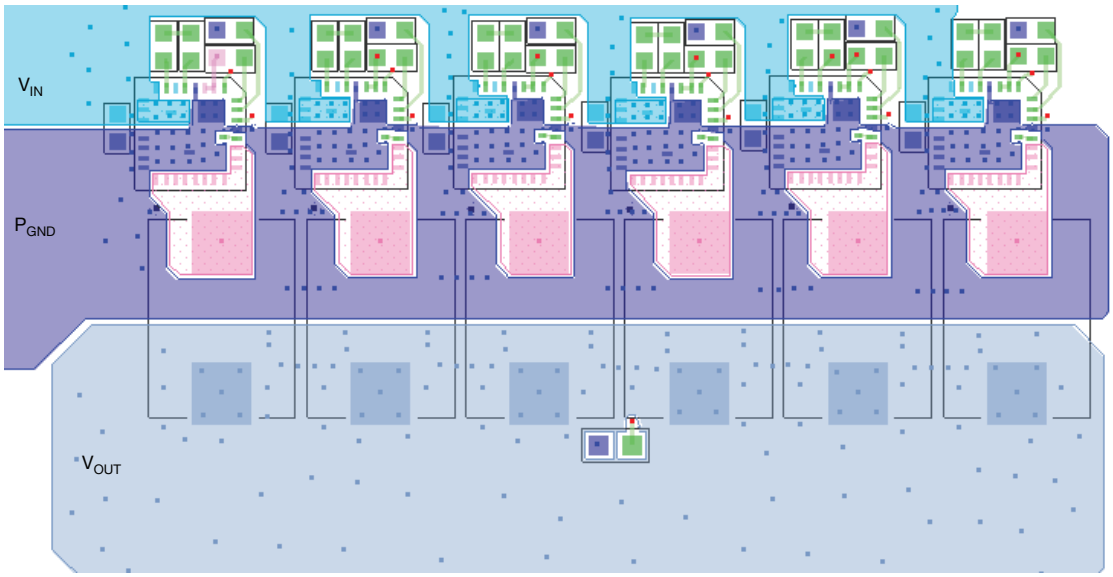


Fig. 13 - Multi-Phase VRPower Layout Top View

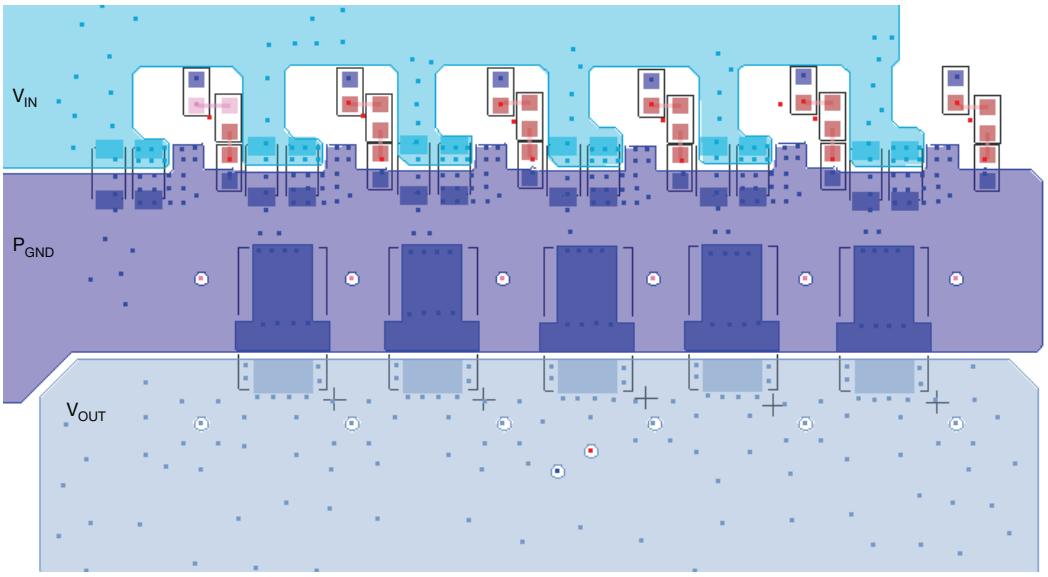


Fig. 14 - Multi-Phase VRPower Layout Bottom View

PRODUCT SUMMARY		
Part number	SiC641	SiC641A
Description	55 A VRPower® Integrated Power Stage	55 A VRPower® Integrated Power Stage
Input voltage min. (V)	2.5	2.5
Input voltage max. (V)	16	16
Current rating (A)	55	55
Switch frequency max. (kHz)	2000	2000
Enable (yes / no)	Yes	Yes
Monitoring features	T_{MON}/FAULT Monitor	T_{MON}/FAULT Monitor
Protection	OCP, OTP, UVLO	OCP, OTP, UVLO
Light load mode	Yes	Yes
Peak efficiency (%)	92.2	92.2
Pulse-width modulation (V)	5	3.3
Package type	PowerPAK® MLP55-31L	PowerPAK® MLP55-31L
Package size (W, L, H) (mm)	5 x 5 x 0.75	5 x 5 x 0.75
Status code	1	1
Product type	VRPower (DrMOS)	VRPower (DrMOS)
Applications	Computers	Computers

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