50 A VRPower® Integrated Power Stage

DESCRIPTION

The SiC658A is an integrated power stage solution optimized for synchronous buck applications to offer high current, high efficiency, and high power density performance. Packaged in Vishay's 5 mm x 5 mm MLP package, SiC658A enables voltage regulator designs to deliver up to 50 A continuous current per phase.

The internal power MOSFETs utilizes Vishay's state-of-the-art TrenchFET technology that delivers industry benchmark performance to significantly reduce switching and conduction losses.

The SiC658A incorporates an advanced MOSFET gate driver IC that features high current driving capability, adaptive dead-time control, an integrated bootstrap switch, a temperature sensor to measure the junction temperature and protects against damage, and zero current detection to improve light load efficiency. The drivers are also compatible with a wide range of PWM controllers and supports tri-state PWM, 3.3 V logic.

FEATURES

RoHS
COMPLIANT
HALOGEN
FREE

- Thermally enhanced PowerPAK® MLP55-31L package
- Vishay's latest TrenchFET technology and low-side MOSFET with integrated Schottky diode
- Delivers in excess of 50 A continuous current, 80 A peak (10 ms) and 100 A peak (10 μs)
- High frequency operation up to 1.5 MHz
- Power MOSFETs optimized for 12 V input stage
- 3.3 V PWM logic with tri-state and support
- Zero current detect control for light load efficiency improvement
- Low PWM propagation delay
- Thermal monitor and fault flag
- Under voltage lockout protection
- Over-current protection
- High-side FET short protection
- Over-temperature protection
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Multi-phase VRDs for CPU, GPU, and memory

TYPICAL APPLICATION DIAGRAM

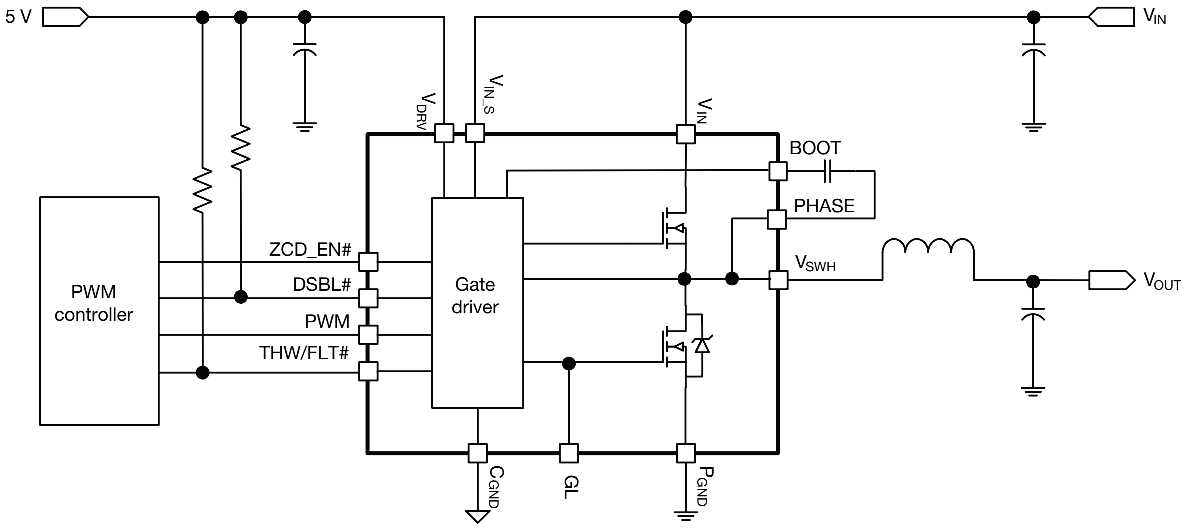
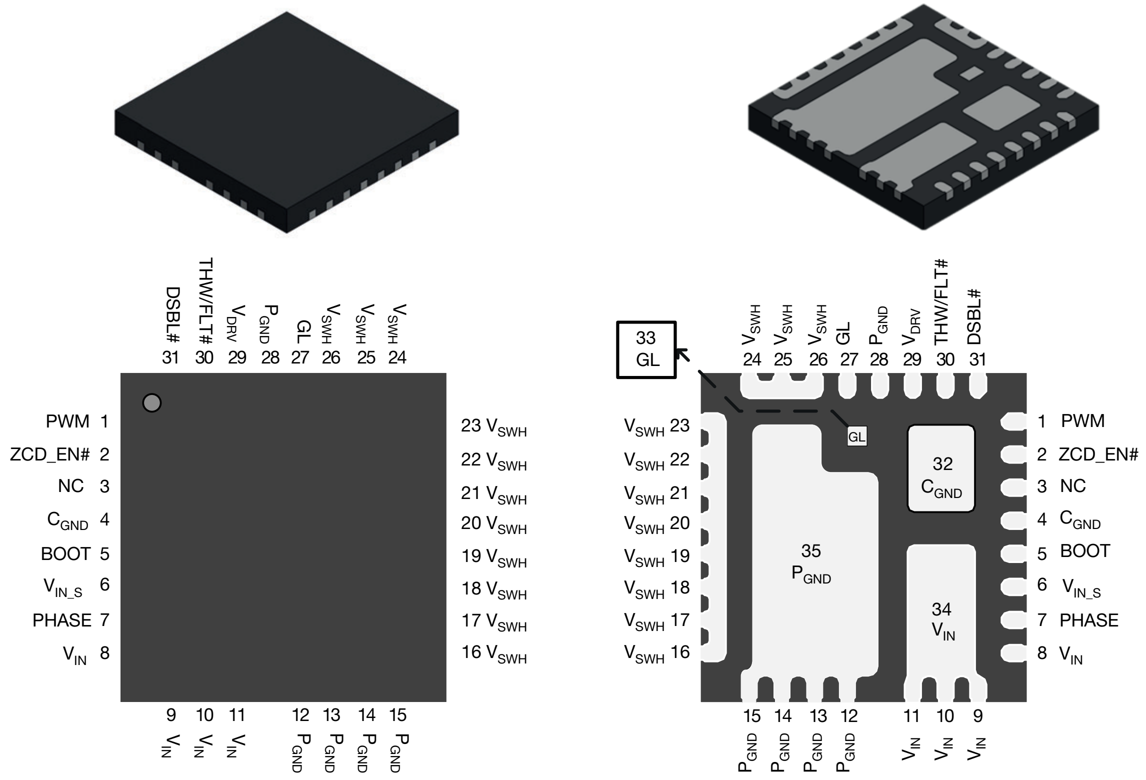


Fig. 1 - SiC658A Typical Application Diagram

PINOUT CONFIGURATION



Top view

Bottom view

Fig. 2 - SiC658A Pin Configuration

PIN CONFIGURATION

PIN NUMBER	NAME	FUNCTION
1	PWM	PWM control input
2	ZCD_EN#	The ZCD_EN# pin enables or disables diode emulation. When ZCD_EN# is low, diode emulation is allowed. When ZCD_EN# is high or floating, continuous conduction mode is forced
3,	NC	Not internally connected
4, 32	C_{GND}	Analog ground for the driver IC
5	BOOT	High-side driver bootstrap voltage
6	V_{IN_S}	This pin is internally connected to V_{IN} pad for HS FET OCP. Please leave it floating or connect a 1 µF filter capacitor to GND
7	PHASE	Return path of high-side gate driver
8 to 11, 34	V_{IN}	Power stage input voltage. Drain of high-side MOSFET
12 to 15, 28, 35	P_{GND}	Power ground
16 to 26	V_{SWH}	Switch node of the power stage
27, 33	GL	Low-side gate signal
29	V_{DRV}	Supply voltage for internal gate driver
30	THW/FLT#	Open-drain, active-low pin to indicate that either an over-temperature or high-side FET short event has occurred. Connect this pin to V_{DRV} with a maximum 20 kΩ pull-up resistor
31	DSBL#	Active low signal to disable the part. There is an internal pull-down resistor to keep the part disabled if an external signal is not present.

ORDERING INFORMATION

PART NUMBER	PACKAGE	MARKING CODE	OPTION
SiC658ACD-T1-GE3	PowerPAK MLP55-31L	SiC658A	3.3 V PWM optimized

ABSOLUTE MAXIMUM RATINGS

ELECTRICAL PARAMETER	SYMBOL	LIMIT	UNIT
Input voltage	V_{IN}	-0.3 to +30	V
Drive supply voltage	V_{DRV}	-0.3 to +7	
Switching / phase node (DC)	V_{SW} / V_{PH}	-0.3 to +30	
Switching / phase node (AC) [(1)]		-14 to +35	
Input to phase (DC)	$V_{IN-PHASE}$	-0.3 to +30	
Input to phase (AC) [(1)]		-14 to +35	
BOOT voltage (DC)	V_{BOOT}	-0.3 to +37	
BOOT voltage (AC) [(2)]		-7 to +40	
BOOT to switching / phase (DC)	$V_{BOOT-PHASE}$	-0.3 to +7	
BOOT to switching / phase (AC) [(2)]		-0.3 to +9	
All logic inputs and outputs (PWM, DSBL#, and THW/FLT#)		-0.3 to V_{DRV} +0.3	
Max. operating junction temperature	T_J	150	°C
Ambient temperature	T_A	-40 to +125	
Storage temperature	T_{stg}	-65 to +150	
Electrostatic discharge protection	Human body model, JESD22-A114	3000	V
	Charged device model, JESD22-C101	1000	

Notes

- Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

[(1)] The specification values indicated “AC” is V_{SW} / V_{PH} to P_{GND}, or V_{IN} to V_{PHASE} , at -14 V (< 10 ns, 10 μJ), min. and 35 V (< 50 ns), max.

[(2)] The specification value indicates “AC voltage” is V_{BOOT} to P_{GND}, -7 V (< 20ns) min and 40V (< 50ns) max., or V_{BOOT} to $V_{SW/PHASE}$, -0.3 V min. and 9 V (< 20ns) max.

RECOMMENDED OPERATING RANGE

ELECTRICAL PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNIT
Input voltage (V_{IN})	4.5	-	24	V
Drive supply voltage (V_{DRV})	4.5	5	5.5	
BOOT to PHASE ($V_{BOOT-PHASE}$, DC voltage)	4	4.5	5.5	
Thermal resistance from junction to ambient	-	10.6	-	°C/W
Thermal resistance from junction to case bottom	-	1.6	-	
Thermal resistance from junction to case top (no heat sink on top)	-	12.6	-	

ELECTRICAL SPECIFICATIONS
(DSBL# = ZCD_EN# = 5 V, V_{IN} = 12 V, V_{DRV} = 5 V, T_A = 25 °C)

PARAMETER	SYMBOL	TEST CONDITION	LIMITS			UNIT
			MIN.	TYP.	MAX.	
POWER SUPPLY						
Drive supply current	I_{VDRV}	f_S = 300 kHz, D = 0.1	-	11	25	mA
		f_S = 1 MHz, D = 0.1	-	38	-	
		$V_{DSBL\#}$ = 0 V, no switching	-	5	-	μA
		$V_{DSBL\#}$ = 5 V, no switching	-	300	-	
V_{DRV} UVLO rising	V_{DRV_R}	-	4.1	-	-	V
V_{DRV} UVLO falling	V_{DRV_F}	-	-	-	3.3	V
V_{DRV} UVLO hysteresis	V_{DRV_HYS}	-	-	275	-	mV
BOOTSTRAP SUPPLY						
Bootstrap switch on resistance	$R_{DS(ON)\_BOOT}$		-	3.4	-	Ω
PWM CONTROL INPUT						
Rising threshold	$V_{TH\_PWM\_R}$		2.7	-	-	V
Falling threshold	$V_{TH\_PWM\_F}$		-	-	0.65	
Tri-state voltage	V_{TRI}	V_{PWM} = FLOAT	-	1.88	-	
Tri-state rising threshold	$V_{TRI\_TH\_R}$		1.38	-	-	
Tri-state falling threshold	$V_{TRI\_TH\_F}$		-	-	1.95	
PWM input current	I_{PWM}	V_{PWM} = 3.3 V	-	-	225	μA
		V_{PWM} = 0 V	-225	-	-	
TIMING SPECIFICATIONS						
Tri-state to GH/GL rising propagation delay	$t_{PD\_TRI\_R}$	No load, see fig. 4	-	35	-	ns
Tri-state hold-off time	t_{TSHO}		-	30	-	
GH - turn off propagation delay	$t_{PD\_OFF\_GH}$		-	25	-	
GH - turn on propagation delay (dead time rising)	$t_{PD\_ON\_GH}$	Load = 50 A	-	15	-	
GL - turn off propagation delay	$t_{PD\_OFF\_GL}$	No load, see fig. 4	-	30	-	
GL - turn on propagation delay (dead time falling)	$t_{PD\_ON\_GL}$	Load = 50 A	-	10	-	
DSBL# Lo to GH/GL falling propagation delay	$t_{PD\_DSBL\#\_F}$	Fig. 5	-	55	-	
PWM minimum on-time	$t_{PWM\_ON\_MIN}$		-	20	-	
PROTECTIONS						
Over current protection	I_{OCP}		90	110	-	A
Over temperature protection	T_{SHDN}		-	160	-	°C
THW/FLT# output low	$V_{OL\_THW/FAULT\#}$	$I_{THW/FAULT\#}$ = 2 mA	-	0.02	-	V

ELECTRICAL SPECIFICATIONS (DSBL# = ZCD_EN# = 5 V, V_{IN} = 12 V, V_{DRV} = 5 V, T_A = 25 °C)						
PARAMETER	**SYMBOL**	**TEST CONDITION**	**LIMITS**			**UNIT**
			MIN.	**TYP.**	**MAX.**	
DSBL# INPUT						
DSBL# logic input voltage	$V_{IH\_DSBL\#}$	Input logic high	2	-	-	V
	$V_{IL\_DSBL\#}$	Input logic low	-	-	0.8	
ZCD_EN# CONTROL INPUT						
Rising threshold	$V_{TH\_ZCD\_EN\#\_R}$		2.8	-	-	V
Falling threshold	$V_{TH\_ZCD\_EN\#\_F}$		-	-	0.7	
Tri-state rising threshold	$V_{TRI\_ZCD\_EN\#\_R}$		1.5	-	-	
Tri-state falling threshold	$V_{TRI\_ZCD\_EN\#\_F}$		-	-	1.9	
ZCD_EN# input current	$I_{ZCD\_EN\#}$	$V_{ZCD\_EN\#}$ = 5 V	-	-	100	μA
		$V_{ZCD\_EN\#}$ = 0 V	-300	-	-	

Notes

[1] Typical limits are established by characterization and are not production tested

[2] Guaranteed by design

DETAILED OPERATIONAL DESCRIPTION

PWM Input with Tri-State Function

The PWM input receives the PWM control signal from the VR controller IC. The PWM input is designed to be compatible with standard controllers using two state logic (H and L) and advanced controllers that incorporate tri-state logic (H, L and tri-state) on the PWM output. For two state logic, the PWM input operates as follows. When PWM is driven above $V_{TH\_PWM\_R}$, the low-side is turned off and the high-side is turned on. When PWM input is driven below $V_{TH\_PWM\_F}$, the high-side is turned OFF and the low-side is turned ON. For tri-state logic, there is a tri-state region that the controller's PWM can be driven to place the MOSFETs into high impedance. If the PWM input stays in this region for the tri-state hold-off period, t_{TSHO}, both high-side and low-side MOSFETs are turned OFF. This function allows the VR phase to be disabled without negative output voltage swing caused by inductor ringing and saves a Schottky diode clamp. The PWM and tri-state regions are separated by hysteresis to prevent false triggering. The SiC658A incorporates 3.3 V compatible PWM thresholds.

Disable (DSBL#)

In the low state, the DSBL# pin shuts down the driver IC and disables both high-side and low-side MOSFETs. In this state, standby current is minimized. If DSBL# is left unconnected, an internal pull-down resistor will pull the pin to C_{GND} and shut down the IC.

Over Current Protection

SiC658A includes an over-current protection feature. When the high-side FET current exceeds the current limit, the device will terminate the high-side FET conduction immediately and turn on the low-side FET. The next high-side ON pulse will be skipped until the low-side FET current drops below the hysteresis threshold. The device does not latch off in over-current condition and will continue to operate at the over-current limit.

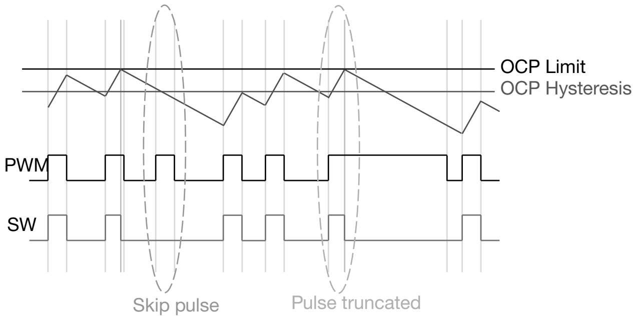


Fig. 3 - OCP Operation

High-Side MOSFET Short Detection

A failure in the high-side FET may cause significant damage to the load. SiC658A detects the high-side FET short event by monitoring the switch node cycle by cycle. If the high-side FET short condition is detected, the device asserts the THW/FLT# pin but continue to respond to PWM commands.

Over-temperature Protection

An internal temperature sensor detects the junction temperature. When the junction temperature exceeds the 160 °C threshold, the device asserts the THW/FLT# pin and shuts down the operation.

Voltage Input (V_{IN} and V_{IN_S})

This is the power input to the drain of the high-side power MOSFET. This pin is connected to the high power intermediate BUS rail. V_{IN_S} is internally connected to V_{IN}, so it can be left floating or have a 1uF capacitor to GND.

Switch Node (V_{SWH} and PHASE)

The switch node, V_{SWH}, is the circuit power stage output. This is the output applied to the power inductor and output filter to deliver the output for the buck converter. The PHASE pin is internally connected to the switch node V_{SWH}. This pin is to be used exclusively as the return pin for the BOOT capacitor. A 20 kΩ resistor is connected between GH and PHASE to provide a discharge path for the HS MOSFET in the event that V_{DRV} goes to zero while V_{IN} is still applied.

Ground Connections (C_{GND} and P_{GND})

P_{GND} (power ground) should be externally connected to C_{GND} (control signal ground). The layout of the printed circuit board should be such that the inductance separating C_{GND} and P_{GND} is minimized. Transient differences due to inductance effects between these two pins should not exceed 0.5 V.

Control and Drive Supply Voltage Input (V_{DRV})

V_{DRV} is the bias supply for the gate drivers and the gate drive control IC. It is recommended to connect a 2.2 μF decoupling capacitor from this pin to GND. This creates a low pass filtering effect to avoid coupling of high frequency gate drive noise into the IC.

Bootstrap Circuit (BOOT)

The internal bootstrap switch and an external bootstrap capacitor form a charge pump that supplies voltage to the BOOT pin. The bootstrap switch is integrated internally so that only an external capacitor is necessary to complete the bootstrap circuit. Connect a boot strap capacitor between the BOOT and PH pins.

Shoot-Through Protection and Adaptive Dead Time

The SiC658A has an internal adaptive logic to avoid shoot through and optimize dead time. The shoot through protection ensures that both high-side and low-side MOSFETs are not turned ON at the same time. The adaptive dead time control operates as follows. The HS and LS gate voltages are specifically monitored to prevent one from rising until the other one falls below 1 V. Timing delays are also built in to ensure that one FET is completely off before the other one is allowed to turn on. The feature allows the dead time to be automatically adjusted and minimized across loads, since gate transitions change with respect to load and temperature.

Under Voltage Lockout (UVLO)

During the start up cycle, the UVLO disables the gate drive and holds the high-side and low-side MOSFET gates low until the supply voltage rail has reached a point at which the logic circuitry can be safely activated. The SiC658A also incorporates logic to clamp the gate drive signals to zero when the UVLO falling edge triggers the shutdown of the device. As an added precaution, a 20 kΩ resistor is connected between GH and PHASE to provide a discharge path for the HS MOSFET.

Diode Emulation Mode and PS4 Mode (ZCD_EN#)

The ZCD_EN# pin enables or disables diode emulation mode. When ZCD_EN# is driven below $V_{TH\_ZCD\_EN\#\_F}$, diode emulation is allowed. When ZCD_EN# is driven above $V_{TH\_ZCD\_EN\#\_R}$, continuous conduction mode is forced. Diode emulation mode allows for higher converter efficiency under light load situations. With diode emulation active, the SiC658A will detect the zero current crossing of the output inductor and turn off the low side MOSFET. This ensures that discontinuous conduction mode (DCM) is achieved. Diode emulation is asynchronous to the PWM signal, therefore, the SiC658A will respond to the ZCD_EN# input immediately after it changes state. The ZCD_EN# pin is internally pulled-up to V_{DRV}, so that if the pin is floating, force continuous conduction mode (FCCM) is automatically enabled.

FUNCTIONAL BLOCK DIAGRAM

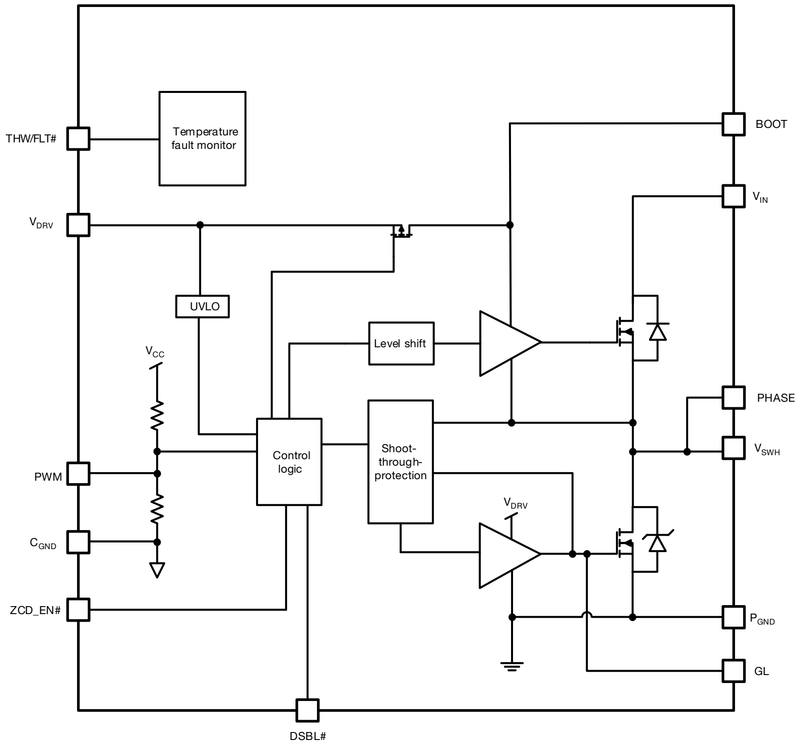


Fig. 4 - SiC658A Functional Block Diagram

DEVICE TRUTH TABLE

DSBL#	ZCD_EN#	PWM	GH	GL
L	X	X	L	L
H	Tri-state	X	L	L
H	L	L	L	H, $I_L > 0$ A L, $I_L < 0$ A
H	L	H	H	L
H	L	Tri-state	L	L
H	H	L	L	H
H	H	H	H	L
H	H	Tri-state	L	L

PWM TIMING DIAGRAM

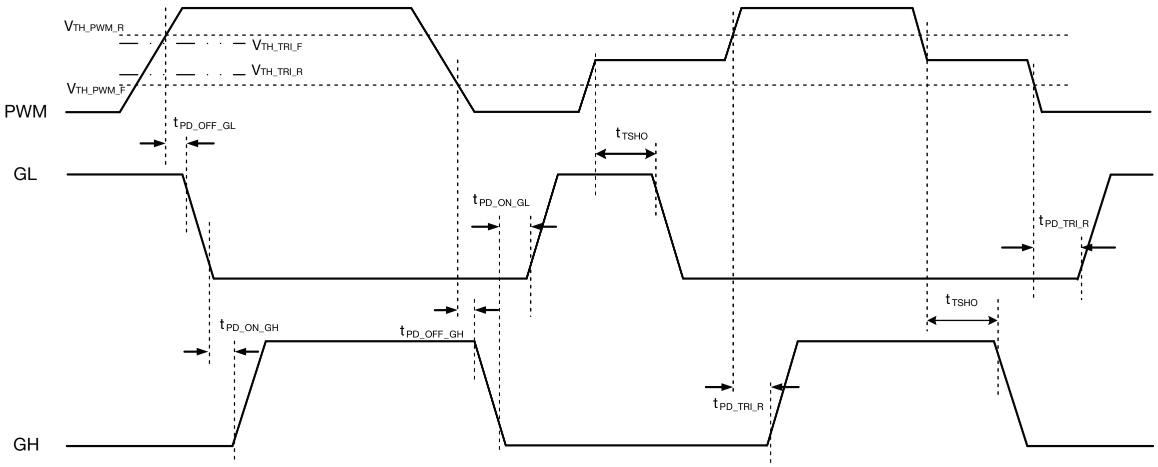
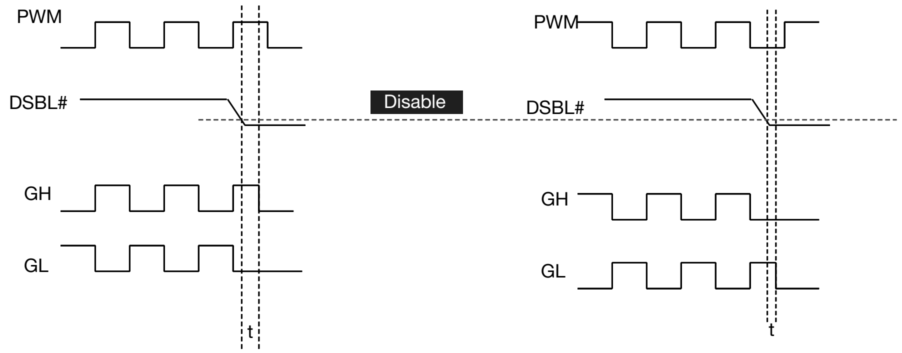


Fig. 5 - Definition of PWM Logic and Tri-state

DSBL# PROPAGATION DELAY



DSBL# Low to GH Falling Propagation Delay

DSBL# Low to GL Falling Propagation Delay

Fig. 6 - DSBL# Falling Propagation Delay

ELECTRICAL CHARACTERISTICS

Test condition: V_{IN} = 12 V, V_{DRV} = 5 V, ZCD_EN# = 5 V, V_{OUT} = 1.0 V, L_{OUT} = 100 nH, F_{SW} = 500 kHz T_A = 25 °C, natural convection cooling (All power loss and normalized power loss curves show SiC658A losses only unless otherwise stated)

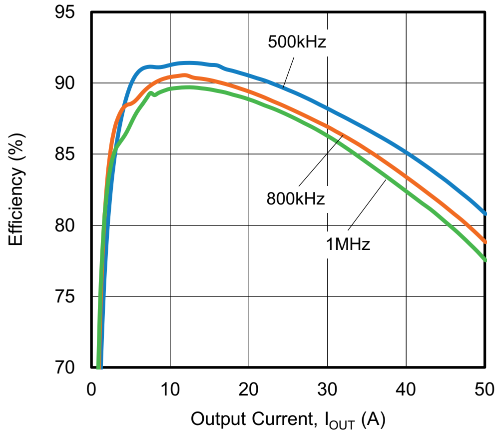


Fig. 7 - Efficiency vs. Output Current

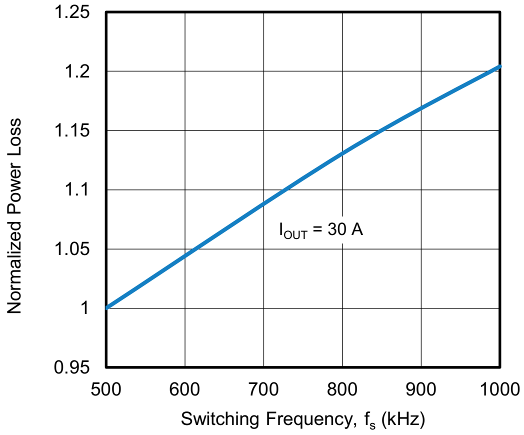


Fig. 10 - Power Loss vs. Switching Frequency

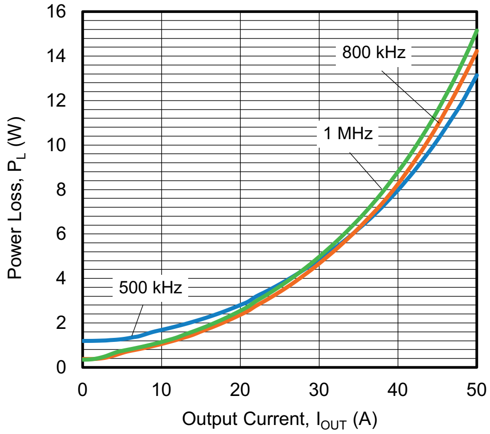


Fig. 8 - Power Loss vs. Output Current

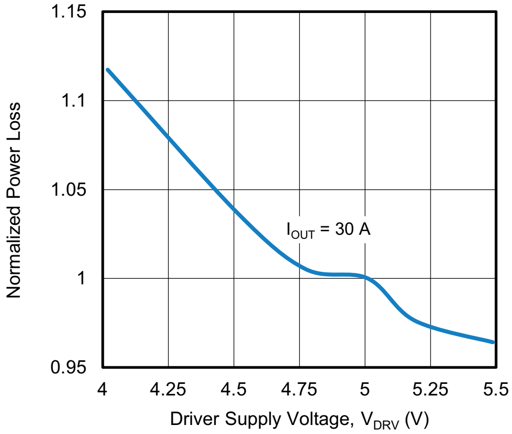


Fig. 11 - Power Loss vs. Drive Supply Voltage

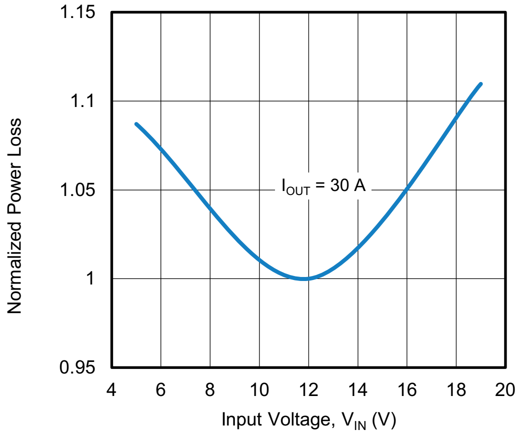


Fig. 9 - Power Loss vs. Input Voltage

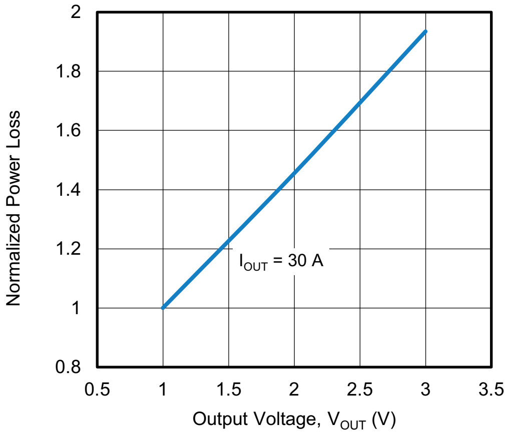


Fig. 12 - Power Loss vs. Output Voltage

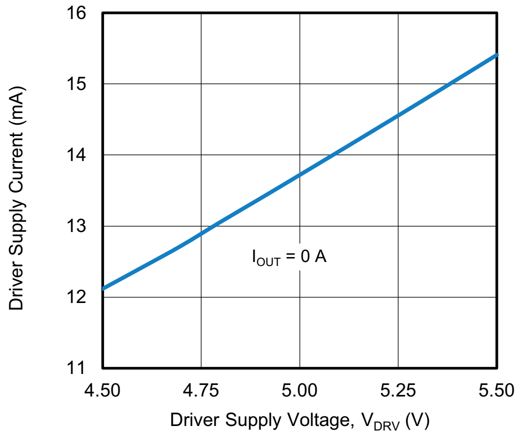


Fig. 13 - Driver Supply Current vs. Driver Supply Voltage

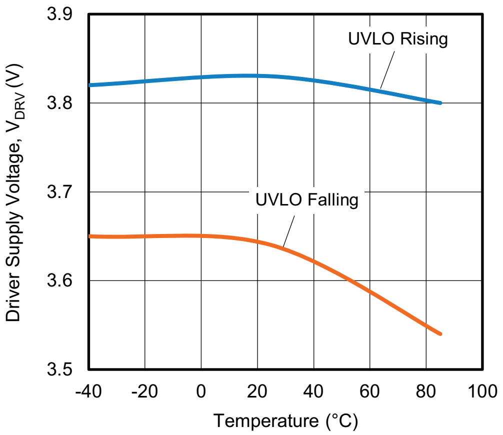


Fig. 16 - Driver Supply UVLO Threshold vs. Temperature

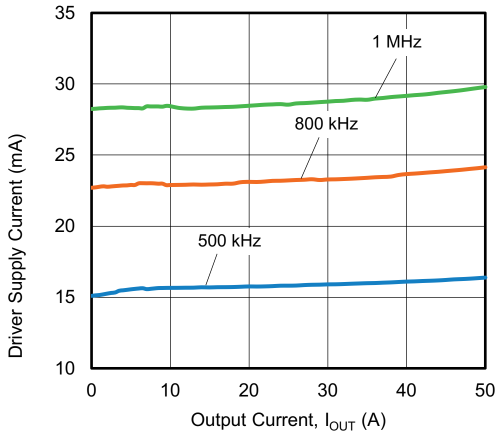


Fig. 14 - Driver Supply Current vs. Output Current

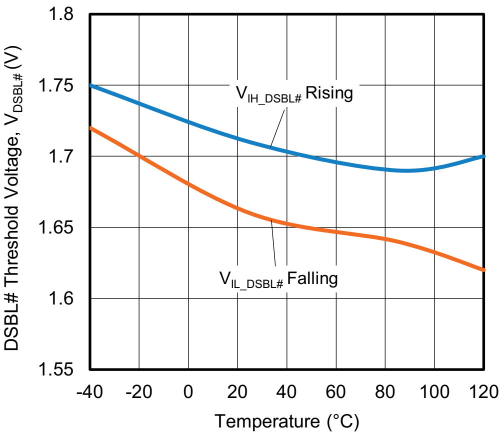


Fig. 17 - DSBL# Threshold vs. Temperature

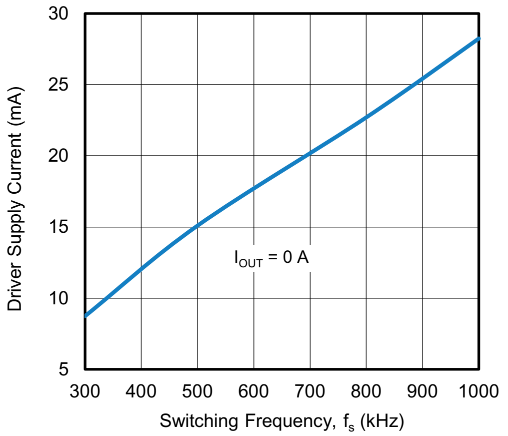


Fig. 15 - Driver Supply Current vs. Switching Frequency

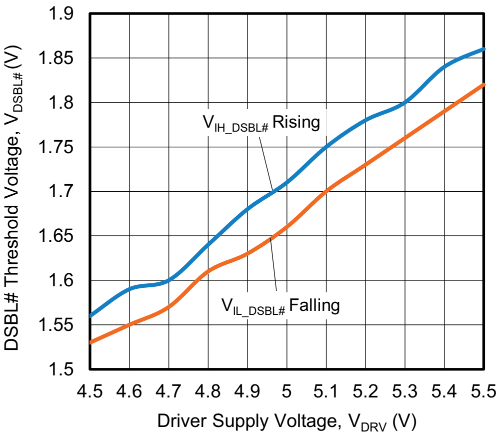


Fig. 18 - DSBL# vs. Driver Input Voltage

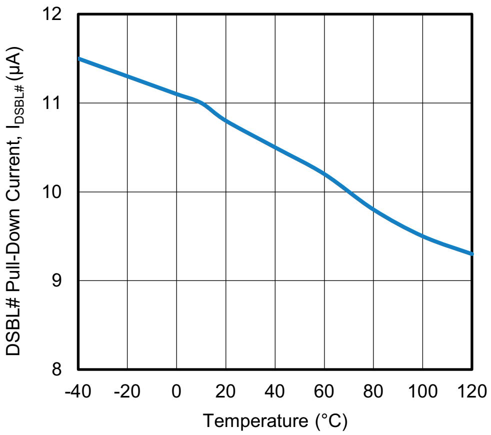
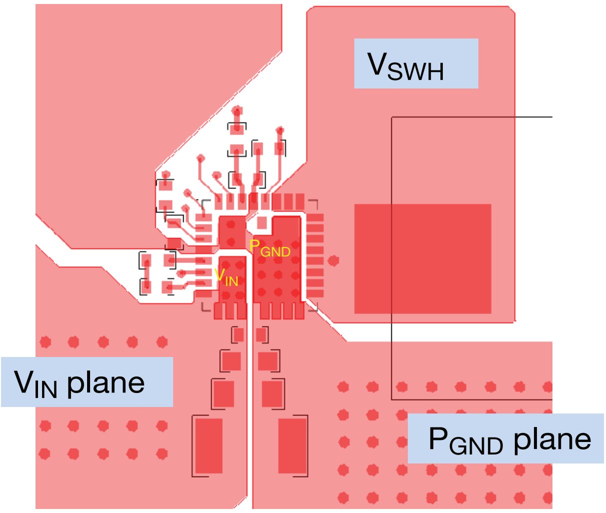


Fig. 19 - DSBL# Pull-Down Current vs. Temperature

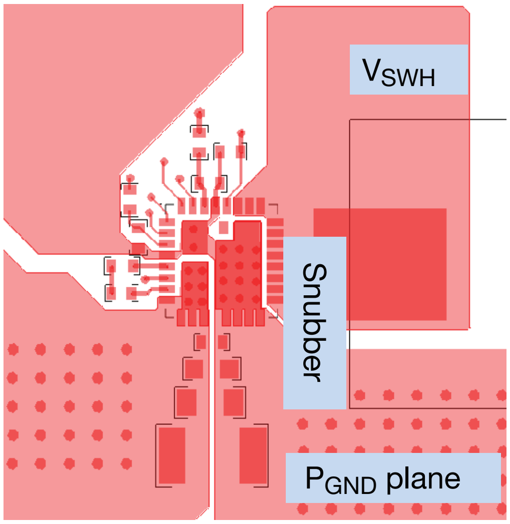
PCB LAYOUT RECOMMENDATIONS

Step 1: V_{IN}/GND Planes and Decoupling



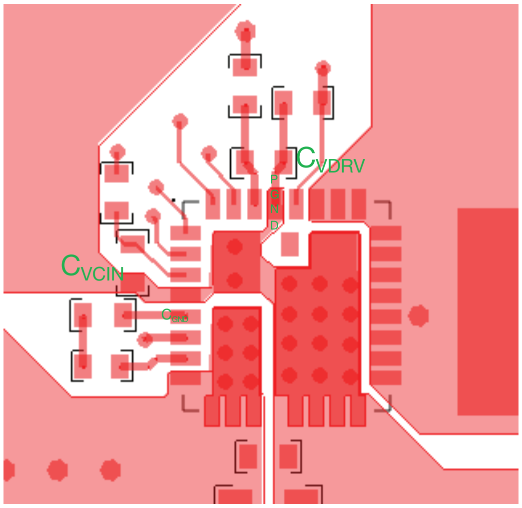
1. Layout V_{IN} and P_{GND} planes as shown above
2. Ceramic capacitors should be placed right between V_{IN} and P_{GND}, and very close to the device for best decoupling effect
3. Difference values / packages of ceramic capacitors should be used to cover entire decoupling spectrum e.g. 1210, 0805, 0603 and 0402
4. Smaller capacitance value, closer to device V_{IN} pin(s) - better high frequency noise absorbing

Step 2: V_{SWH} Plane



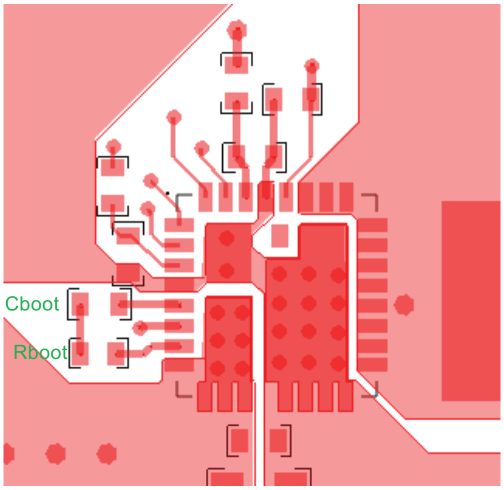
1. Connect output inductor to DrMOS with large plane to lower the resistance
2. If any snubber network is required, place the components as shown above and the network can be placed at bottom

Step 3: V_{DRV} Input Filter



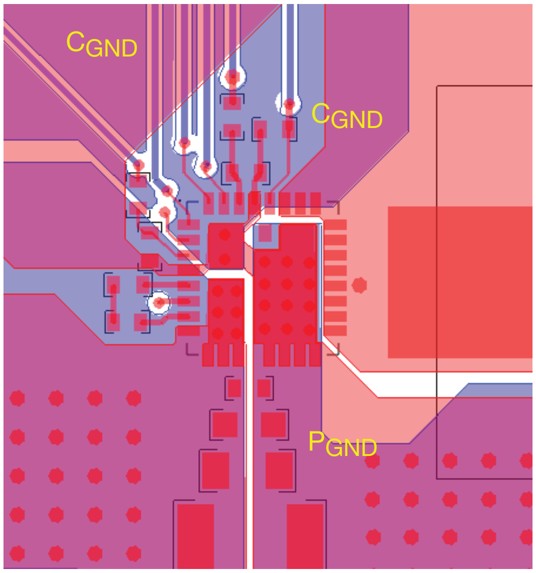
1. The V_{DRV} input filter ceramic cap should be placed very close to IC. It is recommended to connect two caps separately.
2. C_{VDRV} cap should be placed between pin 28 (P_{GND} of driver IC) and pin 29 to provide maximum instantaneous driver current for low-side MOSFET during switching cycle
3. For connecting C_{VDRV} analog ground, it is recommended to use large plane to reduce parasitic inductance.

Step 4: BOOT Resistor and Capacitor Placement



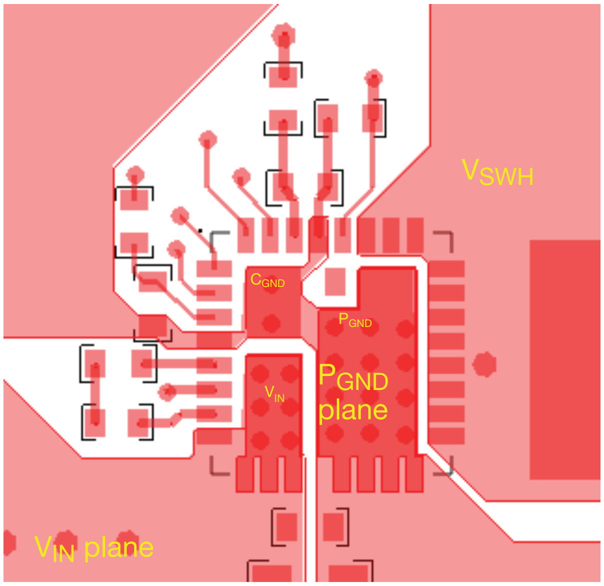
1. These components need to be placed very close to IC, right between PHASE (pin 7) and BOOT (pin 5).
2. To reduce parasitic inductance, chip size 0402 can be used.

Step 5: Signal Routing



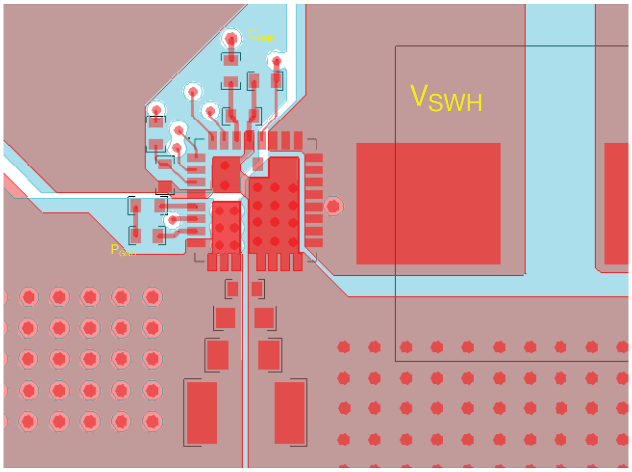
1. Route the PWM / ZCD_EN# / DSBL# / THW/FLT# signal traces out of the top row.
2. PWM signal is very important signal, both signal and return traces should not be routed close to any noisy traces or planes.
3. It is best to “shield” traces form power switching nodes, e.g. V_{SWH}, to improve signal integrity.
4. GL (pin 27) has been connected with GL pad internally and does not need to connect externally.

Step 6: Adding Thermal Relief Vias



1. Thermal relief vias can be added on the V_{IN} and P_{GND} pads to utilize inner layers for high-current and thermal dissipation.
2. To achieve better thermal performance, additional vias can be put on V_{IN} plane and P_{GND} plane.
3. V_{SWH} pad is a noise source and not recommended to put vias on this plane.
4. 8 mil drill for pads and 10 mils drill for plane can be the optional via size. Vias on pad may drain solder during assembly and cause assembly issue. Please consult with the assembly house for guideline.

Step 7: Ground Connection



1. It is recommended to make single connection between C_{GND} and P_{GND} and this connection can be done on top layer.
2. It is recommended to make the whole inner 1 layer (next to top layer) ground plane and separate them into C_{GND} and P_{GND} plane.
3. These ground planes provide shielding between noise source on top layer and signal trace on bottom layer.

Multi-Phases VRPower PCB Layout

Following is an example for 6 phase layout. As can be seen, all the VRPower stages are lined in X-direction compactly with decoupling caps next to them. The inductors are placed as close as possible to the SiC658A to minimize the PCB copper loss. Vias are applied on all PADs (V_{IN}, P_{GND}, C_{GND}) of the SiC658A to ensure that both electrical and thermal performance are excellent. Large copper planes are used for all the high current loops, such as V_{IN}, V_{SWH}, V_{OUT} and P_{GND}. These copper planes are duplicated in other layers to minimize the inductance and resistance. All the control signals are routed from the SiC658A to a controller placed to the north of the power stage through inner layers to avoid the overlap of high current loops. This achieves a compact design with the output from the inductors feeding a load located to the south of the design as shown in the figure.

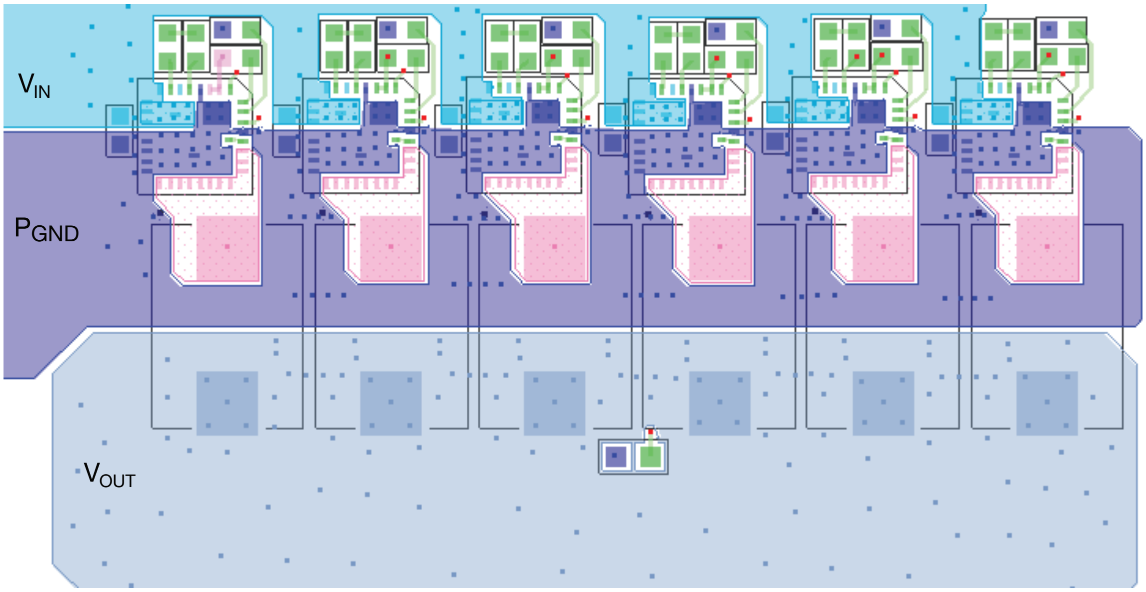


Fig. 20 - Multi - Phase VRPower Layout Top View

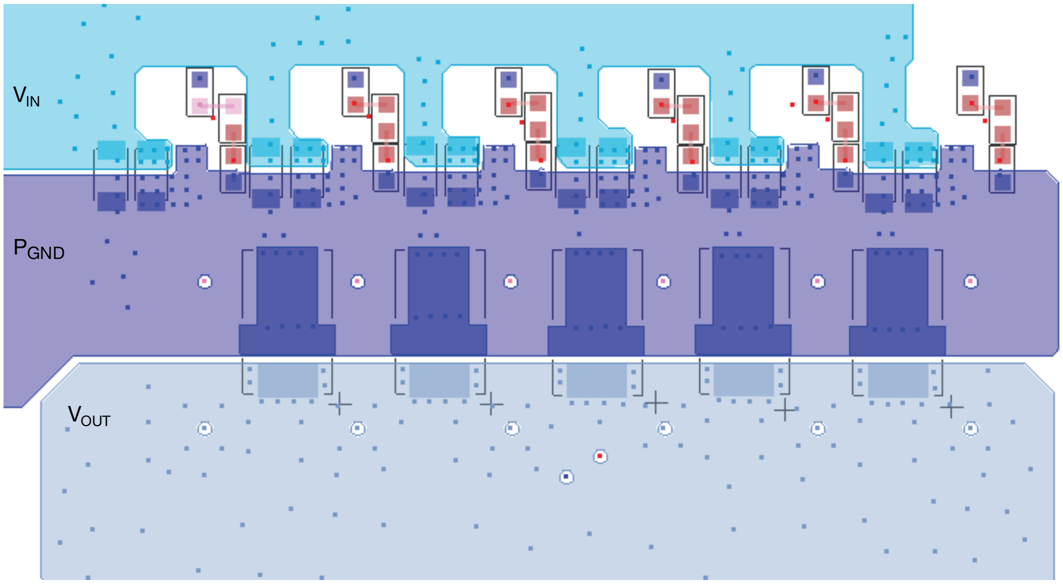
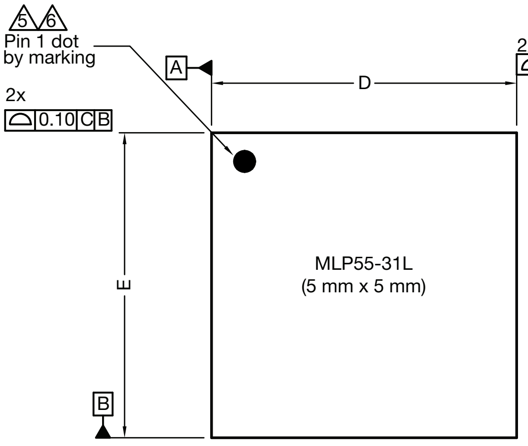


Fig. 21 - Multi - Phase VRPower Layout Bottom View

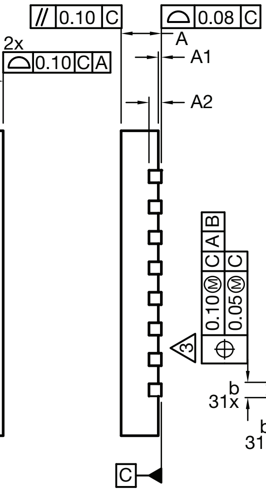
PRODUCT SUMMARY	
Part number	SiC658A
Description	50 A power stage plus, 4.5 V to 24 V_{IN}, 3.3 V PWM
Input voltage min. (V)	4.5
Input voltage max. (V)	24
Current rating (A)	50
Switch frequency max. (kHz)	1500
Enable (yes / no)	Yes
Monitoring features	T_{HDN}
Protection	V_{DRV} UVLO, over-current, over-temperature, high-side short
Light load mode	ZCD
Pulse-width modulation (V)	3.3
Package type	PowerPAK MLP55-31L
Package size (W, L, H) (mm)	5.0 x 5.0 x 0.75
Status code	1
Product type	VRPower (DrMOS)
Applications	Computer, networking

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62113.

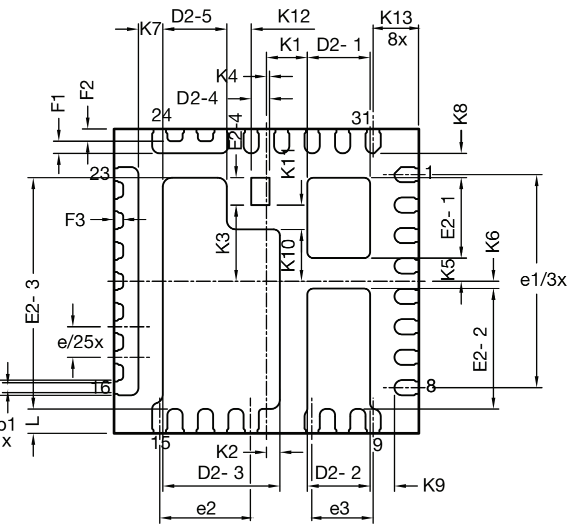
PowerPAK® MLP55-31L Case Outline



Top view



Side view



Bottom view

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.027	0.029	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2	0.20 ref.			0.008 ref.		
b	0.20	0.25	0.30	0.078	0.098	0.011
b1	0.15	0.20	0.25	0.006	0.008	0.010
D	4.90	5.00	5.10	0.193	0.196	0.200
e	0.50 BSC			0.019 BSC		
e1	3.50 BSC			0.138 BSC		
e2	1.50 BSC			0.060 BSC		
e3	1.00 BSC			0.040 BSC		
E	4.90	5.00	5.10	0.193	0.196	0.200
L	0.35	0.40	0.45	0.013	0.015	0.017
D2-1	0.98	1.03	1.08	0.039	0.041	0.043
D2-2	0.98	1.03	1.08	0.039	0.041	0.043
D2-3	1.87	1.92	1.97	0.074	0.076	0.078
D2-4	0.30 BSC			0.012 BSC		
D2-5	1.05	1.10	1.15	0.041	0.043	0.045
E2-1	1.27	1.32	1.37	0.050	0.052	0.054
E2-2	1.93	1.98	2.03	0.076	0.078	0.080
E2-3	3.75	3.80	3.85	0.148	0.150	0.152
E2-4	0.45 BSC			0.018 BSC		
F1	0.15	0.20	0.25	0.006	0.008	0.010
F2	0.20 ref.			0.008 ref.		
F3	0.15 ref.			0.006 ref.		

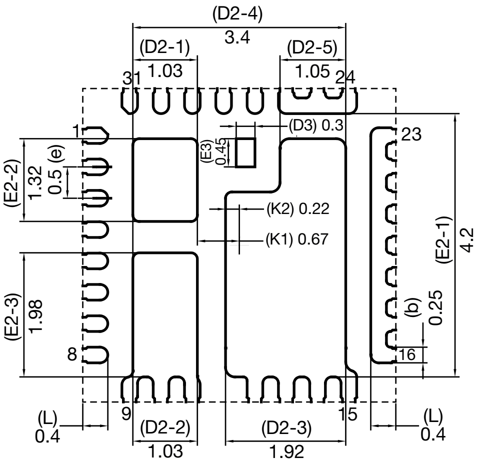
DIM.	MILLIMETERS			INCHES		
	MIN.	**NOM.**	**MAX.**	**MIN.**	**NOM.**	**MAX.**
K1		0.67 BSC			0.026 BSC	
K2		0.22 BSC			0.008 BSC	
K3		1.25 BSC			0.049 BSC	
K4		0.10 BSC			0.004 BSC	
K5		0.38 BSC			0.015 BSC	
K6		0.12 BSC			0.005 BSC	
K7		0.40 BSC			0.016 BSC	
K8		0.40 BSC			0.016 BSC	
K9		0.40 BSC			0.016 BSC	
K10		0.85 BSC			0.033 BSC	
K11		0.40 BSC			0.016 BSC	
K12		0.40 BSC			0.016 BSC	
K13		0.75 BSC			0.030 BSC	
ECN: T17-0423-Rev. F, 21-Aug-17 DWG: 6025						

Notes

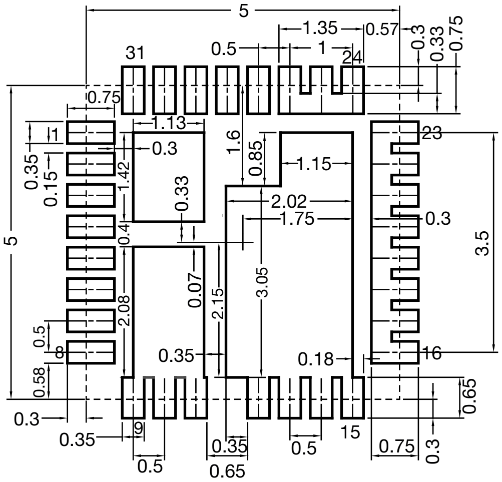
1. Use millimeters as the primary measurement
2. Dimensioning and tolerances conform to ASME Y14.5M. - 1994
3. △ Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip
4. △ The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
5. △ Exact shape and size of this feature is optional
6. Package warpage max. 0.08 mm
7. △ Applied only for terminals

Recommended Land Pattern
PowerPAK® MLP55-31L

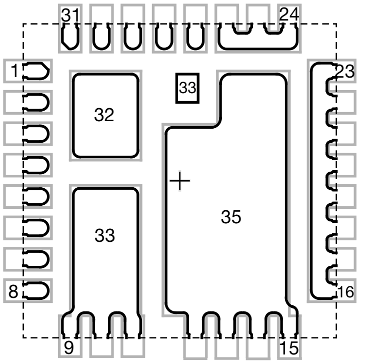
Top side transparent view
(not bottom view)



Land pattern for MLP55-31L



All dimensions in millimeters



☐ Component for MLP55-31L

☐ Land pattern for MLP55-31L

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