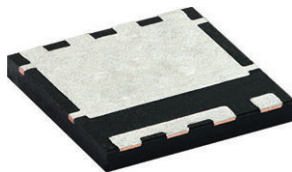


N-Channel 80 V (D-S) 175 °C MOSFET

PowerPAK® 8 x 8 BWL


Top View



Bottom View

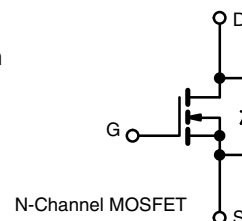
FEATURES

- TrenchFET® Gen IV power MOSFET
- Wettable flanks enhances solderability
- Fully lead (Pb)-free device
- Very low $R_{DS} \times Q_g$ figure of merit (FOM)
- 50 % smaller footprint than D²PAK (TO-263)
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Synchronous rectification
- OR-ing
- Motor drive control
- Battery management



PRODUCT SUMMARY

V_{DS} (V)	80
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.00115
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 7.5$ V	0.00135
Q_g typ. (nC)	140
I_D (A) ^a	608
Configuration	Single

ORDERING INFORMATION

Package	PowerPAK® 8 x 8 BWL
Lead (Pb)-free and halogen-free	SiEH4800EW-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	80	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current ($T_J = 175$ °C)	I_D	$T_C = 25$ °C	381
		$T_C = 70$ °C	319
		$T_A = 25$ °C	34 ^b
		$T_A = 70$ °C	29 ^b
Pulsed drain current ($t = 100$ μ s)	I_{DM}	700	A
Continuous source-drain diode current	I_S	$T_C = 25$ °C	379
		$T_A = 25$ °C	3.1 ^b
Single pulse avalanche current	I_{AS}	87	
Single pulse avalanche energy	E_{AS}	380	mJ
Maximum power dissipation	P_D	$T_C = 25$ °C	417
		$T_C = 70$ °C	292
		$T_A = 25$ °C	3.4 ^b
		$T_A = 70$ °C	2.4 ^b
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^c		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^b	R_{thJA}	33	44	°C/W
Maximum junction-to-case (drain)	R_{thJC}	0.27	0.36	

Notes

- $T_C = 25$ °C
- Surface mounted on 1" x 1" FR4 board
- See solder profile (www.vishay.com/doc?73257). The PowerPAK 8 x 8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

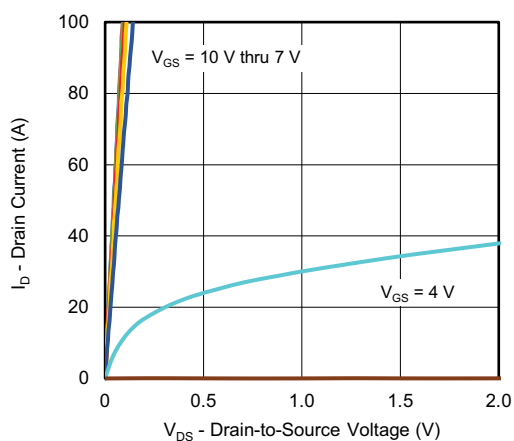
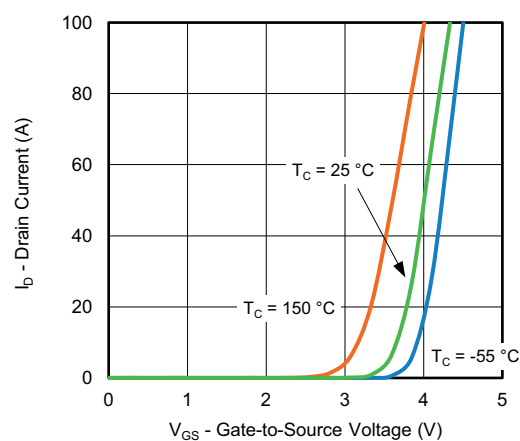
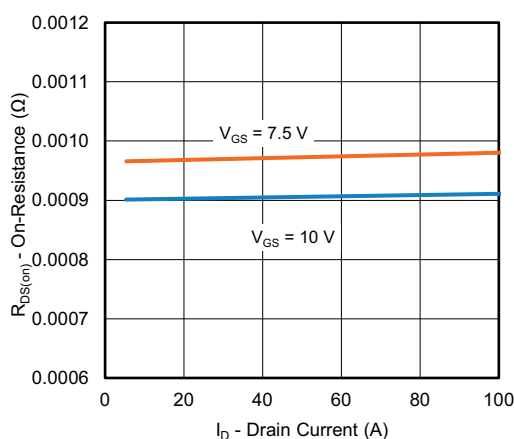
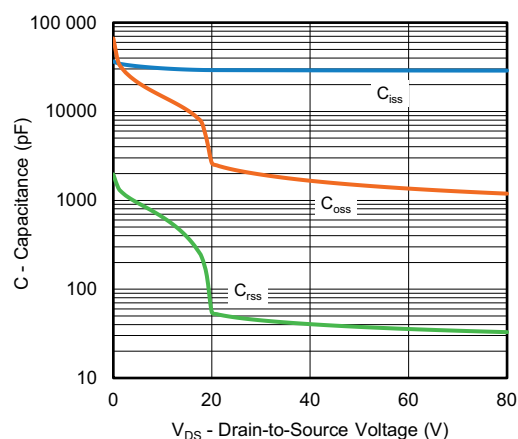
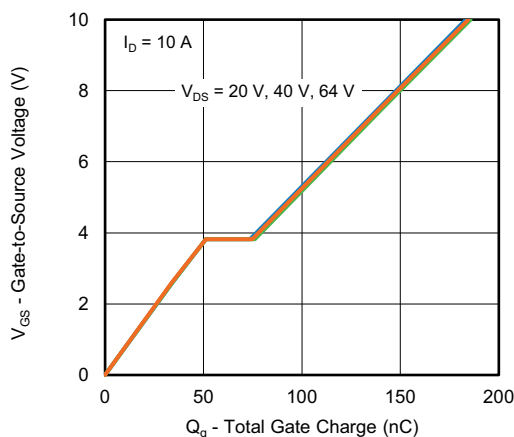
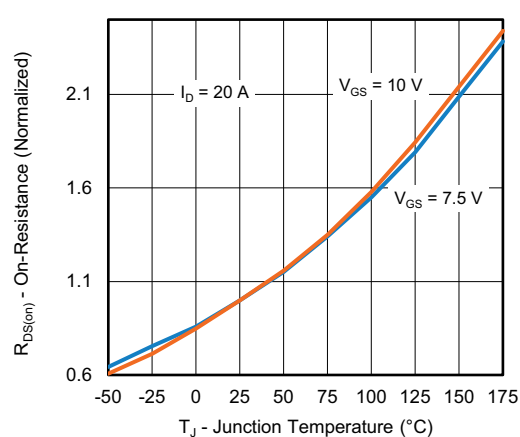


SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	80	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = 10 mA	-	55	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	-	-10	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250 μA	2	-	4	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20	-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 80 V, V _{GS} =0 V	-	-	1	μA
		V _{DS} = 80 V, V _{GS} = 0 V, T _J = 70 °C	-	-	15	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A	-	0.00088	0.00115	Ω
		V _{GS} = 7.5 V, I _D = 20 A	-	0.00091	0.00135	
Forward transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 50 A	-	150	-	S
Dynamic ^b						
Input capacitance	C _{iss}	V _{DS} = 40 V, V _{GS} = 0 V, f = 1 MHz	-	29 000	-	pF
Output capacitance	C _{oss}		-	1650	-	
Reverse transfer capacitance	C _{rss}		-	42	-	
Total gate charge	Q _g	V _{DS} = 40 V, V _{GS} = 10 V, I _D = 10 A	-	185	278	nC
		V _{DS} = 40 V, V _{GS} = 7.5 V, I _D = 10 A	-	140	210	
Gate-source charge	Q _{gs}		-	51	-	
Gate-drain charge	Q _{gd}	-	24	-		
Gate resistance	R _g	f = 1 MHz	0.24	1.2	2.4	Ω
Turn-on delay time	t _{d(on)}	V _{DD} = 40 V, R _L = 4 Ω, I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω	-	23	45	ns
Rise time	t _r		-	17	30	
Turn-off delay time	t _{d(off)}		-	71	140	
Fall time	t _f		-	20	40	
Turn-on delay time	t _{d(on)}	V _{DD} = 40 V, R _L = 4 Ω, I _D ≅ 10 A, V _{GEN} = 7.5 V, R _g = 1 Ω	-	30	60	
Rise time	t _r		-	26	50	
Turn-off delay time	t _{d(off)}		-	64	130	
Fall time	t _f		-	20	40	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	379	A
Pulse diode forward current	I _{SM}		-	-	700	
Body diode voltage	V _{SD}	I _S = 10 A, V _{GS} = 0 V	-	0.68	1.1	V
Body diode reverse recovery time	t _{rr}	I _F = 10 A, dI/dt = 100 A/μs, T _J = 25 °C	-	83	165	ns
Body diode reverse recovery charge	Q _{rr}		-	252	500	nC
Reverse recovery fall time	t _a		-	60	-	ns
Reverse recovery rise time	t _b		-	23	-	

Notes

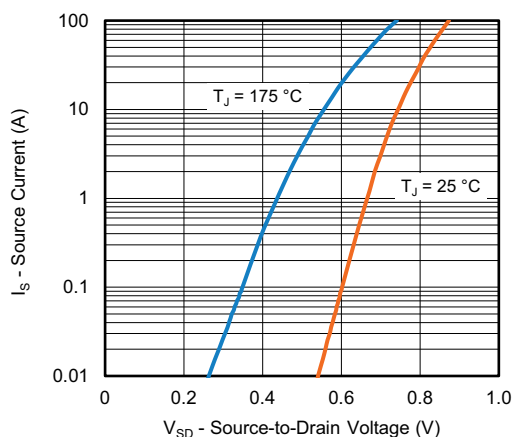
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

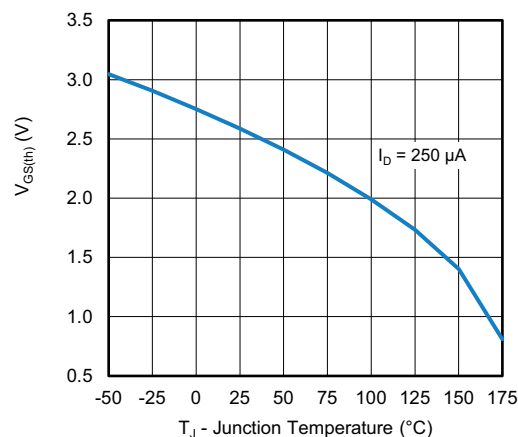
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current and Gate Voltage

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature



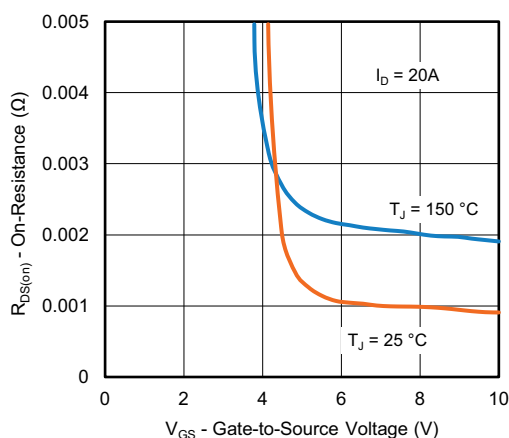
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



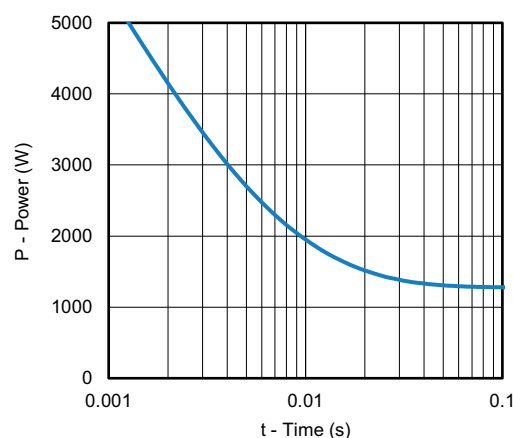
Source-Drain Diode Forward Voltage



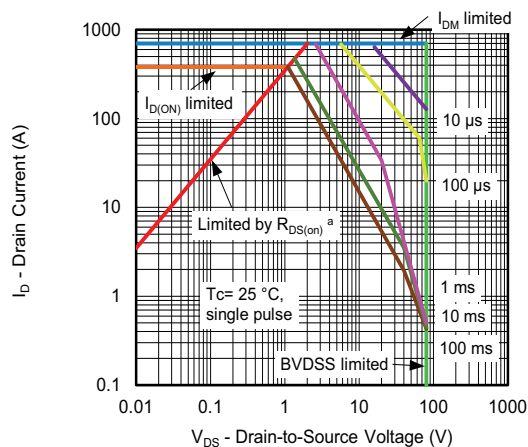
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Case



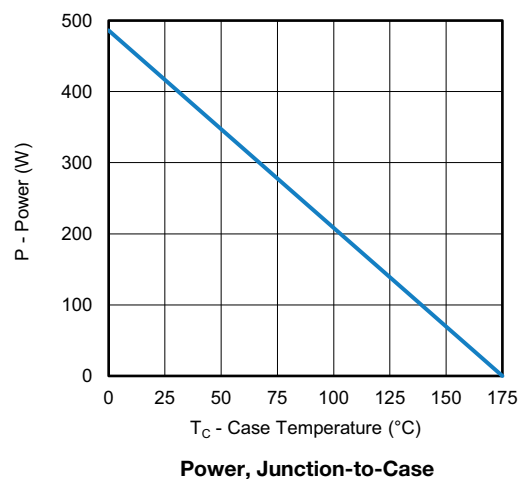
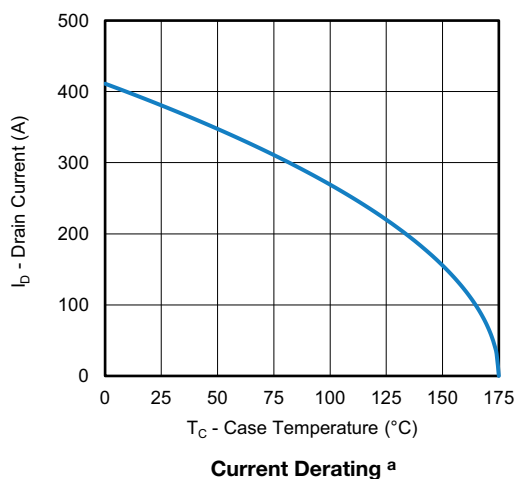
Safe Operating Area, Junction-to-Case

Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

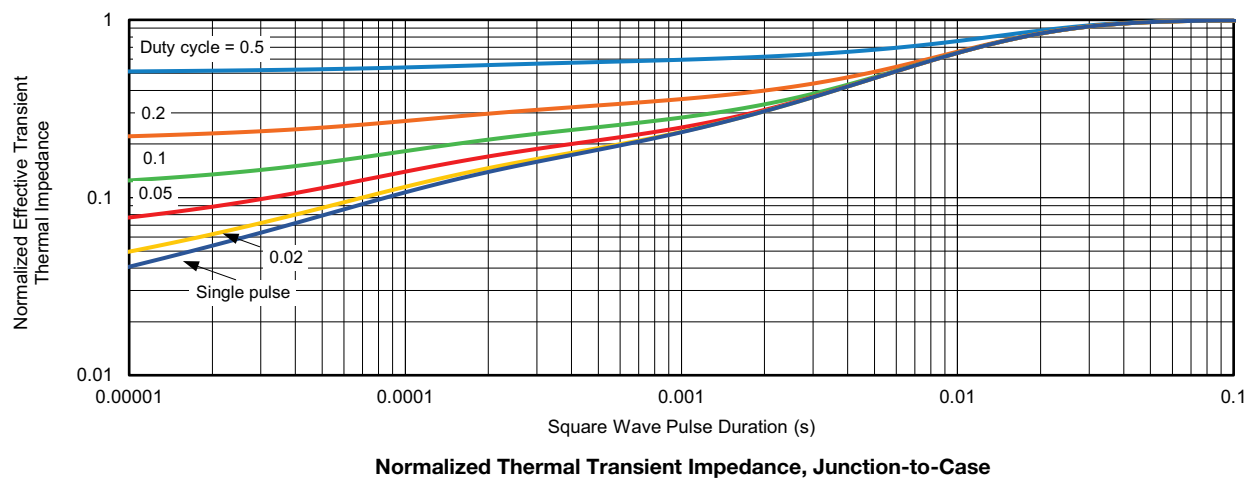


Note

- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

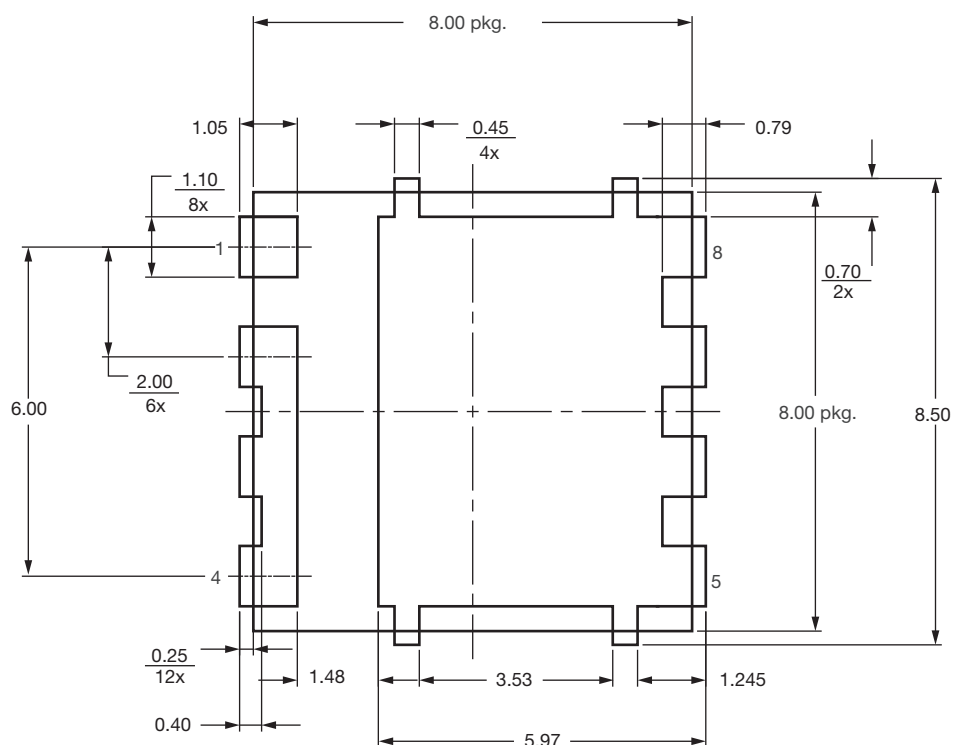
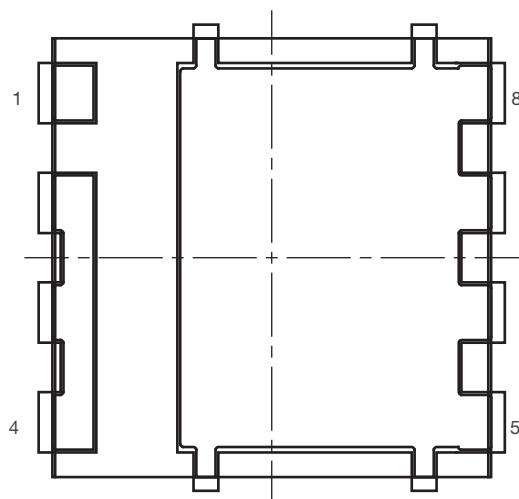


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?61532.

Recommended Land Pattern PowerPAK® 8 x 8 BWL



Note

- Dimensions in mm

ECN: T23-0473-Rev. A, 11-Dec-2023
DWG: 3020



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