



Power MOSFET

PRODUCT SUMMARY	
V _{DS} (V)	650
R _{DS(on)} (Ω)	V _{GS} = 10 V 0.93
Q _g (Max.) (nC)	48
Q _{gs} (nC)	12
Q _{gd} (nC)	19
Configuration	Single

FEATURES

- Low Gate Charge Q_g Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Lead (Pb)-free Available



RoHS* COMPLIANT

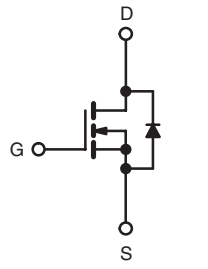
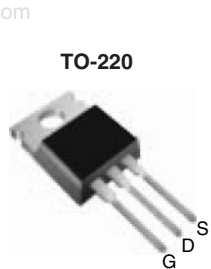
APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching

TYPICAL SMPS TOPOLOGIES

- Single Transistor Flyback
- Single Transistor Forward

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N-Channel MOSFET

ORDERING INFORMATION	
Package	TO-220
Lead (Pb)-free	IRFB9N65APbF
	SiHFB9N65A-E3
SnPb	IRFB9N65A
	SiHFB9N65A


ABSOLUTE MAXIMUM RATINGS T _C = 25 °C, unless otherwise noted				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	V _{DS}	650	V	
Gate-Source Voltage	V _{GS}	± 30		
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	A	
		T _C = 100 °C		5.4
Pulsed Drain Current ^a	I _{DM}	21		
Linear Derating Factor		1.3	W/°C	
Single Pulse Avalanche Energy ^b	E _{AS}	325	mJ	
Repetitive Avalanche Current ^a	I _{AR}	5.2	A	
Repetitive Avalanche Energy ^a	E _{AR}	16	mJ	
Maximum Power Dissipation	T _C = 25 °C	P _D	167	W
Peak Diode Recovery dV/dt ^c	dV/dt	2.8	V/ns	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to + 150	°C	
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d		
Mounting Torque	6-32 or M3 screw	10		lbf · in
		1.1	N · m	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting T_J = 25 °C, L = 24 mH, R_G = 25 Ω, I_{AS} = 5.2 A (see fig. 12).
- I_{SD} ≤ 5.2 A, dI/dt ≤ 90 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.75	

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	650	-	-	V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}^d$	-	670	-	mV/°C	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 30\text{ V}$	-	-	± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$	-	-	25	μA	
		$V_{DS} = 520\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	250		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ $I_D = 5.1\text{ A}^b$	-	-	0.93	Ω	
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}, I_D = 3.1\text{ A}$	3.9	-	-	S	
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5	-	1417	-	pF	
Output Capacitance	C_{oss}		-	177	-		
Reverse Transfer Capacitance	C_{rss}		-	7.0	-		
Output Capacitance	C_{oss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$	-	1912	-	
			$V_{DS} = 520\text{ V}, f = 1.0\text{ MHz}$	-	48	-	
Effective Output Capacitance	$C_{oss\text{ eff.}}$		$V_{DS} = 0\text{ V to } 520\text{ V}^c$	-	84	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 5.2\text{ A}, V_{DS} = 400\text{ V}$ see fig. 6 and 13 ^b	-	-	48	nC
Gate-Source Charge	Q_{gs}			-	-	12	
Gate-Drain Charge	Q_{gd}			-	-	19	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 325\text{ V}, I_D = 5.2\text{ A}$ $R_G = 9.1\text{ }\Omega, R_D = 62\text{ }\Omega$, see fig. 10 ^b	-	14	-	ns	
Rise Time	t_r		-	20	-		
Turn-Off Delay Time	$t_{d(off)}$		-	34	-		
Fall Time	t_f		-	18	-		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	5.2	A	
Pulsed Diode Forward Current ^a	I_{SM}		-	-	21		
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 5.2\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.5	V	
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 5.2\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$	-	493	739	ns	
Body Diode Reverse Recovery Charge	Q_{rr}		-	2.1	3.2	μC	
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80 % V_{DS} .
- Uses SiHFIB5N65A data and test conditions.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

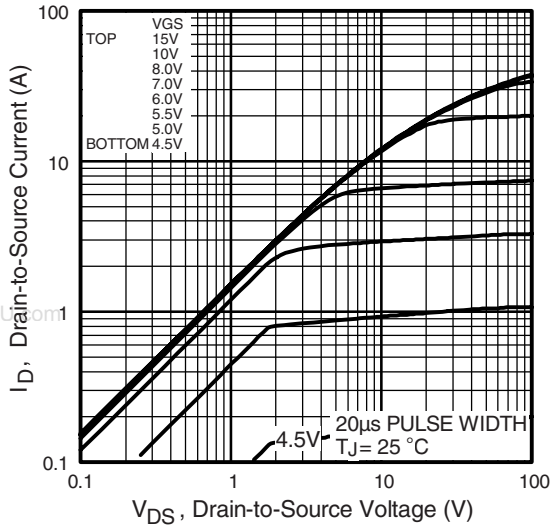


Fig. 1 - Typical Output Characteristics

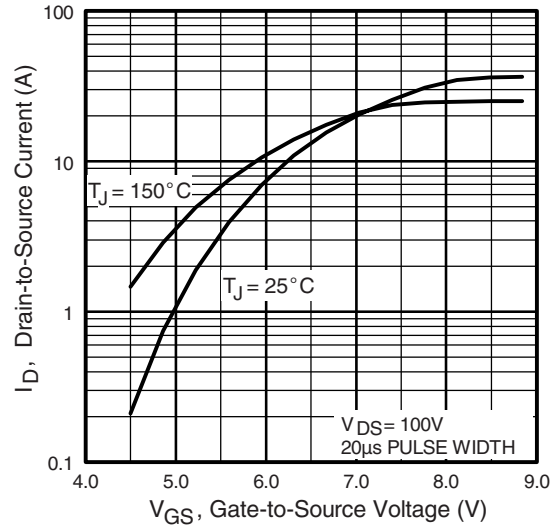


Fig. 3 - Typical Transfer Characteristics

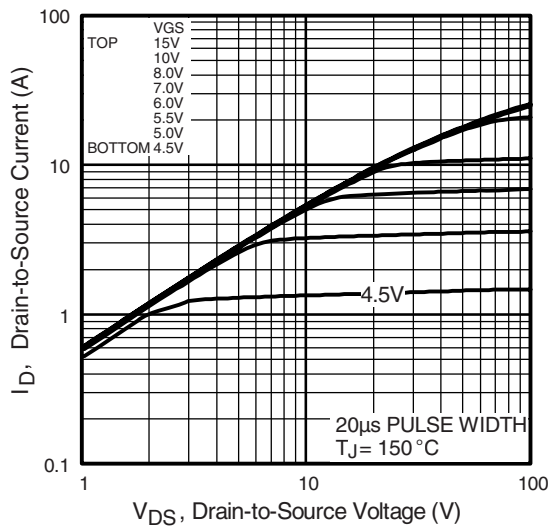


Fig. 2 - Typical Output Characteristics

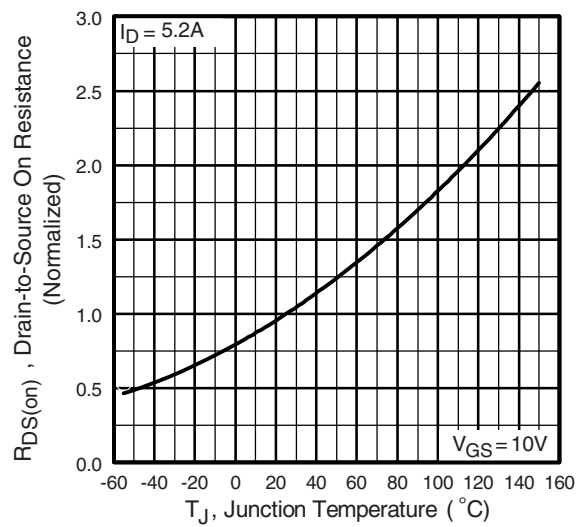


Fig. 4 - Normalized On-Resistance vs. Temperature

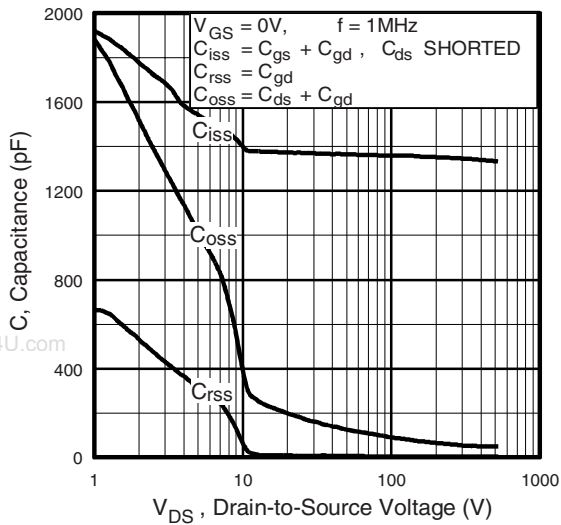


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

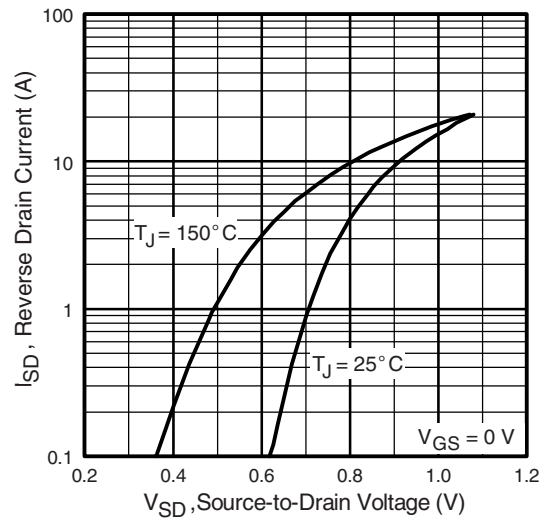


Fig. 7 - Typical Source-Drain Diode Forward Voltage

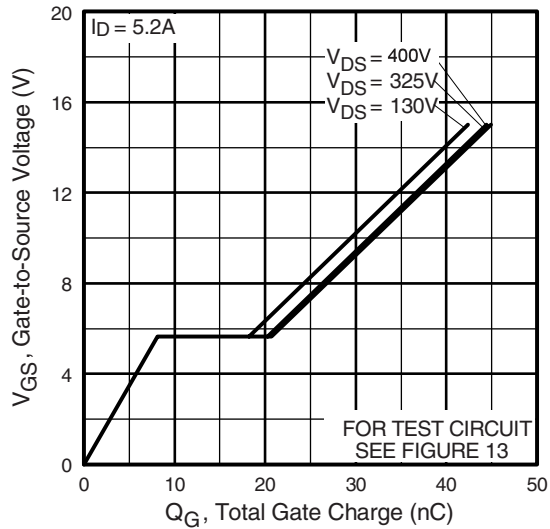


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

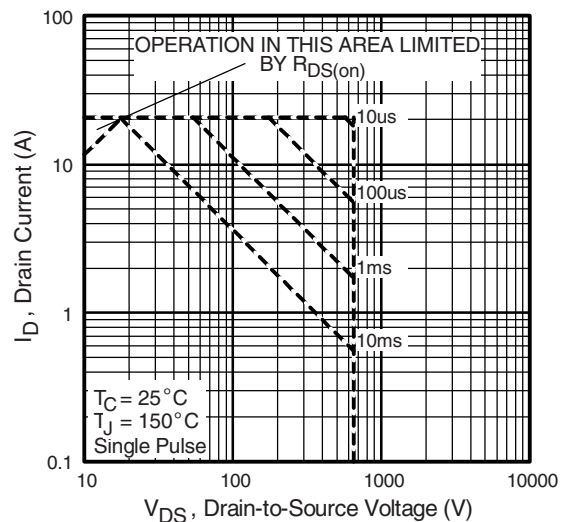


Fig. 8 - Maximum Safe Operating Area

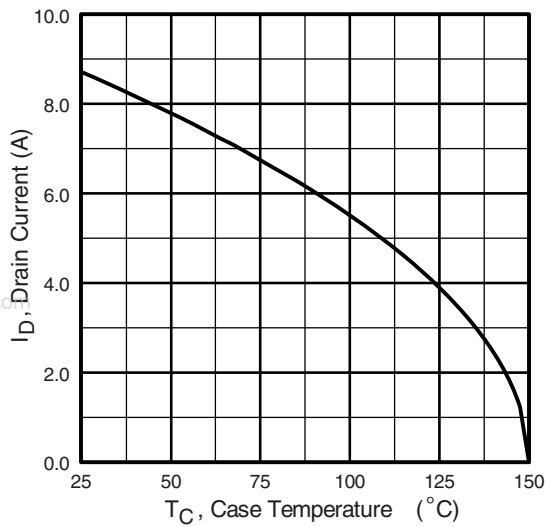


Fig. 9 - Maximum Drain Current vs. Case Temperature

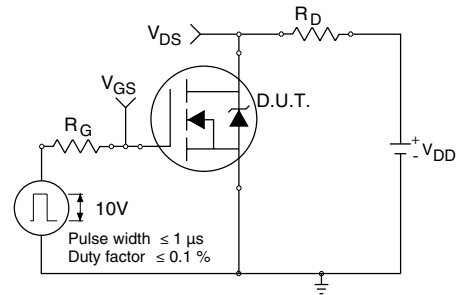


Fig. 10a - Switching Time Test Circuit

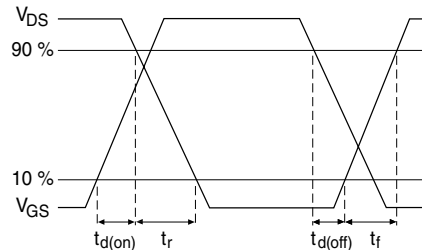


Fig. 10b - Switching Time Waveforms

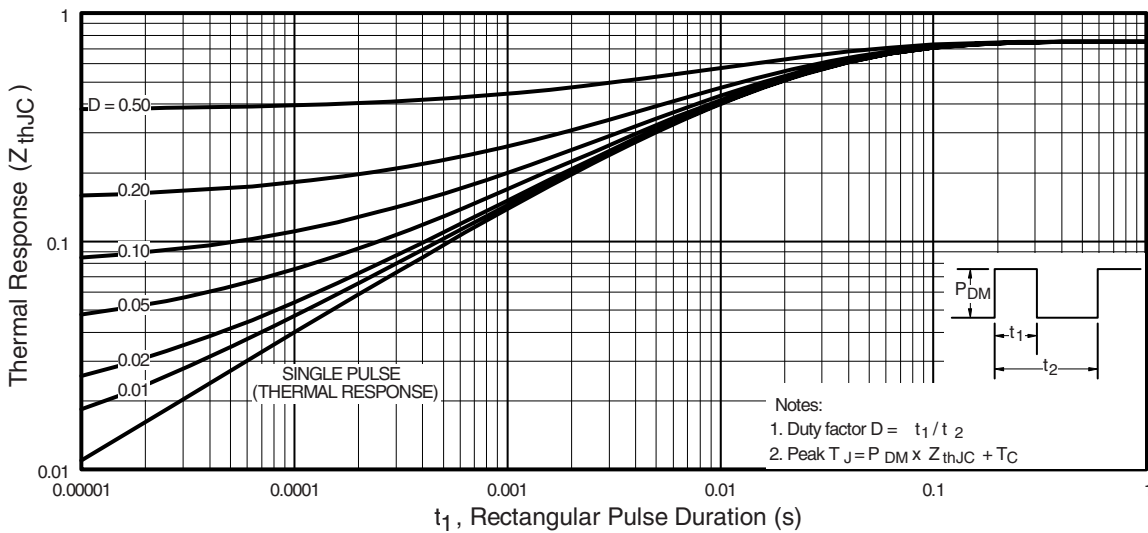


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

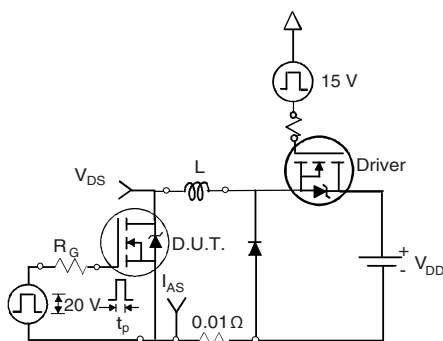


Fig. 12a - Unclamped Inductive Test Circuit

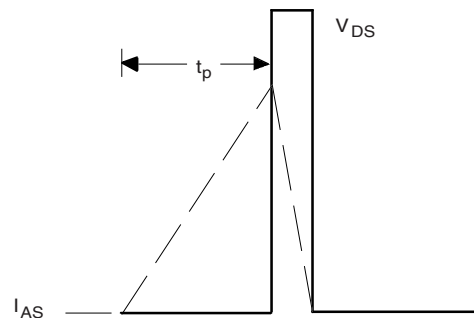


Fig. 12b - Unclamped Inductive Waveforms

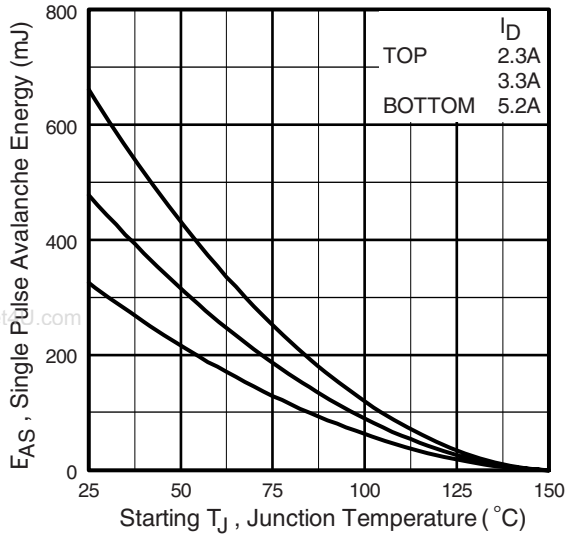


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

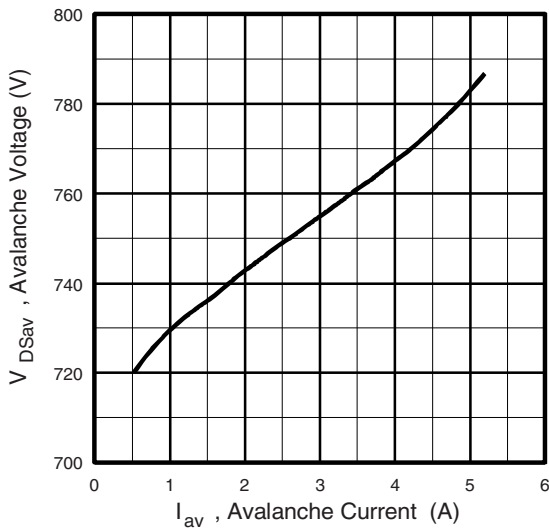


Fig. 12d - Typical Drain-to-Source Voltage vs. Avalanche Current

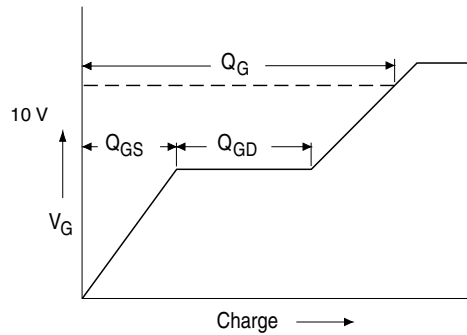


Fig. 13a - Basic Gate Charge Waveform

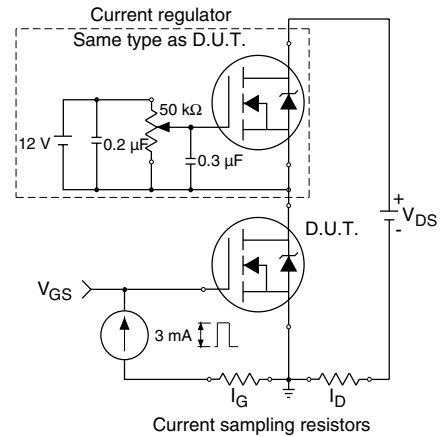
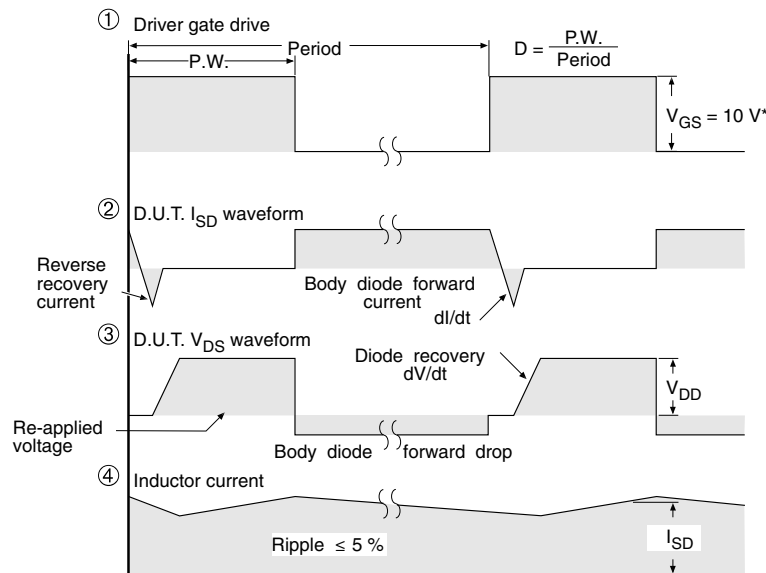
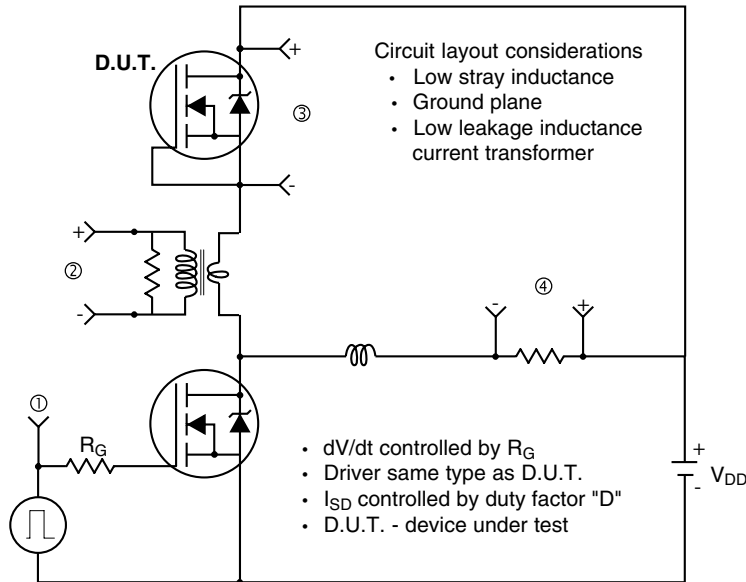


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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