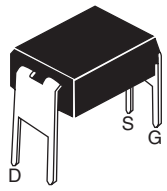
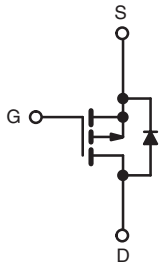
Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	- 200	
$R_{DS(on)}$ (Ω)	V_{GS} = - 10 V	3.0
Q_g (Max.) (nC)	8.9	
Q_{gs} (nC)	2.1	
Q_{gd} (nC)	3.9	
Configuration	Single	

HEXDIP





P-Channel MOSFET

FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- For Automatic Insertion
- End Stackable
- P-Channel
- Fast Switching
- Ease of Paralleling
- Lead (Pb)-free Available

Available
RoHS* COMPLIANT

DESCRIPTION

The Power MOSFETs technology is the key to Vishay advanced line of Power MOSFET transistors. The efficient geometry and unique processing of the Power MOSFETs design archieve very low on-state resistance combined with high transconductance and extreme device ruggedness.
The 4 pin DIP package is a low cost machine-insertable case style which can be stacked in multiple combinations on standard 0.1" pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 W.

ORDERING INFORMATION	
Package	HEXDIP
Lead (Pb)-free	IRFD9210PbF
	SiHFD9210-E3
SnPb	IRFD9210
	SiHFD9210

ABSOLUTE MAXIMUM RATINGS T_C = 25 °C, unless otherwise noted

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	- 200	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current	V_{GS} at - 10 V	T_C = 25 °C	I_D	- 0.40	A
		T_C = 100 °C		- 0.25	
Pulsed Drain Current[a]			I_{DM}	- 3.2	
Linear Derating Factor				0.0083	W/°C
Single Pulse Avalanche Energy[b]			E_{AS}	210	mJ
Repetitive Avalanche Current[a]			I_{AR}	- 0.40	A
Repetitive Avalanche Energy[a]			E_{AR}	0.10	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	1.0	W
Peak Diode Recovery dV/dt[c]			dV/dt	- 5.0	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300[d]	

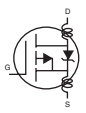
Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. V_{DD} = - 50 V, starting T_J = 25 °C, L = 123 mH, R_G = 25 Ω, I_{AS} = - 1.6 A (see fig. 12).
c. I_{SD} ≤ - 2.3 A, dI/dt ≤ 70 A/µs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C.
d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	-	120	°C/W

SPECIFICATIONS T_J = 25 °C, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA		- 200	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = - 1 mA		-	- 0.23	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA		- 2.0	-	- 4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 200 V, V_{GS} = 0 V		-	-	- 100	µA
		V_{DS} = - 160 V, V_{GS} = 0 V, T_J = 125 °C		-	-	- 500	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = - 10 V	I_D = - 0.24 A[b]	-	-	3.0	Ω
Forward Transconductance	g_{fs}	V_{DS} = - 50 V, I_D = - 0.24 A		0.27	-	-	S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V,		-	170	-	pF
Output Capacitance	C_{oss}	V_{DS} = - 25 V,		-	54	-	
Reverse Transfer Capacitance	C_{rss}	f = 1.0 MHz, see fig. 5		-	16	-	
Total Gate Charge	Q_g	V_{GS} = - 10 V	I_D = - 4.0 A, V_{DS} = - 80 V, see fig. 6 and 13[b]	-	-	8.9	nC
Gate-Source Charge	Q_{gs}			-	-	2.1	
Gate-Drain Charge	Q_{gd}			-	-	3.9	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 100 V, I_D = - 2.3 A, R_G = 24 Ω, R_D = 41 Ω, see fig. 10[b]		-	8.0	-	ns
Rise Time	t_r			-	12	-	
Turn-Off Delay Time	$t_{d(off)}$			-	11	-	
Fall Time	t_f			-	13	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.0	-	nH
Internal Source Inductance	L_S			-	6.0	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	- 0.40	A
Pulsed Diode Forward Current[a]	I_{SM}			-	-	- 3.2	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = - 0.40 A, V_{GS} = 0 V[b]		-	-	- 5.8	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = - 2.3 A, dI/dt = 100 A/µs[b]		-	110	220	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	0.56	1.1	µC

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

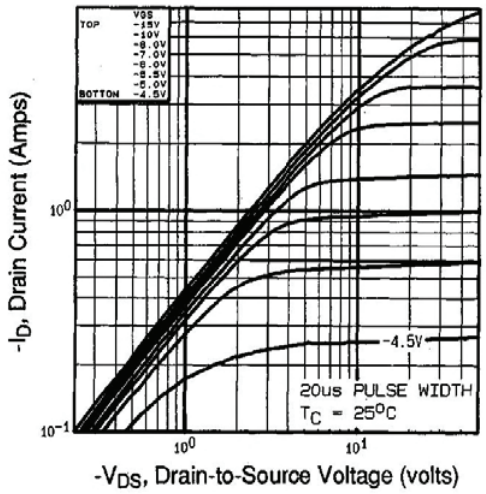


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

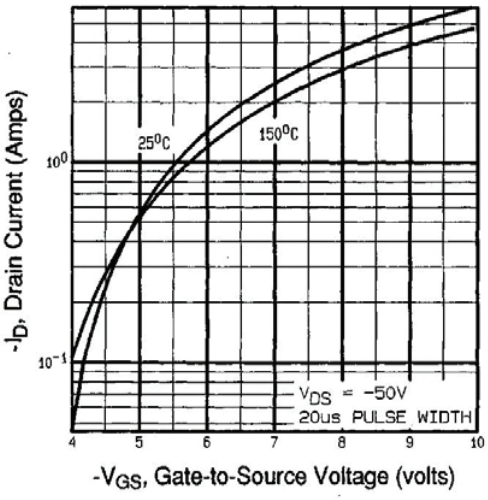


Fig. 3 - Typical Transfer Characteristics

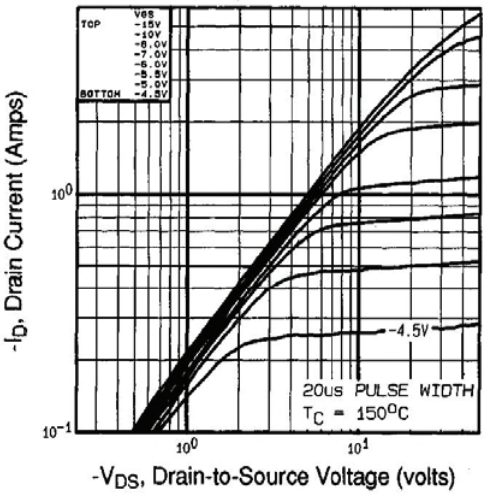


Fig. 2 - Typical Output Characteristics, T_C = 150 °C

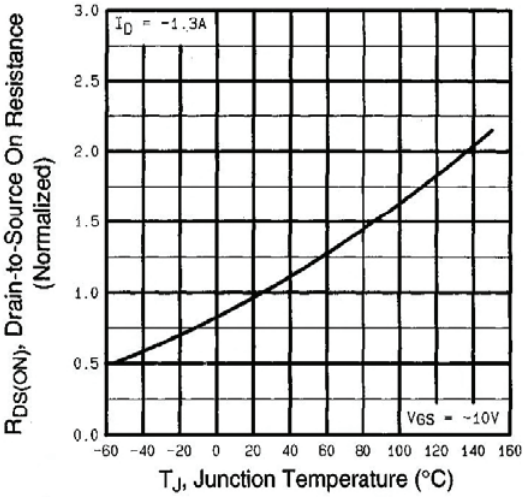


Fig. 4 - Normalized On-Resistance vs. Temperature

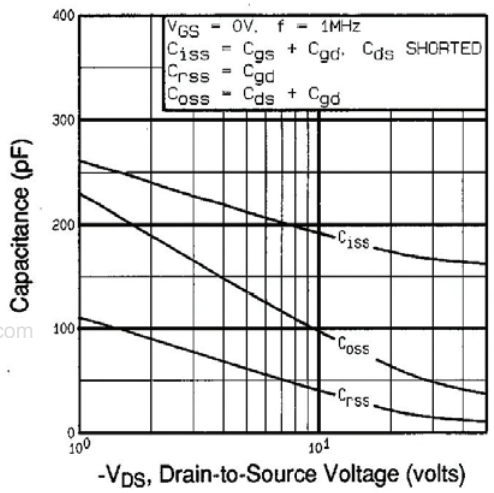


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

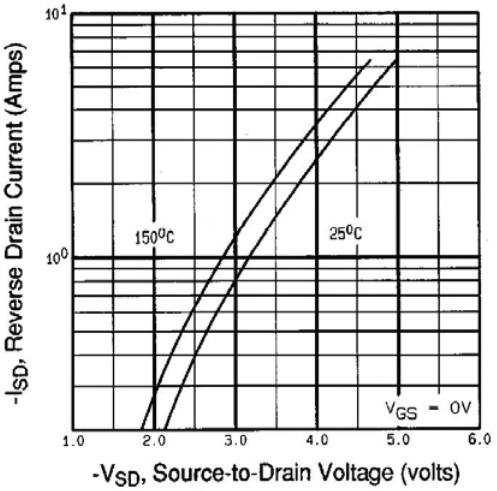


Fig. 7 - Typical Source-Drain Diode Forward Voltage

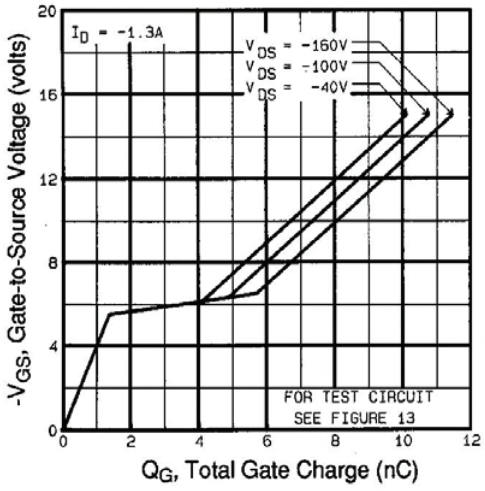


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

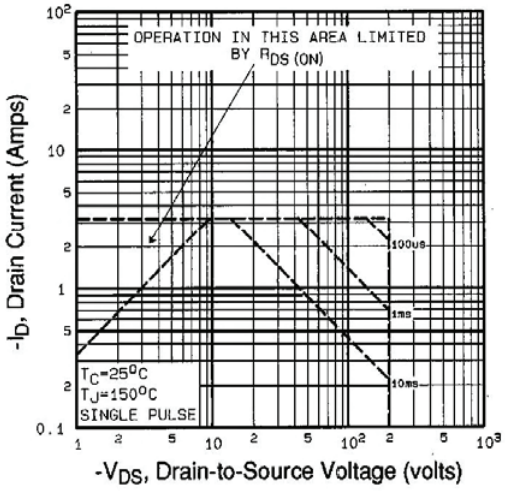


Fig. 8 - Maximum Safe Operating Area

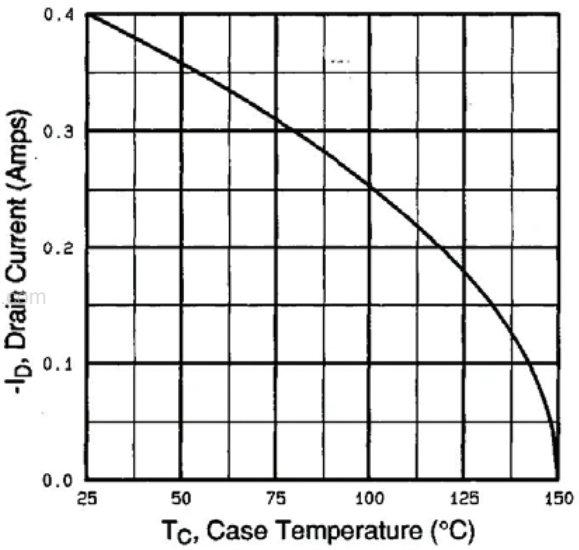


Fig. 9 - Maximum Drain Current vs. Case Temperature

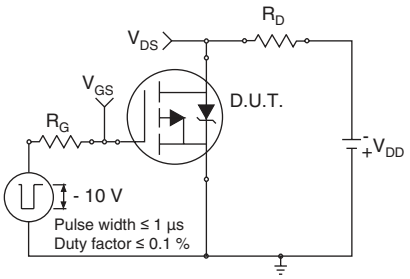


Fig. 10a - Switching Time Test Circuit

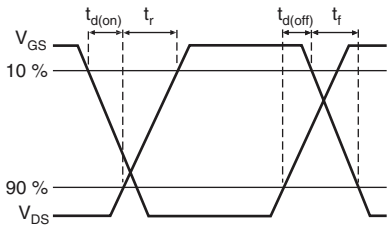


Fig. 10b - Switching Time Waveforms

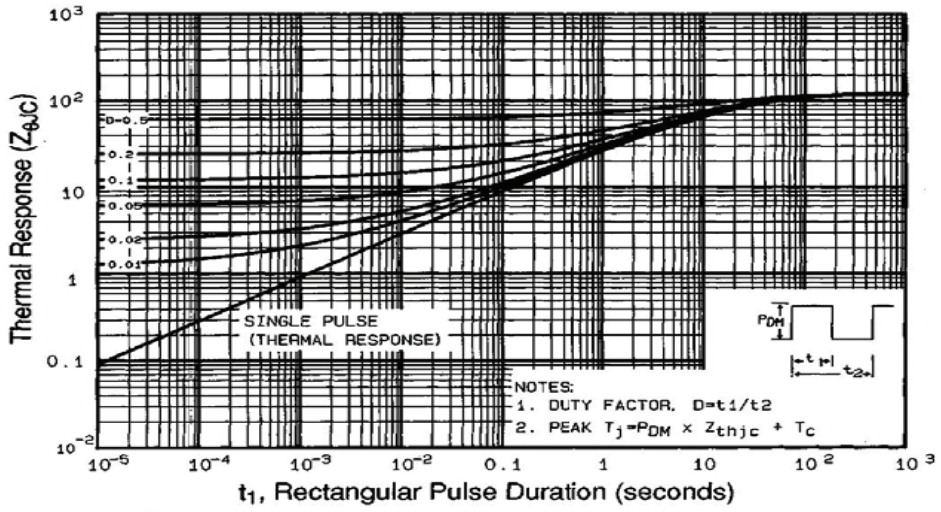


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

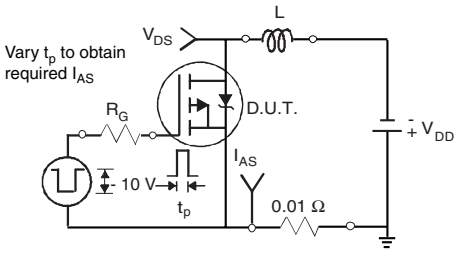


Fig. 12a - Unclamped Inductive Test Circuit

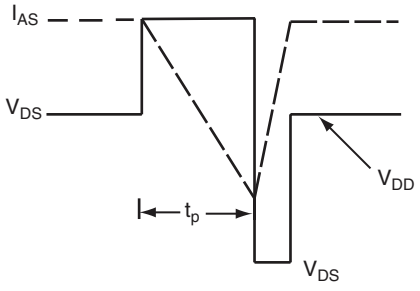


Fig. 12b - Unclamped Inductive Waveforms

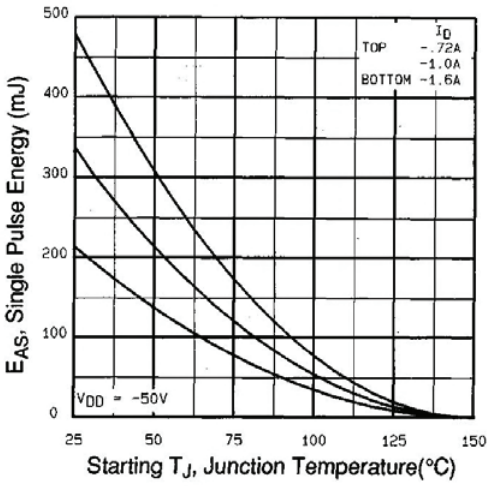


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

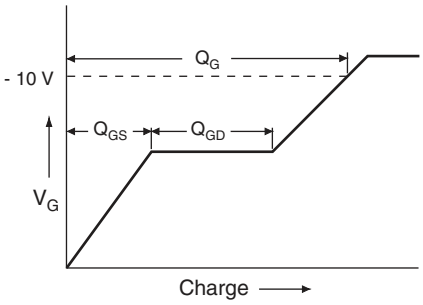


Fig. 13a - Basic Gate Charge Waveform

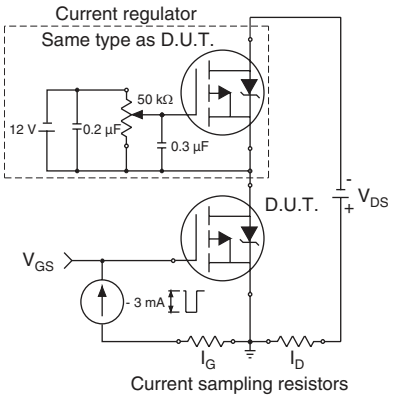
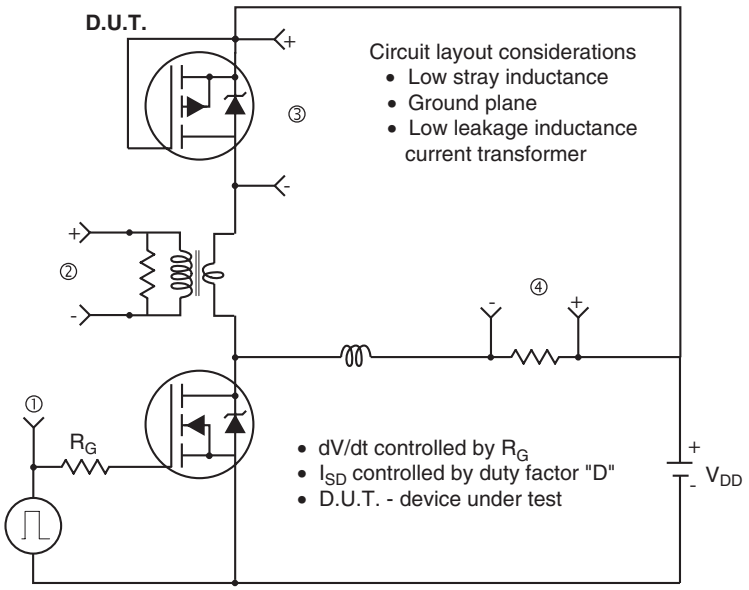
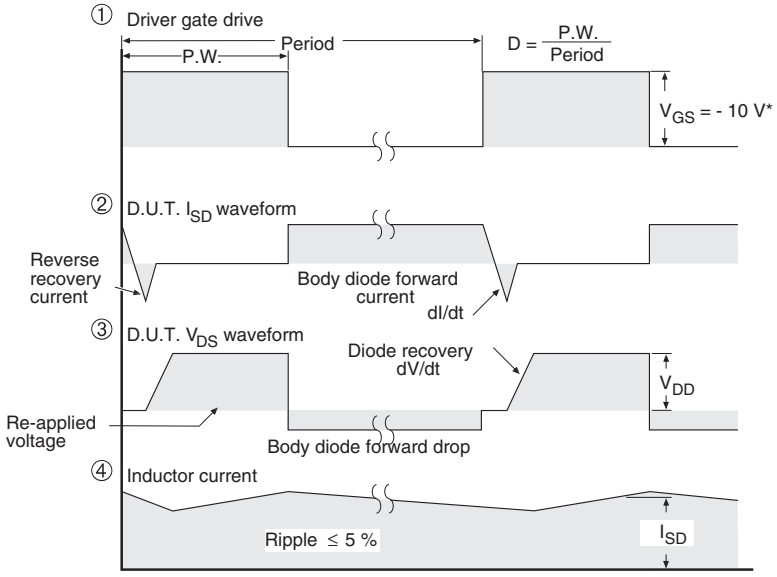


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit





* V_{GS} = - 5 V for logic level and - 3 V drive devices

Fig. 14 - For P-Channel

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