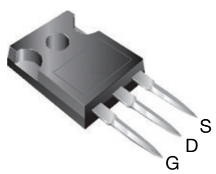
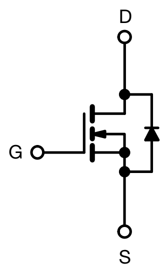
EF Series Power MOSFET with Fast Body Diode

PRODUCT SUMMARY

V_{DS} (V) at T_J max.	650	
$R_{DS(on)}$ max. at 25 °C (Ω)	V_{GS} = 10 V	0.176
Q_g (Max.) (nC)	84	
Q_{gs} (nC)	14	
Q_{gd} (nC)	24	
Configuration	Single	

TO-247AC





N-Channel MOSFET

FEATURES

- Fast body diode MOSFET using E series technology
- Reduced t_{rr}, Q_{rr}, and I_{RRM}
- Low figure-of-merit (FOM): R_{on} x Q_g
- Low input capacitance (C_{iss})
- Increased robustness due to low Q_{rr}
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Telecommunications
  - Server and telecom power supplies
- Lighting
  - High intensity discharge (HID)
  - Light emitting diodes (LEDs)
- Consumer and computing
  - ATX power supplies
- Industrial
  - Welding
  - Battery chargers
- Renewable energy
  - Solar (PV inverters)
- Switch mode power suppliers (SMPS)
- Applications using the following topologies
  - LLC
  - Phase shifted bridge (ZVS)
  - 3-level inverter
  - AC/DC bridge

ORDERING INFORMATION

Package	TO-247AC
Lead (Pb)-free and Halogen-free	SiHG21N60EF-GE3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	600	V
Gate-Source Voltage			V_{GS}	± 30	
Continuous Drain Current (T_J = 150 °C)	V_{GS} at 10 V	T_C = 25 °C	I_D	21	A
		T_C = 100 °C		14	
Pulsed Drain Current [a]			I_{DM}	53	
Linear Derating Factor				1.8	W/°C
Single Pulse Avalanche Energy [b]			E_{AS}	367	mJ
Maximum Power Dissipation			P_D	227	W
Operating Junction and Storage Temperature Range			T_J, T_{stg}	-55 to +150	°C
Drain-Source Voltage Slope	T_J = 125 °C		dV/dt	70	V/ns
Reverse Diode dV/dt [d]				50	
Soldering Recommendations (Peak Temperature) [c]	for 10 s			300	°C

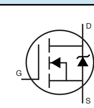
Notes

a. Repetitive rating; pulse width limited by maximum junction temperature.
b. V_{DD} = 50 V, starting T_J = 25 °C, L = 28.2 mH, R_g = 25 Ω, I_{AS} = 5.1 A.
c. 1.6 mm from case.
d. $I_{SD} \leq I_D$, dI/dt = 900 A/μs, starting T_J = 25 °C.

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.55	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA	600	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA	-	0.59	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
		V_{GS} = ± 30 V	-	-	± 1	μA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 480 V, V_{GS} = 0 V	-	-	1	μA
		V_{DS} = 480 V, V_{GS} = 0 V, T_J = 125 °C	-	-	500	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 11 A	-	0.153	0.176	Ω
Forward Transconductance	g_{fs}	V_{DS} = 30 V, I_D = 11 A	-	7	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz	-	2030	-	pF
Output Capacitance	C_{oss}		-	105	-	
Reverse Transfer Capacitance	C_{rss}		-	5	-	
Effective output capacitance, energy related [a]	$C_{o(er)}$	V_{GS} = 0 V, V_{DS} = 0 V to 480 V	-	86	-	
Effective output capacitance, time related [b]	$C_{o(tr)}$		-	299	-	
Total Gate Charge	Q_g	V_{GS} = 10 V, I_D = 11 A, V_{DS} = 480 V	-	56	84	nC
Gate-Source Charge	Q_{gs}		-	14	-	
Gate-Drain Charge	Q_{gd}		-	24	-	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 480 V, I_D = 11 A, R_g = 9.1 Ω, V_{GS} = 10 V	-	21	42	ns
Rise Time	t_r		-	31	62	
Turn-Off Delay Time	$t_{d(off)}$		-	59	89	
Fall Time	t_f		-	27	54	
Gate Input Resistance	R_g	f = 1 MHz, open drain	0.2	0.56	1.2	Ω
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	21	A
Pulsed Diode Forward Current	I_{SM}		-	-	53	
Diode Forward Voltage	V_{SD}	T_J = 25 °C, I_S = 11 A, V_{GS} = 0 V	-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = I_S = 11 A, dI/dt = 100 A/μs, V_R = 400 V	-	135	270	ns
Reverse Recovery Charge	Q_{rr}		-	0.76	1.52	μC
Reverse Recovery Current	I_{RRM}		-	11	-	A

Notes

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}.
b. $C_{oss(tr)}$ is a fixed capacitance that gives the charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

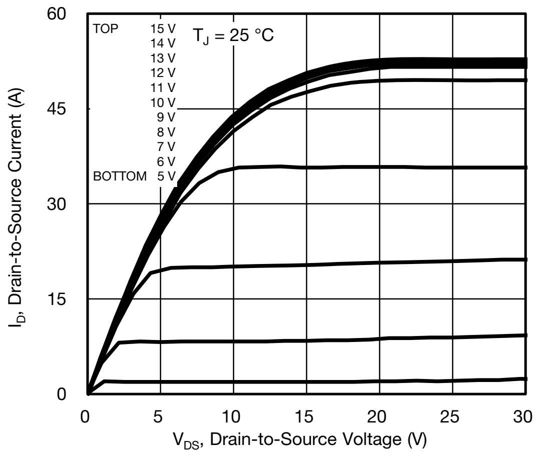


Fig. 1 - Typical Output Characteristics, T_J = 25 °C

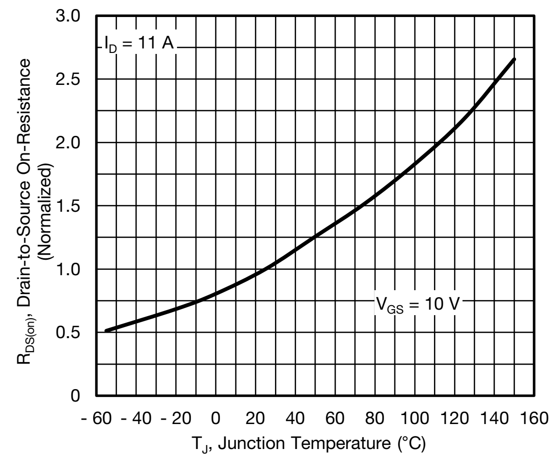


Fig. 4 - Normalized On-Resistance vs. Temperature

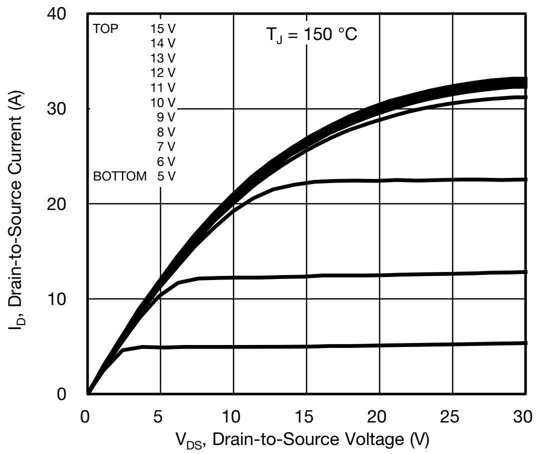


Fig. 2 - Typical Output Characteristics, T_J = 150 °C

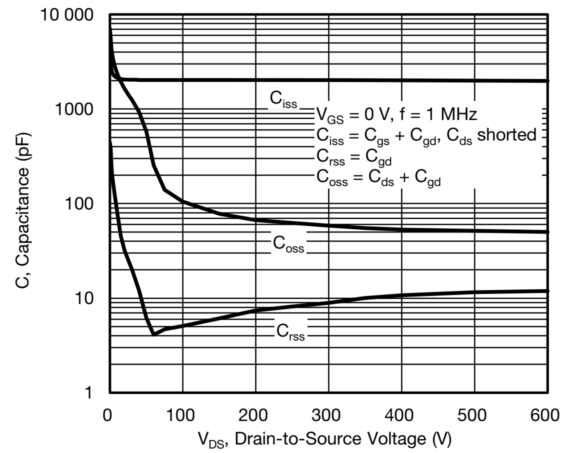


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

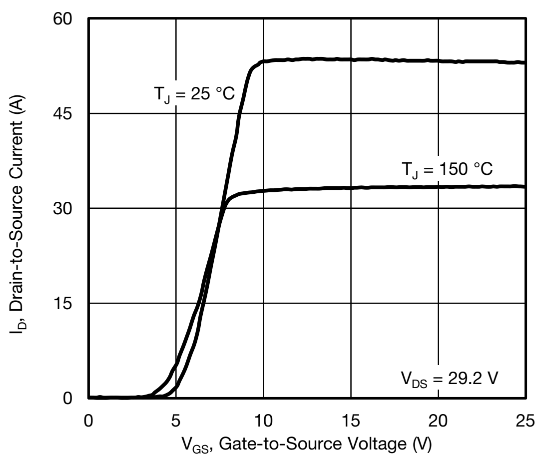


Fig. 3 - Typical Transfer Characteristics

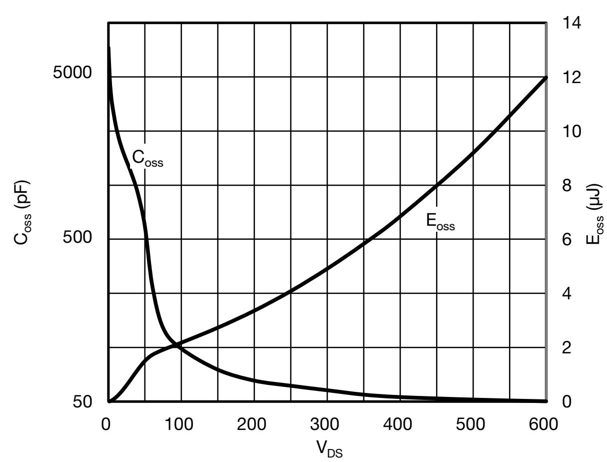


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

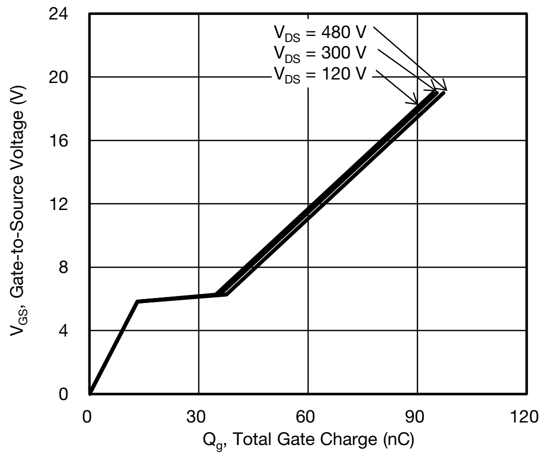


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

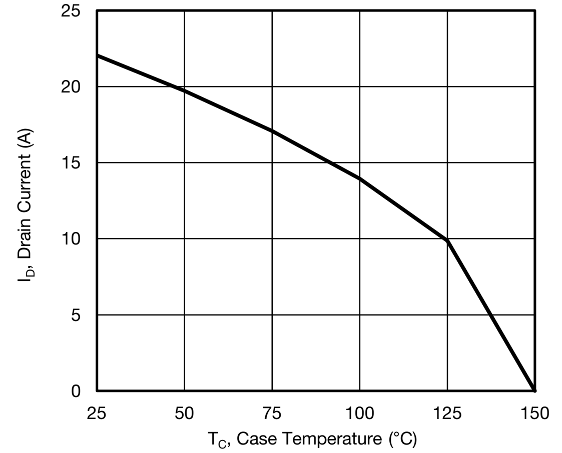


Fig. 10 - Maximum Drain Current vs. Case Temperature

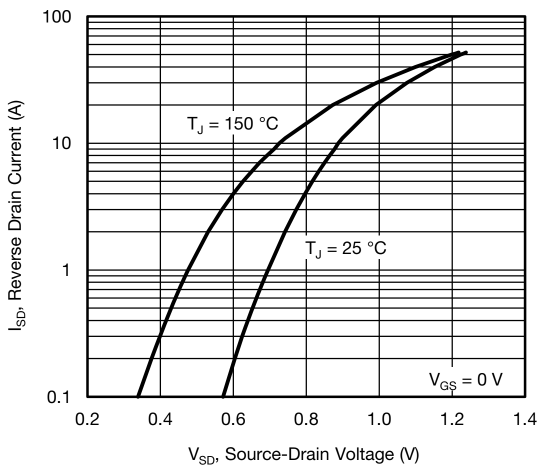


Fig. 8 - Typical Source-Drain Diode Forward Voltage

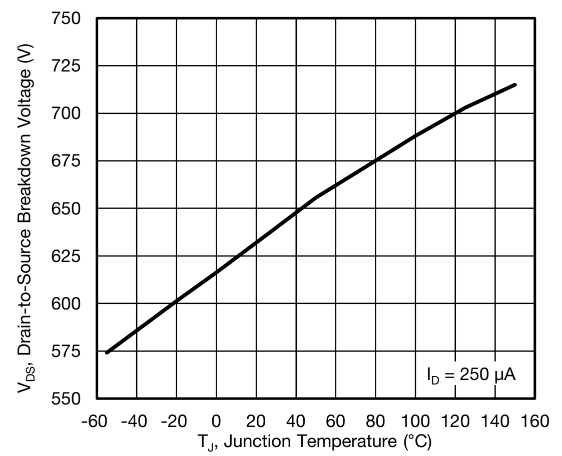
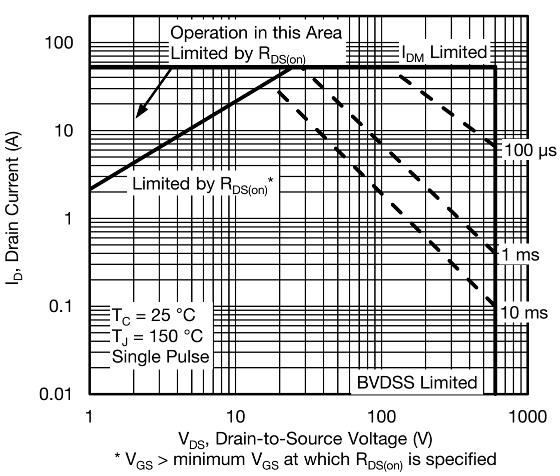


Fig. 11 - Typical Drain-to-Source Voltage vs. Temperature



* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Fig. 9 - Maximum Safe Operating Area

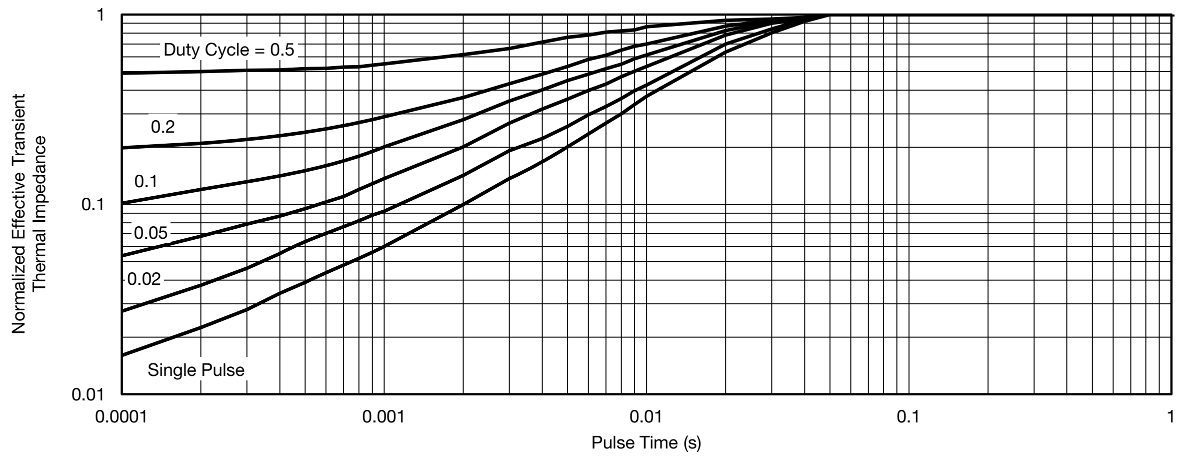


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

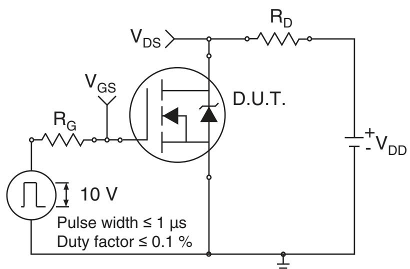


Fig. 13 - Switching Time Test Circuit

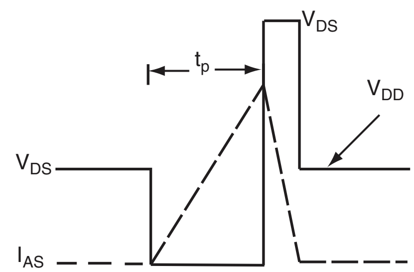


Fig. 16 - Unclamped Inductive Waveforms

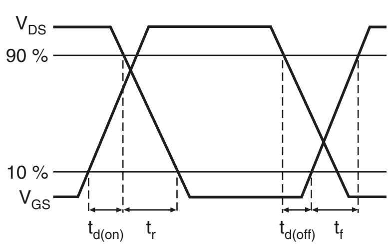


Fig. 14 - Switching Time Waveforms

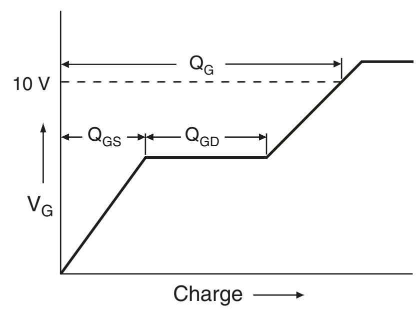


Fig. 17 - Basic Gate Charge Waveform

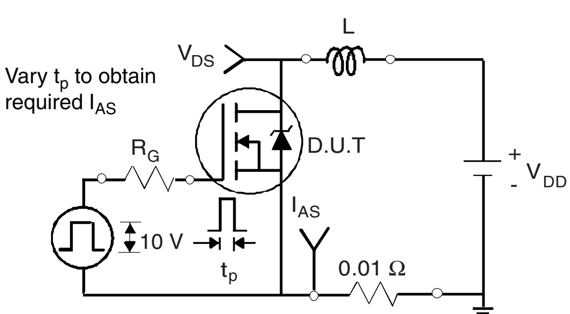


Fig. 15 - Unclamped Inductive Test Circuit

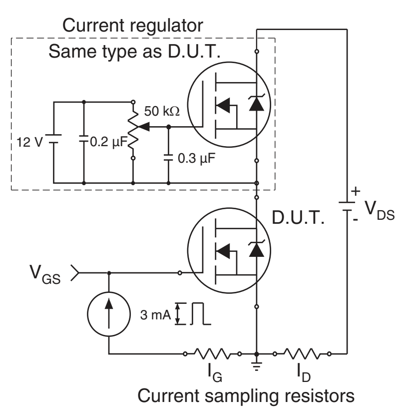
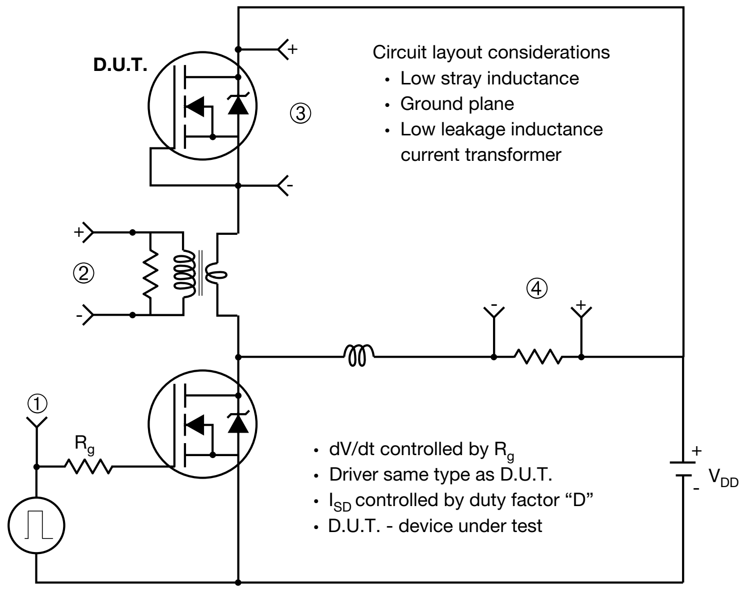
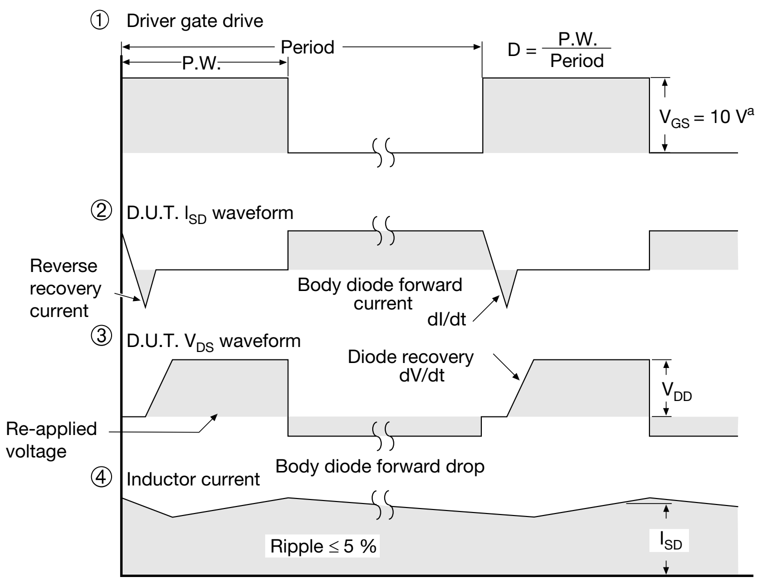


Fig. 18 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit





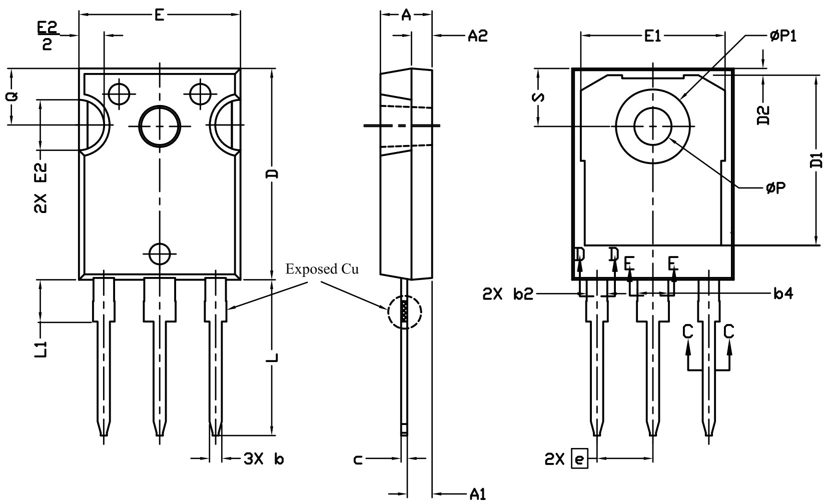
Note

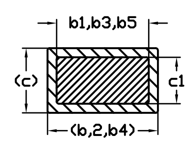
a. V_{GS} = 5 V for logic level devices

Fig. 19 - For N-Channel

TO-247AC (High Voltage)

VERSION 1: FACILITY CODE = 9





Section C--C, D--D, E--E

	MILLIMETERS		
DIM.	MIN.	MAX.	NOTES
A	4.83	5.21	
A1	2.29	2.55	
A2	1.50	2.49	
b	1.12	1.33	
b1	1.12	1.28	
b2	1.91	2.39	6
b3	1.91	2.34	
b4	2.87	3.22	6, 8
b5	2.87	3.18	
c	0.55	0.69	6
c1	0.55	0.65	
D	20.40	20.70	4

	MILLIMETERS		
DIM.	MIN.	MAX.	NOTES
D1	16.25	16.85	5
D2	0.56	0.76	
E	15.50	15.87	4
E1	13.46	14.16	5
E2	4.52	5.49	3
e	5.44 BSC		
L	14.90	15.40	
L1	3.96	4.16	6
Ø P	3.56	3.65	7
Ø P1	7.19 ref.		
Q	5.31	5.69	
S	5.54	5.74	

Notes

(1) Package reference: JEDEC TO247, variation AC

(2) All dimensions are in mm

(3) Slot required, notch may be rounded

(4) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extremes of the plastic body

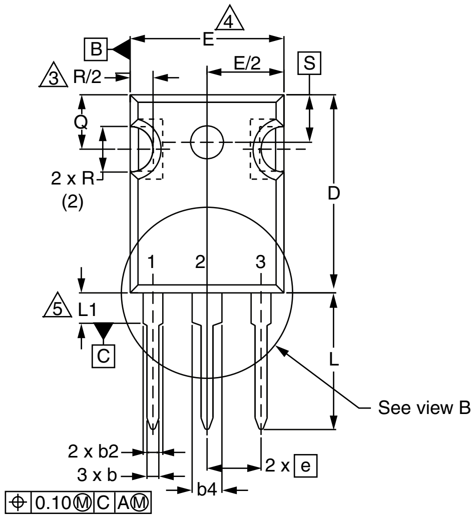
(5) Thermal pad contour optional with dimensions D1 and E1

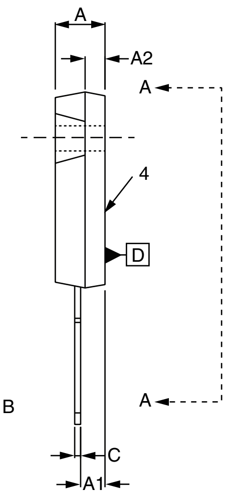
(6) Lead finish uncontrolled in L1

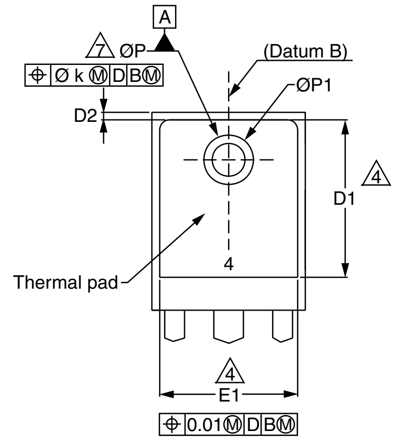
(7) Ø P to have a maximum draft angle of 1.5° to the top of the part with a maximum hole diameter of 3.91 mm

(8) Dimension b2 and b4 does not include dambar protrusion. Allowable dambar protrusion shall be 0.1 mm total in excess of b2 and b4 dimension at maximum material condition

VERSION 2: FACILITY CODE = Y

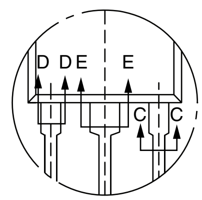




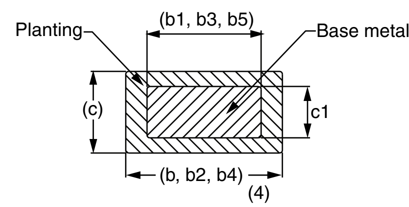


View A - A

Lead Assignments
1. Gate
2. Drain
3. Source
4. Drain



View B



Section C - C, D - D, E - E

	MILLIMETERS				MILLIMETERS		
DIM.	**MIN.**	**MAX.**	**NOTES**	**DIM.**	**MIN.**	**MAX.**	**NOTES**
A	4.58	5.31		D2	0.51	1.30	
A1	2.21	2.59		E	15.29	15.87	
A2	1.17	2.49		E1	13.72	-	
b	0.99	1.40		e	5.46 BSC		
b1	0.99	1.35		Ø k	0.254		
b2	1.53	2.39		L	14.20	16.25	
b3	1.65	2.37		L1	3.71	4.29	
b4	2.42	3.43		Ø P	3.51	3.66	
b5	2.59	3.38		Ø P1	-	7.39	
c	0.38	0.86		Q	5.31	5.69	
c1	0.38	0.76		R	4.52	5.49	
D	19.71	20.82		S	5.51 BSC		
D1	13.08	-					
ECN: E19-0614-Rev. E, 25-Nov-2019 DWG: 5971							

Notes

(1) Dimensioning and tolerancing per ASME Y14.5M-1994
(2) Contour of slot optional
(3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
(4) Thermal pad contour optional with dimensions D1 and E1
(5) Lead finish uncontrolled in L1
(6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")
(7) Outline conforms to JEDEC outline TO-247 with exception of dimension c
(8) Xian and Mingxin actually photo

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